Thesis for the Degree of Master of Engineering

Design of Broadband Balanced Power Amplifier for High Precision Radar Sensors in CMOS Technology

Advisor: Professor Jung-Dong Park

Hyeonseok Lee

Graduate School of Dongguk University
Department of Electronic and Electrical Engineering
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by

Hyeonseok Lee

Advisor: Professor Jung-Dong Park

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Approved by:

Chairman : Professor Joon-Hyeon Jeon (Sign)

Committee member : Professor Min-Sung Kim (Sign)

Committee member : Professor Jung-Dong Park (Sign)

Graduate School of Dongguk University

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ABSTRACT

This work presents a W-band 8-way broadband power amplifier (PA) for a high-precision frequency modulated continuous wave (FMCW) radar in 65-nm CMOS. A balanced architecture is implemented with the Lange coupler to achieve a broadband operation with increased output power for high-range resolution and high-distance coverage of FMCW radar sensors. The coupler naturally combines the output power from two 4-way push-pull PAs. Utilizing a transformer-based push-pull topology and a cross-coupled capacitive neutralization technique, the gate-drain capacitance of the 4-way PA is compensated for the stabilization with improved power gain. Matching networks were carried out using transformers for minimizing the loss from the matching networks and a minimal area occupation. Due to antenna load impedance variance at the reference impedance, the robustness of the power amplifier was assessed in terms of the output power and the output return loss. The implemented 8-way balanced PA performs a saturated output power (P_{sat}) of 16.5 dBm and a 1-dB compressed output power (OP_{1dB}) of 13.3 dBm with a power added efficiency (PAE) of 9.9% at 90 GHz. Moreover, The PA attain 3-dB power bandwidth of 20.4 GHz (79.2-99.6 GHz).

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Chapter 1 Introduction

This thesis has proposed to implement the development of a W-band 8-way power amplifier with the Lange Couplers by combining two 4-way transformer-based push-pull power amplifiers for improvements in the output power, efficiency, and wide bandwidth for a high precision FMCW radar. The W-band PA was implemented in 65-nm CMOS. These paragraphs provide an overview of the thesis:

Chapter 2: The basic theory and architecture of FMCW radars are described. By investigating the range detection and estimation process in FMCW radars, it has been demonstrated the necessity of a broadband PA for high-precision FMCW radars. Accordingly, W-band (75-110 GHz) has been selected as an operation frequency band in order to achieve a wide bandwidth. Additionally, the problems of designing a mm-wave CMOS PA and design solutions are discussed: capacitive cross-coupled neutralization and power combining.

Chapter 3: There is a detailed design specification for the 90 GHz 4-way push-pull power amplifier. The 4-way push-pull PA is used for 8-way PA by combining two 4-way push-pull PA. To minimize parasitic capacitance effects on transistors, capacitive cross-coupled neutralization is utilized in the PA, and its theory is explained. In addition, a transformer-based matching network as well as a combiner/divider is also analyzed. It is shown that the equivalent circuit consisting of lumped components is capable of highly meeting the conjugate matching for

minimizing the insertion loss and reflection, and that it effectively matched the transformer-based matching networks. The EM simulation results of transformer-based matching networks were almost identical to the results that were obtained when lumped component parameter extractions were conducted. It is implemented with two transformer-based combiner and divider at both the input and output, which have low insertion loss and are electrically balanced. The small-signal and large-signal results are shown at the end of the chapter.

Chapter 4: The 8-way broadband balanced power amplifier for 90 GHz is proposed which is composed of two 4-way push-pull amplifiers. The Lange coupler, a lambda-based combiner, is utilized because multiple fingers of coupled lines are distinguished by large coupling coefficients. When considering that an 8-way combining for high output power is available, the length of the quarter wave at W-band is acceptable, 450 um. The presented PA is also robust to load variations with regards to the return loss of the output and the output power of the PA. As a result, it measured the output power of 16.5 dBm with 26.7 dB gain, 9.9% PAE at 90 GHz, 13 GHz (83–96 GHz) of 3-dB gain bandwidth, more than 20 GHz of 3-dB power bandwidth, and 1.5 dB of variation in the saturated output power. Utilizing a hybrid combining technique in conjunction with transformer-based push-pull PAs, the presented PA attains improved output power, gain, and bandwidth, contributing to the highest Figure-of-Merit (FoM) among recently reported CMOS PAs operating at 90 GHz.

Chapter 5: In the conclusion of the thesis, there is a summary that describes the work. In addition, the possibility of future applications of the proposed W-band PA and my suggestions for future work will be discussed.

Chapter 2 Power Amplifier for FMCW Radar

2.1 FMCW Radar

2.1.1 Basic Theory of FMCW Radar

Frequency-modulated continuous-wave (FMCW) radar sensors have been widely used for airborne radars, automotive cruise control, and weather radars. With the use of millimeter-wave radar sensors, it is possible to achieve higher spatial and range resolution due to their wide sweeping bandwidth, as well as a narrower beamwidth for a given antenna size. Furthermore, small-size antennas and low oxygen attenuation at W-band are appealing for improving propagation loss when implementing coherent multi-receiver integrations to improve sensitivity [2]. One of the most important characteristics of a high-precision FMCW radar is its sweep bandwidth, which is crucial to the improvement of high range resolution.

Figure 2.1-1 shows the coverage of automotive radars and the basic architecture of FMCW radars. As the frequency modulated waveform is excited by a synthesizer, it is then sent to a power amplifier (PA) and a mixer. The amplified signal from a PA is transmitted into free space and may interfere with some targets. The reflected signal is received by a low noise amplifier (LNA) which enhances the received signal while minimizing the noise figure (NF) to achieve a high signal to noise ratio (SNR). The received signal is then mixed with the original modulated signal to obtain the beat frequency. The beat frequency is used for range and velocity detection after

digitally processing the signal in an analog to digital converter (ADC).

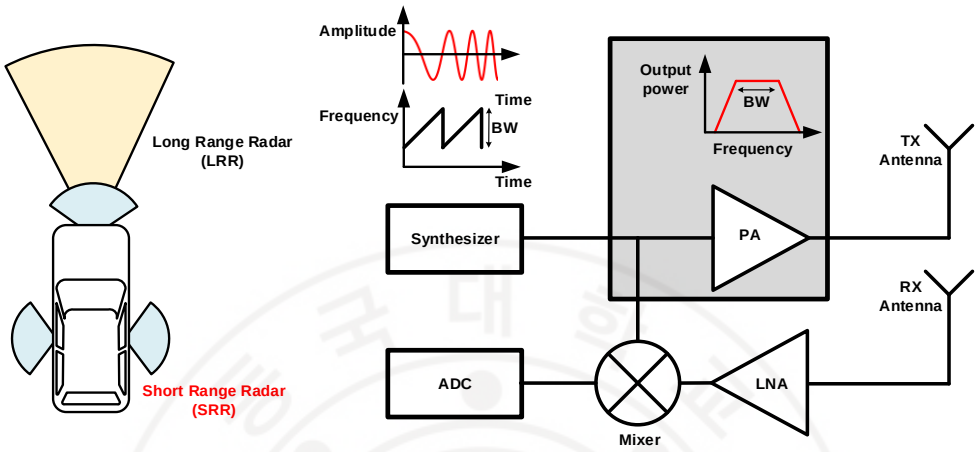


Figure 2.1-1 Architecture of FMCW radar

2.1.2 Necessity of Broadband PA for high precision FMCW Radar

Fig. 2.1-2 illustrates the detection procedure of distance and velocity as described in the text. A two-dimensional matrix is constructed by performing fast Fourier transform (FFT) on one chirp to get range bins and doing FFT on all chirps to get doppler bins. A beat frequency (f_{beat}) is defined as the difference between the transmitted chirp frequency and the received chirp frequency, which is acquired by down conversion in a mixer in order to conduct range detection and estimation. The delay time (t_d) is determined by the sweep rate which is easily obtainable because it equals the rate between the sweep time (T_{sweep}) and the sweep bandwidth (BW) [3].

$$t_d = f_{beat} \times \frac{T_{sweep}}{BW} \tag{2.1-1}$$

The range detection and estimation of targets are conducted by using t_d.

Moreover, the range resolution of FMCW radars for distinguishing two or more targets is determined by the minimum frequency difference (Δf) between f_{beat1} and f_{beat2} in the range bins.

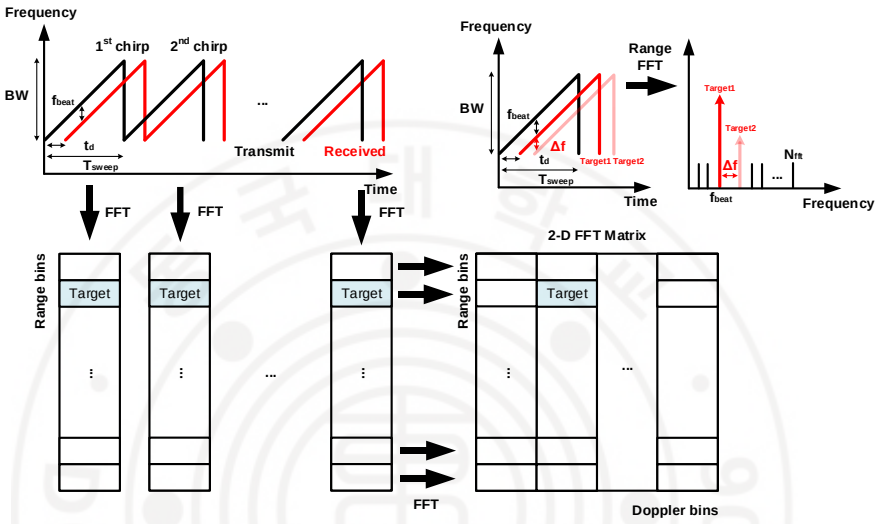


Fig 2.1-1 Range and doppler FFT for 2-D FFT matrix

Two targets can be distinguished as long as Eq. (2.1-2) is satisfied, where Δf is larger than the inverse of T_{sweep} is satisfied, two targets are distinguishable.

$$\Delta f > \frac{1}{T_{sweep}} \tag{2.1-2}$$

$$\Delta f = \Delta t_d \times \frac{BW}{T_{sweep}} \tag{2.1-3}$$

By substituting the left side of Eq. (2.2-2) to the right side of Eq. (2.2-3) with the introduction of the velocity formula, Eq. (2.2-2) becomes below

$$\frac{2\Delta d_{res} \times BW}{cT_{sweep}} > \frac{1}{T_{sweep}} \tag{2.2-4}$$

Where c is the speed of light and Δd_{res} is the minimum range resolution.

Then, Δd_{res} is decided by the sweep bandwidth (BW) as equation (2.2-5) is shown in below

$$\Delta d_{res} > \frac{c}{2BW}. \tag{2.2-5}$$

In this regard, the BW is decisive for high range resolution FMCW radars. As Figure 2.1-1 is shown, PAs for high precision FMCW radars should achieve high output power with the flatness over the BW. Table 2.1-1 shows 10% fractional bandwidth and the corresponded range resolution at S- (2-4 GHz), X- (8-12 GHz), Ka- (26.5-40 GHz) and W- (75-110) band. As can be seen, the sweep bandwidth of FMCW radar needs to be as wide as 10 GHz to distinguish objects which are 1.5 cm apart [4], which is around 10% of the fractional bandwidth of a 90 GHz FMCW radar sensor. In this thesis, the W-band PA in 65-nm CMOS technology is proposed with a high output power over a wide bandwidth which is suitable for the application of high precision FMCW radars.

Table 2.1-1 Fractional bandwidth and range resolution of different operating frequency

Operating Frequency	10% Fractional Bandwidth	Range Resolution
S-Band (2-4 GHz)	0.3 GHz	0.5 m
X-Band (8-12 GHz)	1 GHz	15 cm
Ka-Band (26.5-40 GHz)	3.3 GHz	4.5 cm
W-Band (75-110 GHz)	10 GHz	1.5 cm

2.2 mm-wave Power Amplifier in CMOS

As CMOS technology is advanced, a bulk silicon-based CMOS technology has been considered one of the most popular technologies for mass production, due to its low-cost and high-level integration features. Design of broadband power amplifiers in a nanoscale CMOS, however, is quite challenging because of the channel length modulation effect in the nanoscale CMOS, which appreciably affects the output power, linearity, and power gain.

2.2.1 Gain and Power limitations

Figure 2.2-1 shows RF performance of bulk CMOS technology. As the gate length is increased, the cutoff frequency (F_t) and the maximum oscillation frequency (F_{max}) are also increased which means the device in the more scaled technology achieves high gain [5]. However, the F_t is typically compromised by $F_t \times V_{bd}$ = 200 GHz·V [6]. Thus, for a nanoscale CMOS technology with higher F_t, a relatively

lower breakdown voltage (V_{bd}) is expected which demonstrates it is challenging for a mm-wave PA in CMOS technology to perform both a high output power and efficiency.

Moreover, with the increase in operating frequency, the maximum available gain (MAG) and maximum stable gain (MSG) both decrease correspondingly, thus deteriorating the power gain and efficiency, as well as limiting the gain flatness to get wide bandwidth for FMCW radars at the millimeter-wave regime.

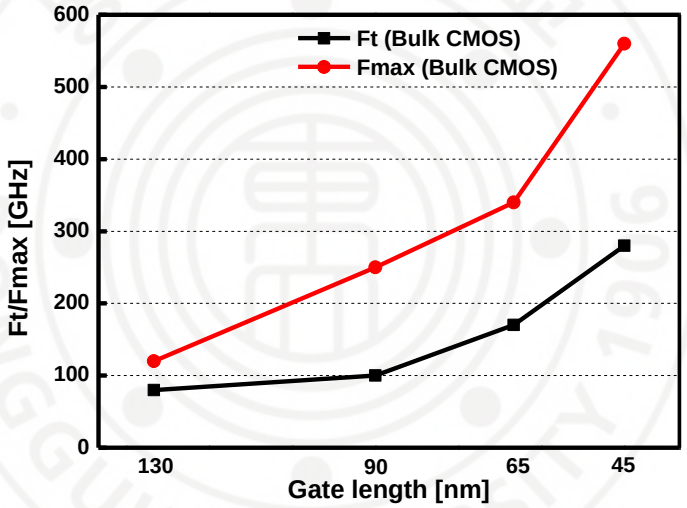


Figure 2.2-1 RF performance of bulk CMOS Technology

It needs to be noted that the power bandwidth required by the PA to meet the sweep bandwidth requirement must extend 3 dB above the power bandwidth of the employed PA. To keep sidelobes from being produced by the undesirable amplitude modulation of the output power level, it is needed that the flatness variation in the output power level is kept to a minimum. In Figure 2.2-2, MAG/MSG, the current

gain (H_{21}) and the maximum unilateral gain (U) of a transistor in TSMC 65-nm CMOS technology which is used for designing the proposed W-band PA are plotted. The maximum oscillation frequency (F_{max}) is the frequency in which maximum unilateral gain (U) is zero, and the cutoff frequency (F_t) is that in which the current gain (H_{21}) is zero. The F_{max} and Ft are 210 GHz and 225 GHz, respectively. Thus, the transistors of W-band PAs in 65-nm CMOS technology operate at only around 45 % of the F_{max} and Ft. It indicates that the matching network of PAs should be carefully designed so that the insertion loss can be minimized in order to obtain an acceptable gain and efficiency level.

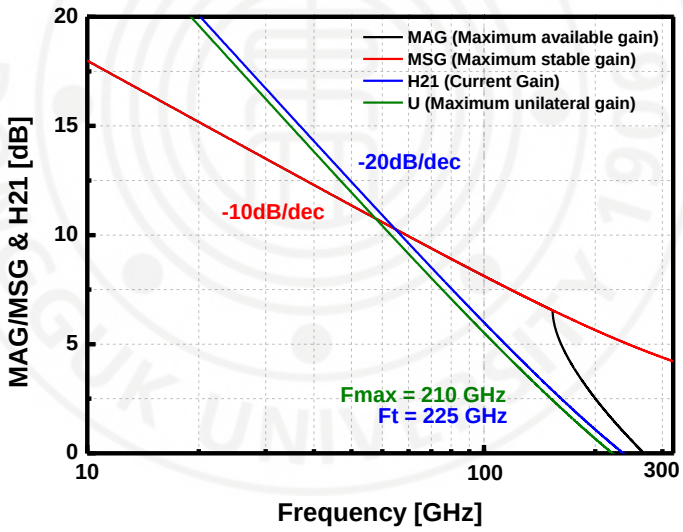


Figure 2.2-2 TSMC 65-nm CMOS device small-signal simulation results

In RF transistors, the main cause of the MAG and MSG reduction has been identified as the presence of parasitic capacitances. Hence, the common-source (CS) topology with the capacitive cross-coupling neutralization method has been widely

used in millimeter-wave amplifiers to compensate for parasitic capacitances [7]. The gate-drain capacitance C_{gd} develops undesirable shunt feedback which leads to decreased gain and stability of the system. In a push-pull arrangement, cross-coupled neutralization capacitors C_n are placed across the drain of one transistor and the gate of the other transistor to eliminate this problem. Moreover, the value of C_n should be carefully chosen since overcompensating the capacitive neutralization can result in positive feedback. Accordingly, the power gain and power addition efficiency (PAE) need to be compromised with stability. In chapter 3.2, the operation of the cross-coupled neutralization and the choice of the capacitors value are described in detail.

2.2.2 Power Combining Techniques

One of the most important parameters that must be taken into account while designing millimeter-wave CMOS PAs is the saturated output power (P_{sat}) which is determined by a suitable active device size, given a feasible output matching network. Because of low breakdown voltages of CMOS PAs, which are usually implemented with a low supply voltage of around 1 V due to thin oxide layers on MOS, it is difficult to achieve an efficient output power matching network with a relatively large device. There have been considerable efforts in the literature in order to resolve this issue. Stacking MOS transistors can increase output voltage, but ultimately requires expensive SOI technology if more than two transistors must be stacked [8]. There are various power combining techniques that have been more prevalently used to boost the output power of a PA. Transmission-line-based combiner [10,11], λ/4-

based combiner [12,13], and transformer-based combiner [13–17] are widely used to boost the output power. Figure 2.2-3 shows schematic of these different power combining techniques.

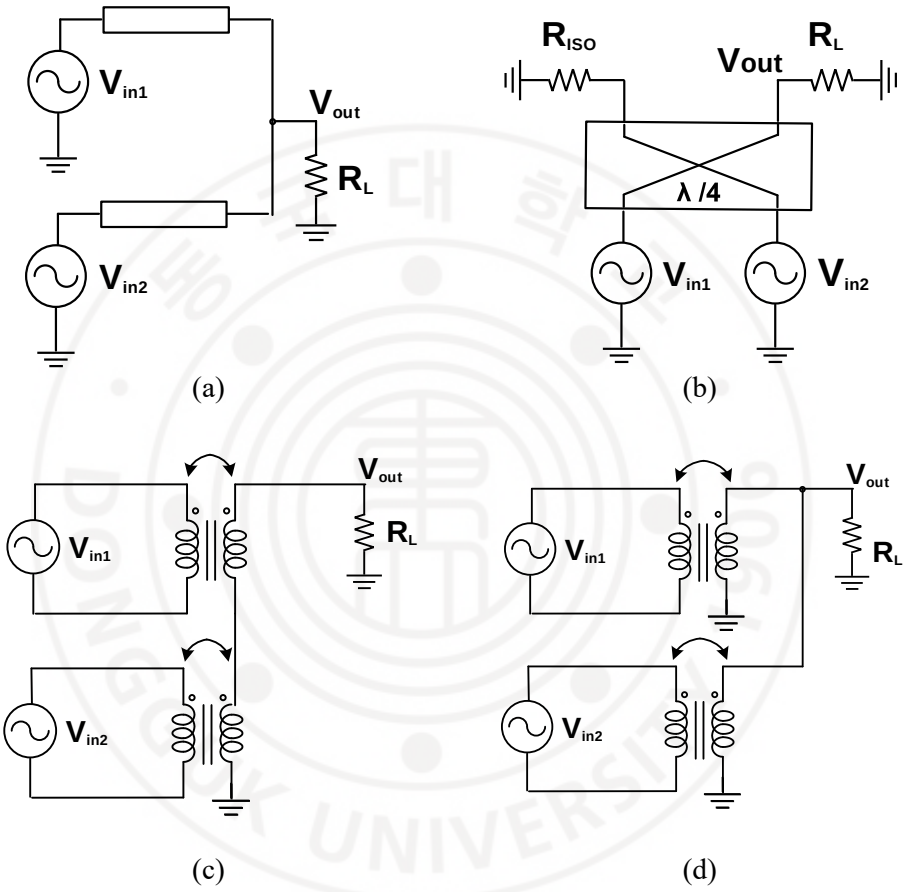


Figure 2.2-3 Schematics of different power combining techniques: (a) Transmission line-based combiner. (b) λ/4-based combiner. (c) Transformer-based series combiner (d) Transformer-based parallel combiner

Transmission-line-based combiner is usually used for combining multiple transistors due to its simple combining components. However, the combiner

occupies too much space, and long transmission-lines induces quite large insertion loss compared to other power combining methods. λ/4-based combiner is based on quadrature couplers and is normally implemented with an isolation resistor (R_{ISO}). The λ/4 transmission line delays the phase of the signal by 90 degree which can be utilized for the compensation of the reflected signal by R_{ISO}. Thus, λ/4-based combiner naturally combines power with a high return loss but the number of combined transistors is limited to two and the length of λ/4 transmission line requires large space. Transformer-based power combining is considered to be the most widely adopted technique out of these approaches due to its simplified matching network and the fact that no additional AC coupling capacitor is necessary, which has a very low quality factor in the millimeter-wave regime. There are two different types of transformer-based power combiner: series voltage mode combiner and parallel current mode combiner. Series combiners combine a power by adding voltage coupled by a transformer. As voltage is added on the load impedance 50 Ω, the effective load impedance seen at V_{in} is smaller than 50 Ω. Meanwhile, as current is added on the load impedance 50 Ω, the effective load impedance seen at V_{in} is larger than 50 Ω. Since the coupler is physically symmetrical, it forms electrical symmetry, thus minimizing the amplitude impedance and phase impedance between the two signals being combined. To combine two push-pull differential PAs and acquire single-ended output port with remaining the electrical balance, transformer-based parallel combiner is used which converts a differential signal to single-ended signal

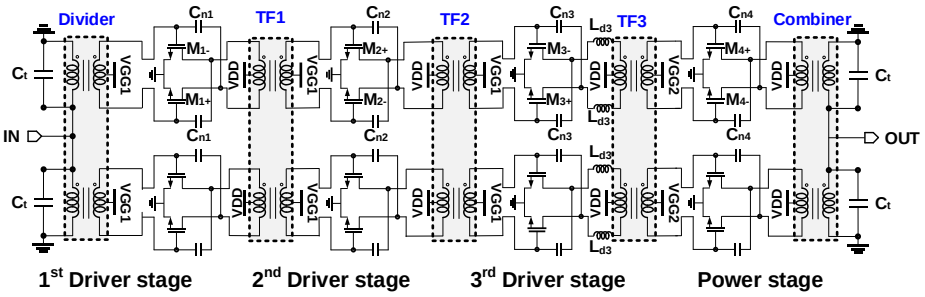
in the proposed PA. In addition, λ/4-based combiner limits itself more than two combine only two ports. However, the proposed W-band PA uses λ/4-based combiner and combines two single-ended ports each obtained by two transformer-based parallel combiners to integrate a larger number of devices with a high return loss and an acceptable size regarding high output power at mm-wave.

Chapter 3 90 GHz 4-Way Push-Pull Power Amplifier

The proposed balanced 8-way PA consists of the two transformer-based 4-way push-pull PAs combined with the Lange couplers. The 4-way PA described in this section is constructed by using the transformer-based power dividers and combiners in the current mode architecture.

3.1 Architecture of 4-Way PA

The schematic diagram of the proposed 4-way, 4-stage PA is shown in Figure 3.1-1. It is composed of an input power divider and output power combiner in the current domain, two 2-way PAs with the push-pull pairs utilizing transformer-based interstage matching networks with a compact size and a low insertion loss which are named TF1, TF2 and TF3. The capacitive neutralization technique was applied to enhance the impedance matching and stability of the circuit for every pair of push-pull inputs of the 2-way PA. Also, two push-pull PAs are synthesized in the current domain with a transformer-based combiner which can increase the effective impedance seen from each push-pull PA by twice. As a result, It ultimately helps in choosing an appropriate output device size of the PA to improve the power efficiency and the current handling capability of the output matching network. A description of the value of device parameters and the extracted transformer parameters is also given in Figure 3.1-1.



Device parameters

W_1	32×0.8 um(M_1)	C_{n1}	12 fF	L_{d3}	20 pH
W_2	32×0.8 um(M_2)	C_{n2}	12 fF	VGG1	0.6 V
W_3	32×1 um(M_3)	C_{n3}	14.3 fF	VGG2	0.7 V
W_4	48×1 um(M_4)	C_{n4}	19 fF	VDD	1.2 V

Transformer parameters

	L_1	L_2	M	R_1	R_2	R_t
TF1	71.1 pH	82.2 pH	46.9 pH	2.2 Ω	3.9 Ω	339 mΩ
TF2	65.5 pH	76.5 pH	42.7 pH	2.1 Ω	3.8 Ω	293 mΩ
TF3	39.4 pH	54.7 pH	21.8 pH	1.7 Ω	3.5 Ω	62 mΩ

Figure 3.1-1 Schematic of the 4-way transformer-based push-pull power amplifier used in the balanced 8-way PA

3.2 Push-pull PA Unit Cell

To improve the stability factor in the proposed PA, the push-pull structure with the use of a differential pair utilizing the capacitive neutralization method as shown in Figure 3.1-1.

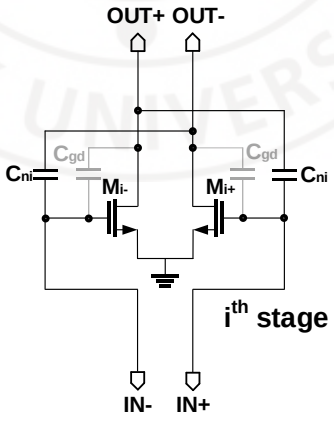


Figure 3.2-1 Schematic of the push-pull PA unit cell

The schematic of a push-pull PA unit cell at each stage with the common-source (CS) topology is shown in Figure 3.2-1. Parasitic gate-drain capacitance (C_{gd}) and cross-coupled neutralization capacitors (C_n) at each stage. It is the result of this architecture that improves the impedance matching, the isolation between the input and output, as well as the gain for every consecutive stage.

3.2.1 Theory of Capacitive Cross-coupled Neutralization

The cutoff frequency (F_t) and the maximum oscillation frequency (F_{max}) in a Metal-oxide-semiconductor field-effect transistor (MOSFET) device are defined by the expression

$$F_t \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{3.2-1}$$

$$F_{\max} \approx \sqrt{\frac{f_t}{8\pi R_g C_{gd}}} \tag{3.2-2}$$

where R_g and R_d are series parasitic gate and drain resistance in common source amplifier. Both of them are zero for Eq. (3.2-1), and only R_d is zero for Eq. (3.2-2). It shows that the denominator term C_{gd} and C_{gd} indicating the parasitic capacitances degrade the RF performance of the transistor.

In Figure 3.2-2 small-signal schematic of differential common-source amplifiers with cross-coupled neutralization capacitors is described. The active device is depicted as a voltage controlled current source with a transconductance (g_m), the parasitic capacitances (C_{gs}, C_{gd} and C_{ds}) the non-quasi static model gate-source resistance (R_g) the internal gate-drain resistance and (R_{ds}).

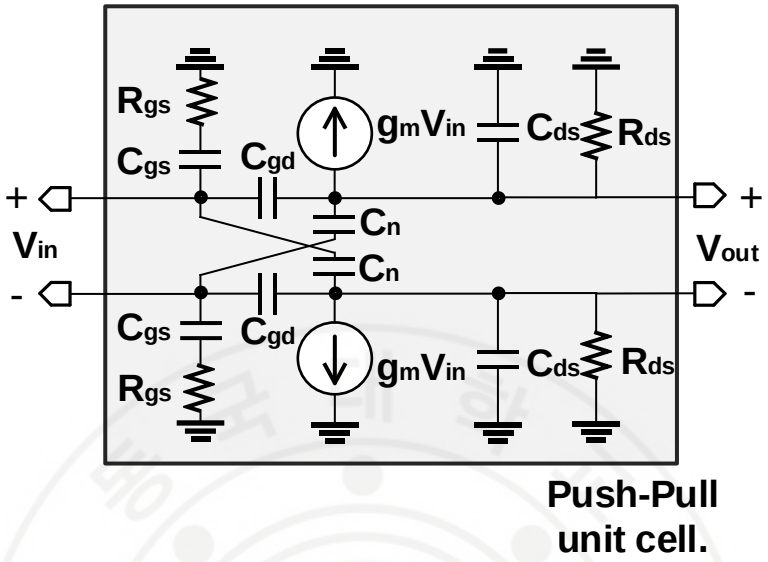


Figure 3.2-2 Small-signal schematic of differential common-source amplifiers with cross-coupled neutralization capacitors.

Further, the small-signal model of the intrinsic device is easily analyzed by introducing Y-parameters equivalent circuit [7]. Figure 3.2-3 shows the equivalent circuit of Y-parameters. The matrix of Y-parameters is described in Eq. (3.2-3) regarding Figure 3.2-3.

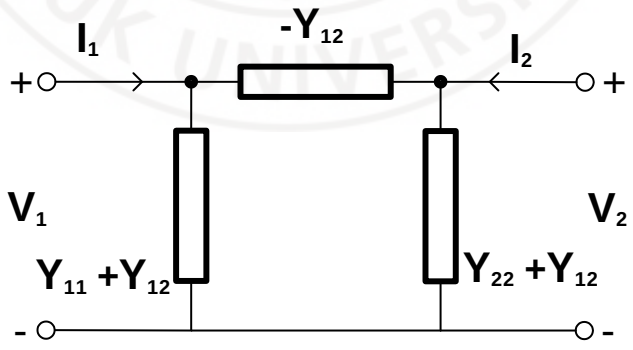


Figure 3.2-3 Equivalent circuit of Y-parameters

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{3.2-3}$$

Thus, Eq. (3.2-4) ~ (3.2-7) can be derived from the intrinsic small-signal model in figure (3.2-2). It is noteworthy that both Y_{12} and Y_{22} have $C_{gd} - C_n$ because they are the short-circuit reverse admittance and transfer admittance respectively. That means, by introducing cross-coupled neutralization capacitors, the stability, gain and efficiency of the device are improved.

$$Y_{11} = \frac{w^2 R_{gs} C_{gs}^2 + jwC_{gs}}{w^2 R_{gs}^2 C_{gs}^2 + 1} \; jwC_{gs} + jw(C_{gd} + C_n) \tag{3.2-4}$$

$$Y_{12} = -jw(C_{gd} - C_n) \tag{3.2-5}$$

$$Y_{21} = g_m - jw(C_{gd} - C_n) \tag{3.2-6}$$

$$Y_{22} = \frac{1}{R_{ds}} \; jwC_{ds} + jw(C_{gd} + C_n) \tag{3.2-7}$$

Rollett's stability factor (k) is expressed by equation (3.2-8) which characterizes the stability of two port networks [18]. The stability factor should be larger than 1 for the stable condition of the network.

$$k = \frac{2\,\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} \tag{3.2-8}$$

By introducing eq. (3.2-4) ~ (3.2-7) to eq. (3.2-8), stability factor (k) can be derived as

$$k = \frac{2w^2 \frac{R_{gs}}{R_{ds}} C_{gs}^2 + w^2 (C_{gd} - C_n)^2}{w|C_{gd} - C_n| \sqrt{g_m^2 + w^2 (C_{gd} - C_n)^2}} \tag{3.2-8}$$

assuming $w^2 R_{gs}^2 C_{gs}^2 \ll 1$ with the proper device size and operating frequency.

When C_n approaches to C_{gd}. k is the largest which means the stability of PA is enhanced. Also, the maximum available gain (MAG) with the conjugate matching impedances of the input and output is expressed as

$$MAG = \left|\frac{Y_{21}}{Y_{12}}\right| (k - \sqrt{k^2 - 1}) \cdot \quad (3.2\text{-}9)$$

$$MSG = \left|\frac{Y_{21}}{Y_{12}}\right| \cdot \quad (3.2\text{-}10)$$

The maximum stable gain (MSG) is used when the k is below than 1. From eq. (3.2-4) ~ (3.2-7), MSG is defined as follows

$$MSG = \sqrt{1 + \frac{g_m^2}{w^2 (C_{gd} - C_n)^2}} \quad (3.2\text{-}11)$$

The push-pull PA unit cell can achieve the maximum value of MAG when C_n equals to C_{gd}.

3.2.2 Choice of Cross-coupled Neutralization Capacitors

The value of the neutralization capacitor was selected to be close to the C_{gd} of a transistor. If the value of C_n is larger than the C_{gd}, it would construct positive feedback which is the stability of PA. Figure 3.2-4 shows the MSG and MAG of the differential pair in the power stage depending on the neutralization capacitance C_{n4} over frequency. In this design, C_{n4} = 19 fF was chosen, and it is verified that the active device with the capacitive neutralization technique was unconditionally stable from the extracted K and |Δ| at W-band.

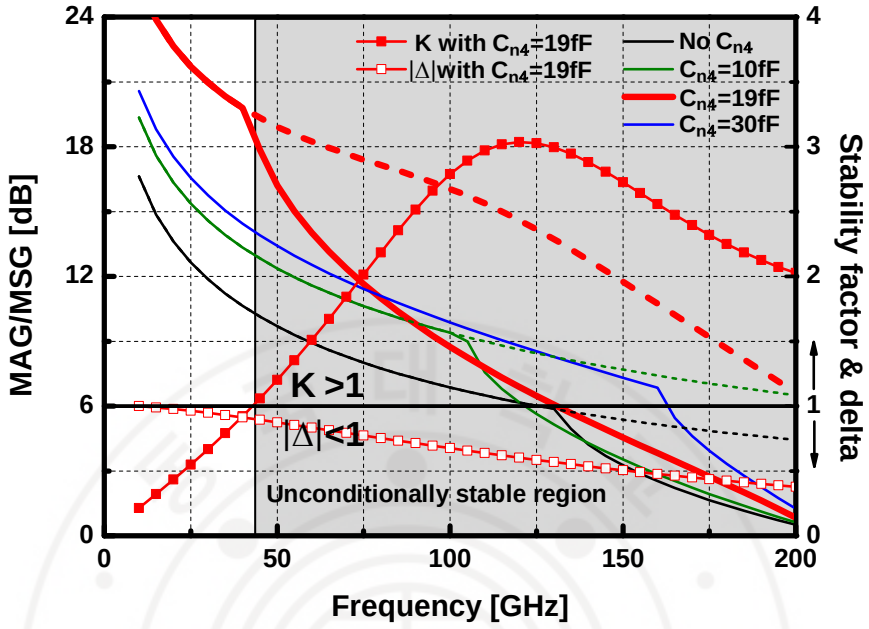


Figure 3.2-4 Simulated MSG (dashed lines)/MAG (solid lines) of the power stage differential pair depending on the neutralization capacitor C_{n4} and K and |Δ| with C_{n4} = 19 fF.

Furthermore, when using cross-coupled neutralization, the MSG and MAG become significantly larger than what they are when the cross-coupled neutralization is used, which implies that C_{n4} is appropriate in this case. The gate width (W) of the transistors at first and second driver stage was $W_{1,2}$ = 32×0.8 μm. For the transistors at the third driver stage and final power stage, W_3 = 32×1 μm and W_4 = 48×1 μm were used, respectively. The neutralization capacitors were set by $C_{n1,2}$ = 12 fF, C_{n3} = 14.3 fF, and C_{n4} = 19 fF in each stage to obtain an optimal capacitive neutralization for a given device size.

3.3 Transformer-Based Matching Network

In order to identify the inductive coupling of the two windings of the transformer and the capacitive coupling, respectively, a modeling analysis of an on-chip transformer (TF) for a PA design in the CMOS technology is carried out, using six parameters (L_1, R_1, L_2, R_2, M, and R_f), as shown in Figure 3.3-1 [19–21]. The source and the load of the transformer model can be either the 50-Ω terminal, or the gate or the drain of transistors especially in interstage matching network design. The coupling coefficient and the quality factors are defined as below:

$$k = \frac{M}{\sqrt{L_1 L_2}}; \quad Q_1 = \frac{\omega L_1}{R_1 + R_f}; \quad Q_2 = \frac{\omega L_2}{R_2 + R_f} \tag{2.2-1}$$

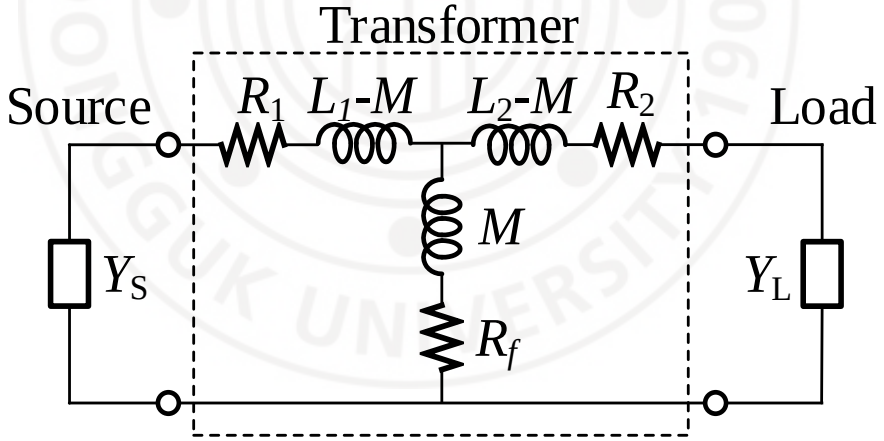


Figure 3.3-1 Six-parameter transformer model with general load and source

The optimum source ($Z_s = R_s + jX_s$) and load ($Z_L = R_L + jX_L$) for a given transformer are given in [20], and they are written in terms of admittances as:

$$B_s = \frac{1}{\omega L_1} \cdot \frac{Q_1^2}{1 + Q_1^2 + k^2 Q_1 Q_2}; G_s = \frac{1}{R_1} \cdot \frac{\sqrt{1 + k^2 Q_1 Q_2}}{1 + Q_1^2 + k^2 Q_1 Q_2} \quad (2.2\text{-}1)$$

$$B_L = \frac{1}{\omega L_2} \cdot \frac{Q_2^2}{1 + Q_2^2 + k^2 Q_1 Q_2}; G_L = \frac{1}{R_2} \cdot \frac{\sqrt{1 + k^2 Q_1 Q_2}}{1 + Q_2^2 + k^2 Q_1 Q_2} \quad (2.2\text{-}1)$$

where $Y_S = jB_S + G_S$ is the source admittance and $Y_L = jB_L + G_L$ is the load admittance of the transformer.

The conductance and susceptance of the source and load can be transferred into the forms of parallel resistance (R_p) and reactance (X_p) as below:

$$R_{sp} = \frac{1}{G_s}. \; X_{sp} = \frac{1}{B_s}. \; R_{Lp} = \frac{1}{G_L}. \; X_{Lp} = \frac{1}{B_L} \quad (2.2\text{-}1)$$

For an on-chip transformer in the CMOS process, the five-parameter model with $R_f = 0$, can properly model the electrical behavior of a winding transformer up to around 70% of its SRF with 10% of precise tolerance [21]. There is a noteworthy aspect here in that the intrinsic insertion loss of a TF is reduced monotonically for $k^2Q_1Q_2$.

In designing the interstage matching networks, transformers with a center tap were employed to bias and supply the transistors and named TF1, TF2, and TF3, as illustrated in Figure 3.1-1. Considering the device size and neutralization capacitors of each unit cell amplifier, interstage matching networks are designed using the lumped components model of the transformer, presented in Figure 3.3-1. Each interstage transformer has a turns ratio of 1:1, and the transformers operate below

the self-resonance frequency (SRF) to ensure the validity of the lumped component model. The diameters of TF1, TF2, and TF3 are 39 um, 37um and 26 um, respectively. In the case of TF3 at the input of the final stage, additional series inductors were applied to resonate out the drain-source capacitance. The 3-D structures of the interstage matching networks TF1, TF2 and TF3 including additional inductance L_{d3} are depicted in Figure 3.3-2.

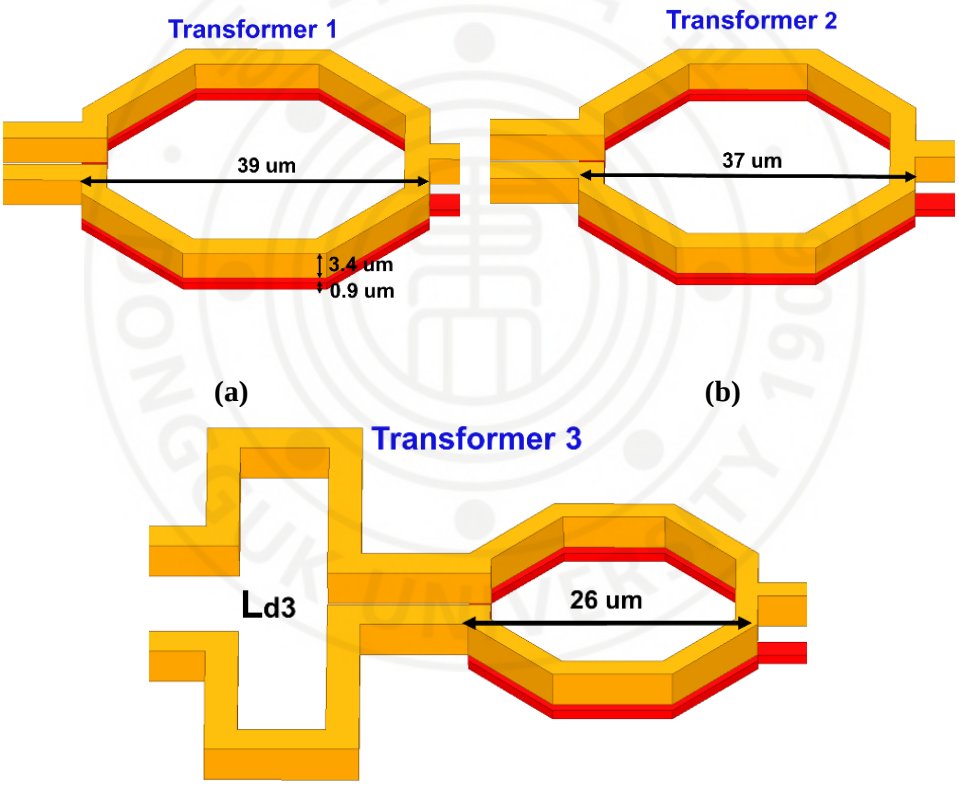


Figure 3.3-2 Structures of interstage matching networks (a) TF, (b) TF2 (c) T iF3

Figure 3.3-3 presents the trace at each interstage by using the lumped components model. Considering that the size of M1 is equal to M2, the conjugate admittance of the source is also plotted at the same point. The impedance for the lumped model is in good agreement with the 3-D EM simulated results presented in Figure 3.3-3

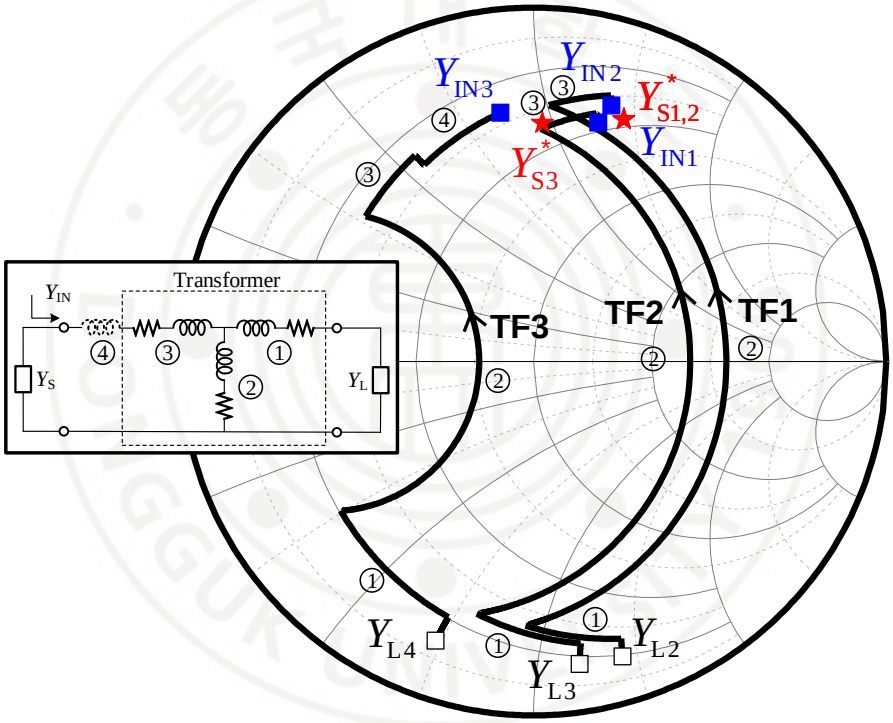


Figure 3.3-3 Admittance derived from 3D EM simulation results (blue squares) and from the modeled lumped components (black solid lines) and conjugate source admittance (red stars) of the TF1, TF2, and TF3 at each interstage in the 4-way PA.

3.4 Transformer-Based Parallel Combiner

In employing the transformer-based combiner, the ultra-thick metal (UTM) with the thickness of 3.4 μm is used for the primary coil to minimize the voltage drop in the path of VDD, while Metal 8 is used for the secondary coil. Also, the input impedance seen at each differential port of the primary coils is well balanced even while the secondary coil is a single-ended structure connected to the ground. The 3D EM model of the input divider and output combiner is described in Figure 3.4-1(a) and (b), respectively. All the simulations of the passive components were performed with Ansoft HFSS. The diameter of the divider and the outside coils of the combiner are 52 μm and 46 μm, respectively. For the transformer-based divider in Figure 3.4-1(a), the primary coils have a larger self-inductance compared to the secondary coil as the diameter of the secondary coil is 39 μm. In order to increase the coupling factor k for the transformer, broadside-coupled coil on the M8 layer are implemented, which has a smaller minimum spacing rule than the UTM layer. The simulated insertion losses of the combiner and the divider are shown in Figure 3.4-2(a). In implementing the output parallel combiner for each 4-way push-pull PA, vertical-coupled transformers were used to combine output signals at the coils. It is advantageous to combine signals with low insertion loss using this on-chip vertical-coupled structure, as it can achieve a very small distance between primary and secondary coils. Due to the symmetry in the layout, the parallel combiner with the current mode is highly balanced. To verify the electrical symmetry of the

transformer-based combiner and divider, the amplitude and the phase imbalance of each component are simulated, which shows almost 0 dB and below 1-degree imbalance below 140 GHz, as presented in Figure 3.4-2(b). The small amplitude and phase imbalances are caused by the paths for cross-coupled capacitors in different layers.

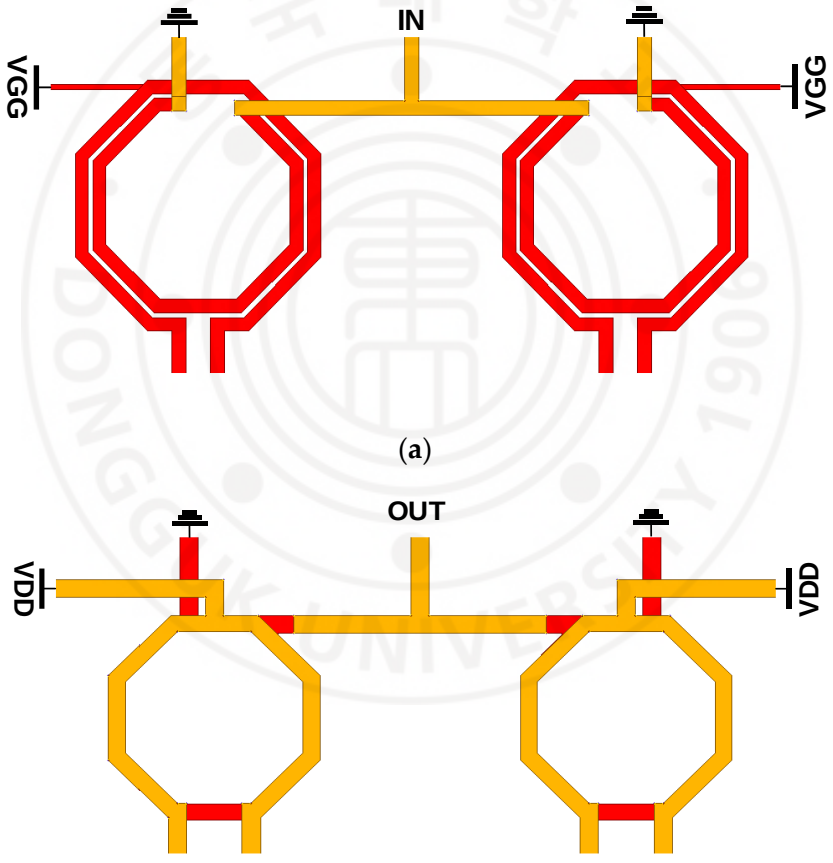
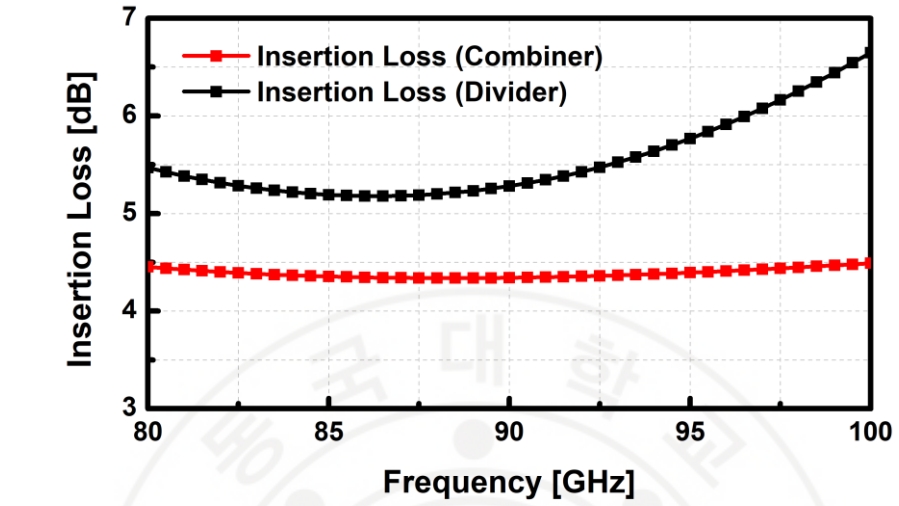
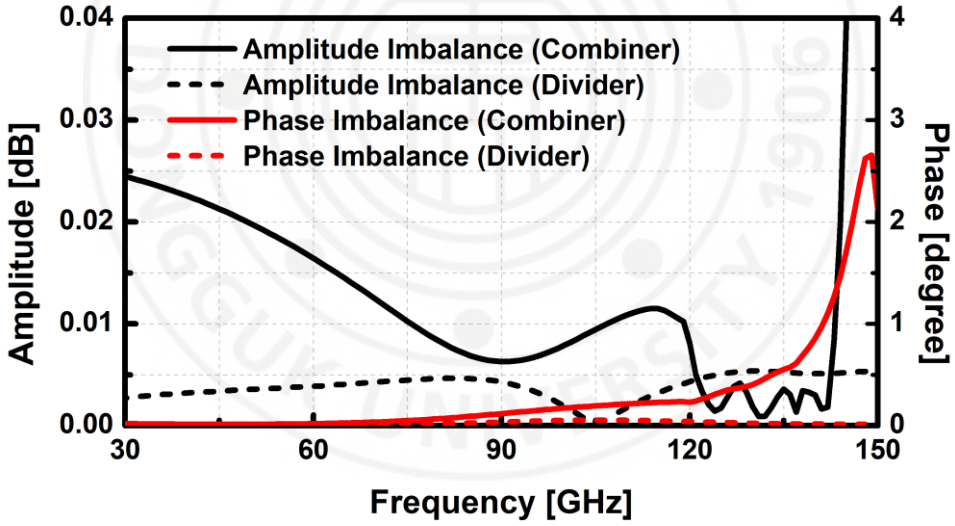


Figure 3.4-1 Structure of (a) the divider and (b) the combiner at the input and output of the 4-way PA.



(**a**)

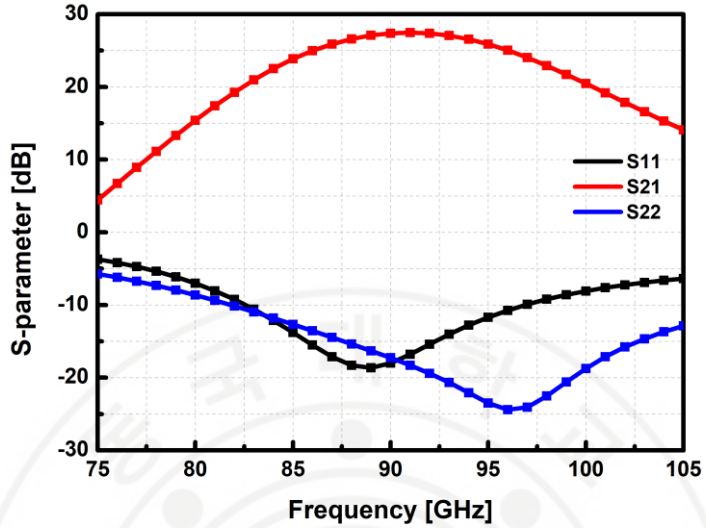


(**b**)

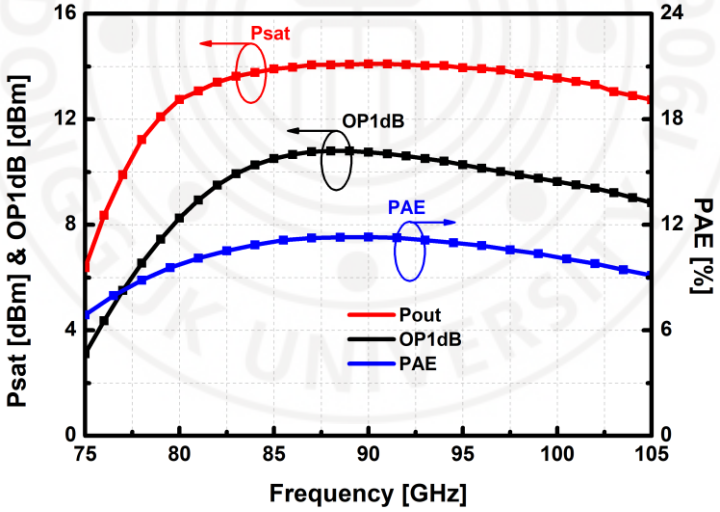
Figure 3.4-2 Simulated (a) insertion loss and (b) amplitude and phase imbalance of the divider and the combiner in the 4-way PAs.

3.5 Simulation Results

The output power matching has been performed using the Load-pull analysis with Harmonic Balanced (HB) simulation. Differential optimum impedance $Z_{opt1diff}$ and $Z_{opt2diff}$ of the power stage are derived using load-pull simulations, and each input impedance at differential ports of the output matching network combiner is matched to $Z_{opt1diff}$ and $Z_{opt2diff}$. The simulated S-parameters of the designed 4-way PA are shown in Figure 3.5-1(a). The 4-way PA achieves a peak gain of 27.5 dB at 91 GHz with a 3-dB gain bandwidth of 11 GHz (85.5–96.5 GHz). Within the 3-dB gain bandwidth, input and output return losses are greater than 10 dB. Also, the large-signal results of the 4-way PA were simulated. The simulated output power and the 1-dB compressed output power (OP_{1dB}) are 14.2 dBm and 10.8 dBm at 90 GHz, respectively. The maximum power efficiency of the 4-way PA is simulated to be 11% at 90 GHz. For the simulation of the 4-way PA, the source and load impedance of 35 Ω are placed, which is a designed characteristic impedance of the transmission line in the Lange coupler. The simulation and layout of the designed PA were performed with Cadence Virtuoso. Figure 3.5-1(b) shows simulated results of the large-signal performance versus frequency.



(a)



(b)

Figure 3.5-1 4-way PA's simulation results of (a) S-parameters and (b) large signals.

Chapter 4 90 GHz 8-Way Balanced Power Amplifier

4.1 W-Band Microstrip Lange Coupler

The advantage of utilizing a balanced power amplifier configuration is its wideband matching at input and output. In addition, it provides wide ranges of stability since the reflected power from impedance mismatches is dissipated in the 35 Ω which is used to combine the output power from each 4-way PA. It is noteworthy that the size of the Lange coupler becomes comparable to that of the coupler's termination of the isolation port at the coupler. By utilizing the balanced structure, the flatness can also be enhanced as the unbalanced output power from the mismatches of the two 4-way PAs must be dissipated in the termination as well [22]. Considering this feature, a balanced PA is ideal for a high-precision FMCW radar sensor.

To achieve the balanced architecture with an improved P_{sat} for a wideband operation, the Lange couplers with lumped components at W-band. Furthermore, at 90 GHz, the transmission-line-based couplers exhibit a lower insertion loss than their counterparts. The UTM layer is used as a coupled line in the designed Lange coupler to mitigate the insertion loss (IL).

In order to build a Microstrip-line, the M1 and M2 layers were stacked together with vias to form a solid ground plane, while the UTM layer (ultra-thick metal layer) served as a signal line. According to Figure 4.1-1 (a), the Lange coupler's bridges

were formed with the M8 layer. The length of the coupled lines is $\lambda g/4 \approx 450$ μm for 90 GHz. It has to be noted that the characteristic impedance was chosen to be 35 Ω considering the limited minimum width of the UTM layer in implementing the coupled line of the Lange coupler.

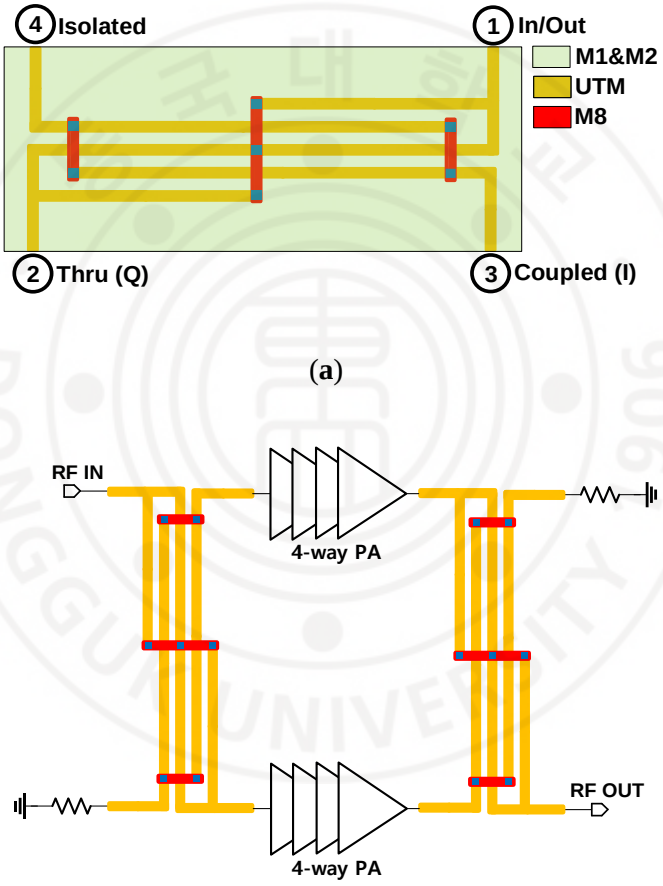
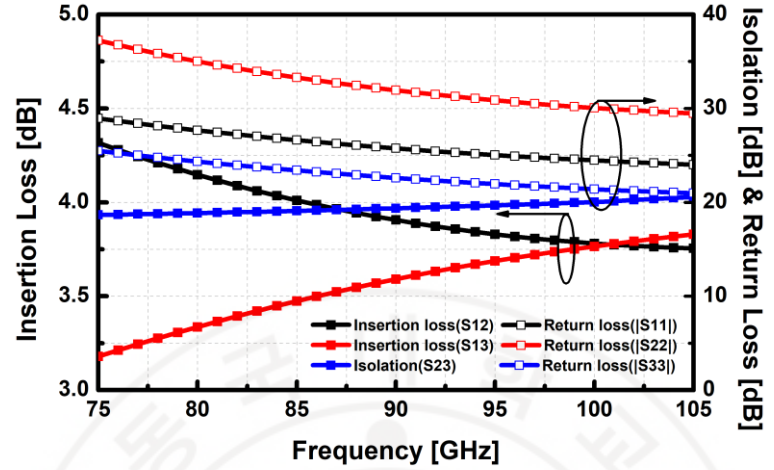
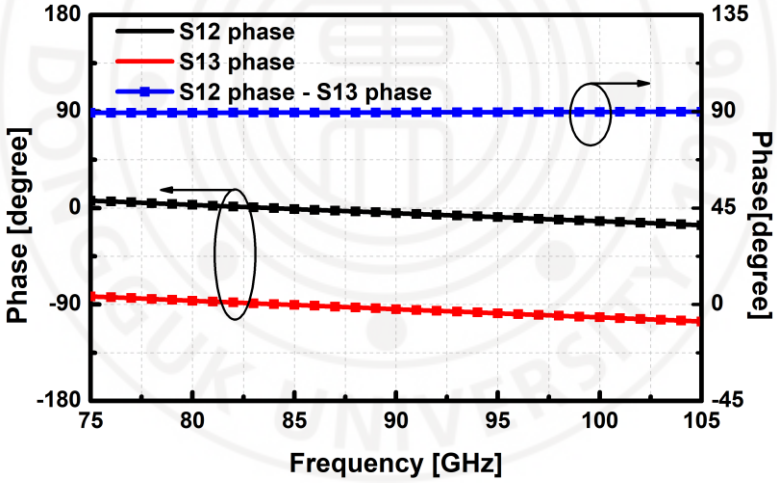


Figure 4.1-1 (a) Structure of the on-chip Lange coupler and (b) block diagram of the balanced 8-way PA with the Lange coupler.

The PA's input and output VSWRs are highly dependent on the functions of the Lange coupler, but the return loss (RL) from the mismatch between 35 Ω and 50 Ω loads is still good enough (RL ≈ 19 dB). As a result, the load impedance of the 4-way PA was also designed to be 35 Ω. The Microstrip-line also features a reference impedance of 35 Ω that allows more current to flow [10]. As illustrated in Figure 4.1-1 (b), the implemented 8-way PA forms a balanced structure with two 4-way four-stage push-pull PAs utilizing the input and output Lange couplers with its high coupling feature, owing to the multiple fingers. The 4-way PAs were implemented with two transformer-based push-pull PAs using transformer-based combiners and dividers, as presented in Figure 3.1-1. The simulated magnitude and phase of the S-parameters for the designed Lange coupler are shown in Figure 4.1-2 (a) and (b). Due to relatively long supply lines, transistors in two internal paths are placed away from DC pads, and this increases common-mode inductance. In this coupler, bypass capacitors were placed not only around DC pads, but also between two quadrature paths.



(**a**)



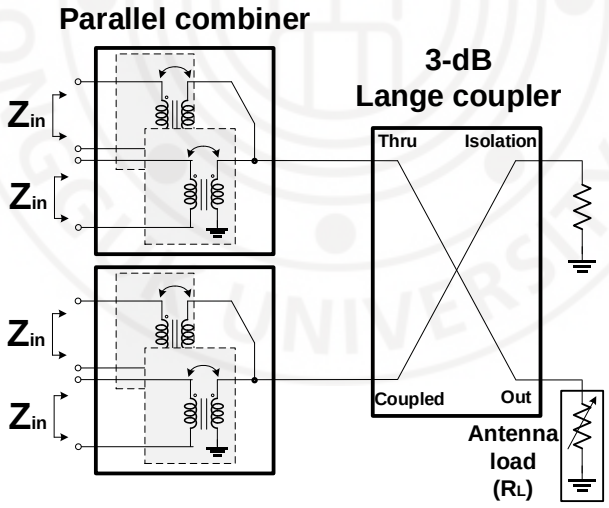
(**b**)

Figure 4.1-2 Simulation results of the (a) insertion loss, isolation and (b) phase response for the designed Lange coupler.

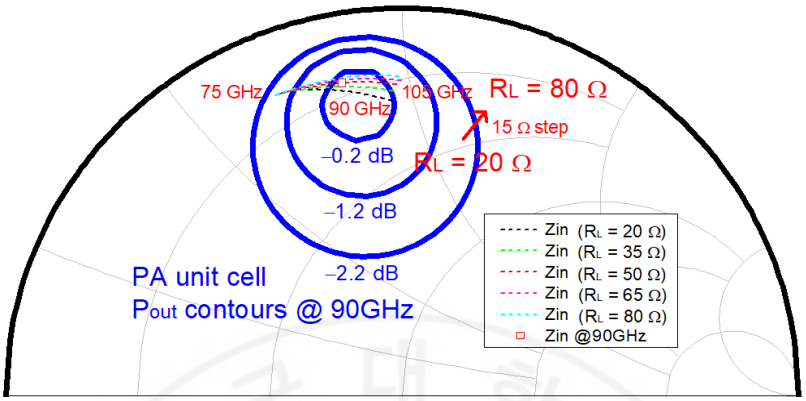
4.2 Robustness to Load Variation

In this design, the extracted differential optimum load impedance $Z_{optdiff}$ = 11.3

+ j43 Ω at 90 GHz is matched from a 50 Ω load. Although, the load impedance cannot be exactly 50 Ω, in practice, because the antenna at the output must be connected to the PA, resulting in load variations. In order to ensure robustness to load variations, the impedance of the load R_L was varied from 20 to 80 Ω (±60% variations) during simulation. The output power, output return loss, and input impedance of the transformer-based combiner preceding the Lange coupler were then measured. The output matching network and unintentionally variable antenna load are shown in Figure 4.2-1 (a). Due to the balanced structure of the PA designed as shown in Figure 4.2-1 (b), the load impedance does not affect much the input impedance of the output matching network.



(**a**)



(**b**)

Figure 4.2-1 (a) Configuration of output matching network and (b) Power contours and the input impedance seen at each device with the load variations from 20 to 80 Ω at 90 GHz.

The arrows in Figure 4.2-2 indicate the improved output return loss (RL) of the 8-way PA in comparison to the 4-way PA. However, the output return loss of the 8-way PA with an 80 Ω load achieved the output RL better than the acceptable value (>8 dB) in the operating frequency between 75 and 105 GHz; the S22 of the 4-way PA was distinctively shifted depending on the load variations, which resulted in 5 dB of the output return loss in the operating band. In the condition of the load variations, the PA achieved the minimum P_{sat} of 15.7 dBm with the 80 Ω load and the maximum P_{sat} of 16.2 dBm with the 50 Ω load at 90 GHz. Thus, the simulated output power results show that the Lange coupler compensates for the load variations, which effectively mitigates the performance degradations of the PA from the load variations.

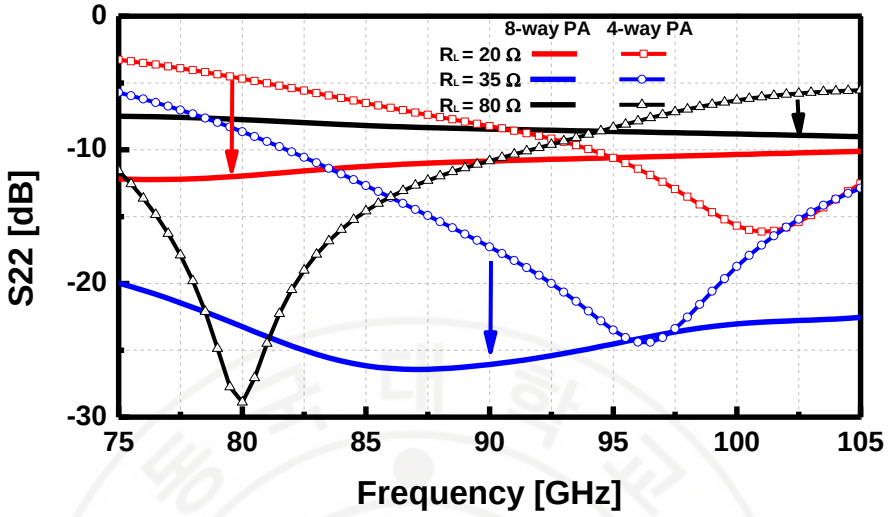


Figure 4.2-2 Simulation results of the output return loss of the 8-way PA (solid line) and 4-way PA (line with symbol) with the load variations.

4.3 Measurement Results

This PA is implemented on a chip having the dimensions of 0.94 × 0.8 mm^2, which includes RF pads and DC pads. Without RF pads and DC pads, the size of the core area is 0.62 × 0.62 mm^2. As shown in Figure 4.3-1, the chip photograph of PA is presented. In order to conduct the measurement of S-parameters of the implemented balanced PA, a vector network analyzer N5224A (Keysight, CA, United States) combined with an extension module (75–110 GHz) was used with an on-wafer probe station, and on-wafer setup was calibrated with a CS-5 calibration kit.

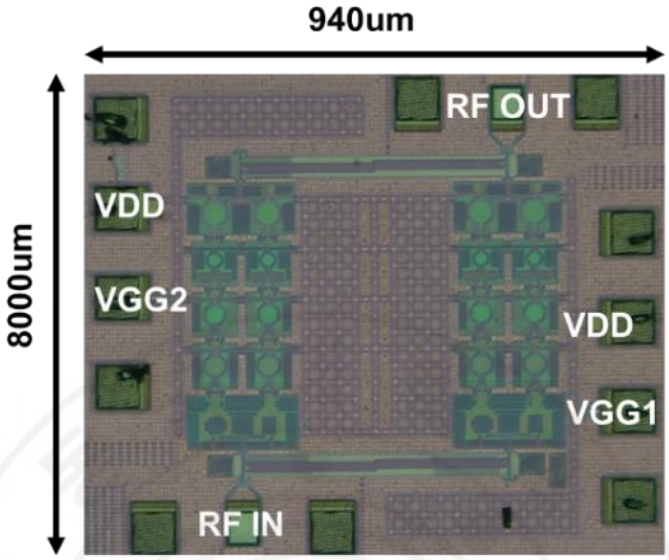
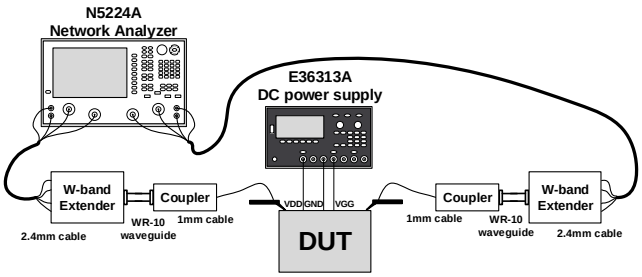
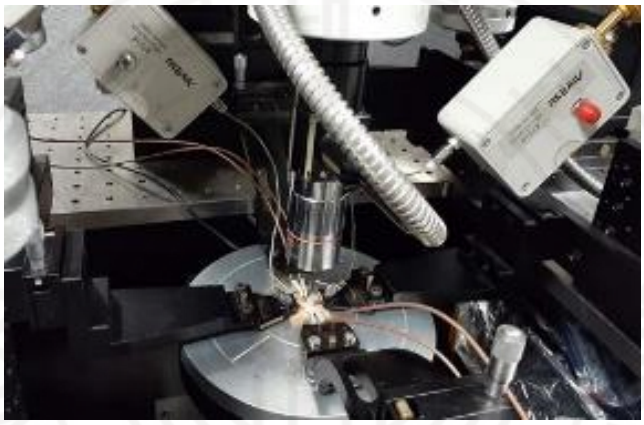


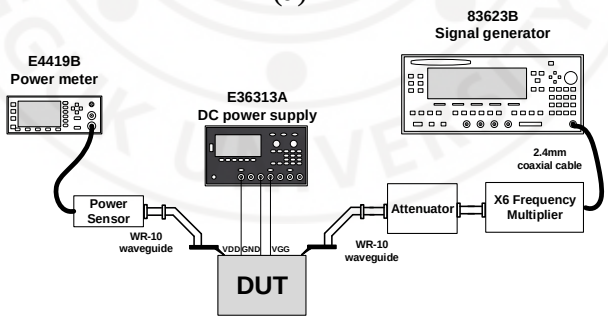
Figure 4.3-1 Chip photograph with the size of 0.94 mm × 0.8 mm including RF pads and DC pads.

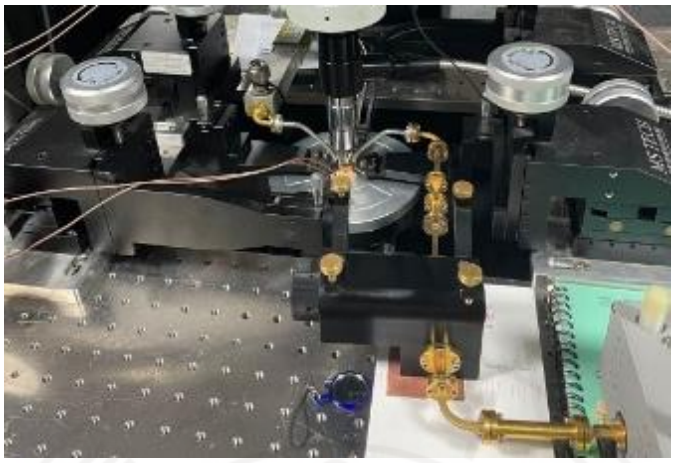
The implemented PA consumes a DC-current of 370 mA from a 1.2-V supply. In measuring the large-signal performance, the W-band input signal was generated using a ×6 frequency multiplier and an X-band signal generator 83623B (Agilent, CA, United States), A W-band attenuator QAD-W00000 (Quinstar, CA, United States) was placed at the output of the frequency multiplier to control the input power. The output power of the PA was measured using a power meter E4419B (Agilent, CA, United States) and a W-band power sensor W8486A (Agilent, CA, United States). The setup for the S-parameters and the large-signal measurement at W-band are illustrated in Figure 4.3-2 (a) and (b), respectively.


N5224A
Network Analyzer
E36313A
DC power supply
W-band
Extender
Coupler
1mm cable
WR-10
waveguide
2.4mm cable
VDD GND VGG
DUT
Coupler
1mm cable
WR-10
waveguide
W-band
Extender
2.4mm cable



(**a**)


83623B
Signal generator
E4419B
Power meter
E36313A
DC power supply
2.4mm
coaxial cable
Power
Sensor
WR-10
waveguide
VDD GND VGG
DUT
WR-10
waveguide
Attenuator
X6 Frequency
Multiplier



(**b**)

Figure 4.3-2 Setup for the proposed W-band PA measurements of (a) S-parameters and (b) the large-signal performance.

The measured S-parameters of the balanced PA are presented in Figure 4.3-3. The peak gain improvement of 27.4 dB was observed at 86.4 GHz, and the 3 dB gain bandwidth of the balanced PA was measured to be 13 GHz (83–96 GHz). Due to the broadband characteristic of the employed Lange coupler, the input and output return loss are above 10 dB from 75 GHz to 105 GHz, except for around 97 GHz. Figure 4.3-4 (a) and (b) show results of the large-signal measurement over the frequency and input power, respectively. The implemented PA achieved the peak P_{sat} of 16.5 dBm, OP_{1dB} of 13.3 dBm, and PAE was 9.9% at 90 GHz. Over the 3-dB gain bandwidth, the designed balanced 8-way PA achieves P_{sat} higher than at least 14.9 dBm, where the maximum variation of 1.6 dB is observed. To demonstrate the output power flatness, which is advantageous for the application of PA in high-precision FMCW radars, the 1-dB power bandwidth ($P_{sat}BW_{-1dB}$) and 3-dB power bandwidth

($P_{sat}tBW_{-3dB}$) were evaluated from the measurement results, as shown in Figure 4.3-4. $P_{sat}tBW_{-1dB}$ is 13.8 GHz (81.6–95.4 GHz), and $P_{sat}BW_{-3dB}$ is 20.4 GHz (79.2–99.6 GHz). Both $P_{sat}tBW_{-1dB}$ and $P_{sat}BW_{-3dB}$ were degraded from evaluated values in simulation due to the low P_{sat} above 94 GHz in the measurement and yet the balanced PA achieved a wide power bandwidth representing the availability of high-precision FMCW radars.

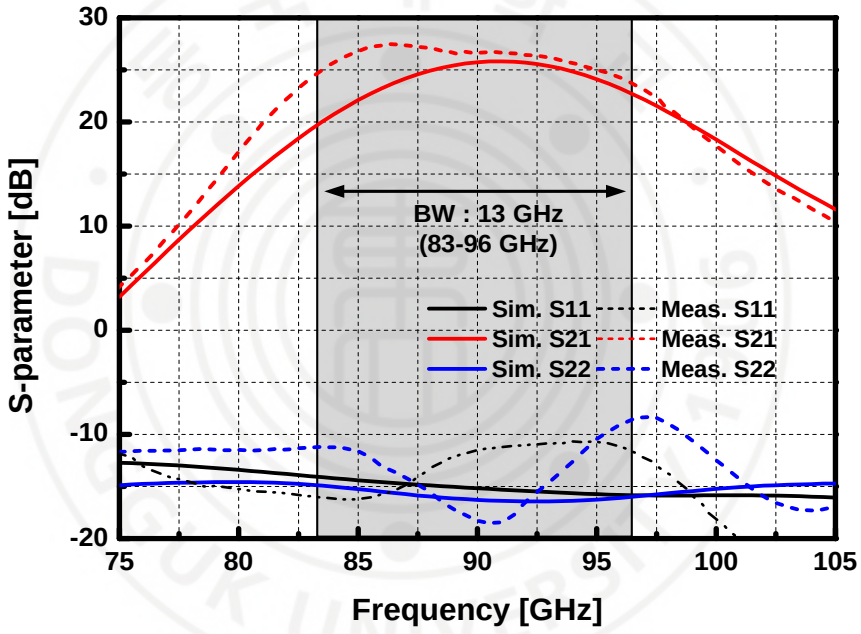


Figure 4.3-3 Measurement and simulation results of S-parameter of the W-band 8-way PA with a 50 Ω load.

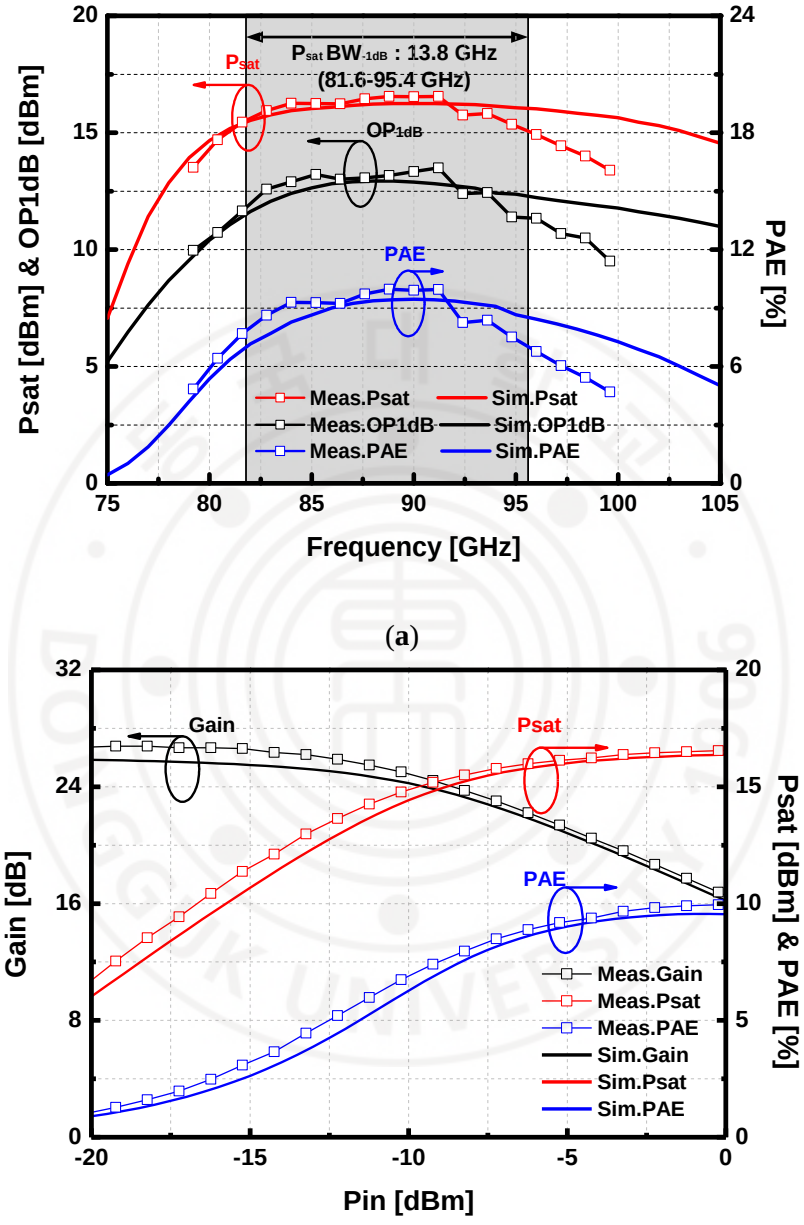


Figure 4.3-4 Large-signal simulation and measurement results of the W-band 8-way PA versus (a) frequency (b) input power at the center frequency (90 GHz).

Table 4.3-1 summarizes the performance of the implemented PA in this work and other recently reported W-band CMOS PAs. Both PAs in [9,10] utilized transmission-line (T-line)-based combiners. The PA in [9] achieved a 38 GHz of OP_{1dB} bandwidth, and the 16-way PA in [10] performed the highest output power among W-band PAs. Though, it is noticed that the PAs with direct T-line combiner had relatively lower PAE due to the high loss of the output matching network. Works in [13–15,23] utilized compact transformer-based combiners, and they achieved the saturated output power higher than 14 dBm with small area occupancy. However, with this configuration, $P_{sat}BW_{-1dB}$ is comparatively lower than other reported PAs. Meanwhile, our proposed balanced PA features better 1-dB and 3-dB power bandwidth by effectively combining two transformer-based push-pull PAs with Lange couplers. The presented 8-way PA attains the highest FoM and FoM_{BW} among the recently reported CMOS PAs operating above 90 GHz to date.

Table 4.3-1 Comparison table of CMOS power amplifiers.

	This	**[9]**	**[10]**	**[13]**	**[14]**	**[15]**	**[23]**	**[24]**
Freq (GHz)	83–96 @90	77–110 @87	75–100 @90	85–100 @94	101–117 @109	100–117 @109	73–89 @81	75–90 @80
VDD (V)	1.2	1.2	1.2	1.8	2/1.2	1.2	2.5	2
Gain (dB)	26.7	18	12.5	13	14.1	20.3	16.1	11
P_{sat} (dBm)	16.5	14	18	14	14.8	15.2	18	12.4
$P_{sat}BW_{-1dB}$ (GHz)	13.8	38 † (OP_{1dB})	12	>11 ‡	>7 ‡	>9 ‡	N/A	>7 ‡ (OP_{1dB})
$P_{sat}BW_{-3dB}$ (GHz)	20.4	N/A	N/A	15	>10 ‡	>16 ‡	N/A	>10 ‡ (OP_{1dB})
OP_{1dB} (dBm)	13.3	12	17.5	10.3	11.6	12.5	12.9	12
PAE (%)	9.9	4.5	9	4	9.4	10.3	12.6	14.2
Way	8	4	16	4	4	4	4	1
Size (mm^2)	0.752	0.57	0.82	0.24	0.322	0.343	0.21 (core)	0.321
FoM *	92.2	77.3	79.1	72.5	79.4	86.4	83.2	73.0
FoM_{BW} **	2420.0	204.8	237.2	28.3	127.3	677.2	419.7	37.3
Topology	4 stage CS + BA	6 stage CS	3 stage CS	3 stage CC	2 stage CC + 1 stage CS	4 stage CS	2 stage CC	2 stage CC
Process	65 nm	65 nm	65 nm	65 nm	65 nm	65 nm	55 nm	45 nm SOI

† Simulated result.

‡ Graphically estimated from measurements.

* FoM = P_{sat}[dBm] + Gain[dB] + 10log(PAE[%] × f_c^2[GHz]).

** FoM_{BW} = P_{sat}[W] × Gain × PAE[%] × f_c^2[GHz] × BW_{gain}[%] [25].

CS: Common source, CC: Cascode, BA: Balanced amplifier.

Chapter 5 Conclusions

This thesis demonstrated a W-band balanced power amplifier (PA) that attains 20.4-GHz 3-dB power bandwidth, +16.5 dBm peak saturated output power (P_{sat}) and 9.9% of the peak power added efficiency (PAE) in 65nm CMOS technology. By combining two push-pull PAs in the current mode, each transformer-based 4-way PA was designed at 90 GHz. For wideband operation, on-chip Lange couplers were utilized as balancing hybrids to combine the two transformer-based 4-way PAs. The implemented 8-way PA demonstrated wideband operation, capable of being used for high-precision FMCW radars with the highest FoM of the recently published CMOS PAs at 90 GHz.

For the future works, the proposed 90 GHz broadband PA can be implemented in a front-end transceiver for the application of high-precision FMCW radars. Thus, the performance of high-precision W-band FMCW radars can be demonstrated. Moreover, the presented PA could be applied to 6G communication system which also needs high output power over wide bandwidth.

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국문 초록

본 학위 논문은 65 nm CMOS 기술 기반의 고정확도 주파수 변조 연속파(FMCW) 레이더용 W-대역 8방향 광대역전력증폭기 (PA)를 제안한다. FMCW 레이더 센서의 높은 범위 해상도와 장거리 탐지 범위를 위해 향상된 출력 전력으로 광대역 동작을 실현하는 평형 구조는 2개의 4방향 push-pull PA로부터의 출력 전력을 결합하는 Lange 커플러로 구현되었다. 4방향 PA의 게이트-드레인 캐패시턴스는 cross-coupled capacitive neutralization 기술과 함께 변압기 기반의 push-pull 구조를 이용하여 향상된 전력 이득으로 안정성을 위해 보상되었다. 정합 네트워크의 손실을 줄이고 크기를 최소화하기 위해 변압기를 사용하여 단간 정합이 이루어졌다. 또한, 안테나 부하 임피던스는 기준 임피던스인 50 Ω에서 변할 수 있기 때문에, 전력 증폭기의 부하 부정합에 따른 견고성을 반사 손실과 출력 전력의 관점에서 해석하였다. 구현된 8방향 평형전력증폭기는 90 GHz에서 16.5 dBm의 포화출력전력(P_{sat}), 13.3 dBm의 1dB 압축출력전력(OP_{1dB}), 9.9%의 전력부가효율(PAE) 특성을 갖는다. 광대역 특성을 설명하기 위한 3dB 이득대역폭, 1dB 및 3dB 출력전력대역폭은 각각 13 GHz (83~96 GHz), 13.8 GHz (81.6~95.4 GHz) 및 20.4 GHz (79.2~99.6 GHz)로 측정되었다.