Master's Thesis

Implementation Study of a Low-Loss X-Band System-in-Package (SiP)

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ABSTRACT

Despite continuous advancements in integrated circuit (IC) technology, the miniaturization of transistors has reached its limitations, leading to challenges such as interconnect delays and high power consumption. To overcome these limitations, advanced packaging technologies that go beyond conventional semiconductor processes have emerged as a critical solution. In particular, optimizing wire-bonding and via structures within the package is essential for effectively reducing insertion loss and inductance.

In the field of high frequency (RF) circuits, especially in the X-band(8-12GHz), maximizing signal transmission performance requires more precise simulation and measurement techniques for package design. A differentiated approach from conventional advanced packaging technologies is necessary, with an emphasis on structural optimized to the specific characteristics of RF packages.

This thesis studies the performance enhancement of X-band RF packages through meticulous simulation and modeling of System-in-Package (SiP) structures. To this aim, 3D electromagnetic (EM) simulations were conducted to analyze insertion loss and inductance with high precision. The simulation results were then compared with

measurements, leading to the development of a more accurate modeling technique. Additionally, a calibration method was applied to minimize discrepancies between experimental data and simulation results, ensuring the reliability of the proposed model.

While System-in-Package (SiP) technology provides an effective approach for integrating heterogeneous semiconductor chips within a single module, the choice of packaging type is also critical for ensuring signal integrity and system performance in high frequency environments. Among various packaging methods, Land-Grid-Array (LGA) package has gained attention as an ideal solution for RF circuits due to its structural advantages, including low parasitic inductance, short interconnection lengths, and high I/O density. In particular, LGA package facilitates channel to channel path symmetry and delay matching, making it highly advantageous for maintaining phase and attenuation alignment in multi-channel transceiver systems. In this study, a highly integrated LGA package structure incorporating a 4-channel Multi-functional Chip (MFC) fabricated using TSMC's 65nm CMOS process was designed to enhance RF performance in the X-band. By optimizing routing lengths and interlayer configurations, the proposed package minimizes variations in insertion loss, inductance, and group delay among channels,

thereby enabling the phase and attenuation alignment required for high frequency systems.

To ensure signal integrity at the package level, 3D electromagnetic (EM) simulations were conducted, and a high precision modeling methodology was established by comparing simulation results with experimental measurements. Furthermore, a calibration technique was applied to minimize discrepancies between simulation and measurement data, enhancing the reliability of the proposed model.

The modeling and optimization techniques presented in this study are expected to be applicable not only to the X-band but also to a broader frequency range in RF package design, which may contribute to the performance enhancement and commercialization of next generation high frequency semiconductor packaging technologies.

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Chapter I. Introduction

1.1 Research Background

System-in-Package (SiP) technology integrates multiple heterogeneous semiconductor chips within a single package, enabling miniaturization, high integration, and functional diversity. SiP has been widely adopted in various applications, including high frequency RF systems, mobile devices, and IoT platforms, due to its ability to combine different process technologies within a single module [1]. However, in such high frequency environments, maintaining signal integrity remains a critical challenge, with issues such as insertion loss, inductance, and parasitic coupling requiring careful consideration. In parallel, this study also explores Land-Grid-Array (LGA) package as a separate research focus. LGA packages offer short interconnection lengths, low parasitic inductance, and high I/O density, making them highly suitable for high frequency RF systems. They are particularly advantageous for multi-channel transceiver systems, where maintaining path symmetry and delay matching across channels is essential [2]. In this research, a 4-channel Multi-functional Chip (MFC) fabricated using TSMC's 65nm CMOS process was integrated into LGA package, and its performance was optimized

through 3D EM simulations and experimental validation, effectively minimizing variations in insertion loss, inductance, and group delay across channels. In addition to SiP and LGA, various other advanced packaging technologies are being actively developed.

Ball-Grid-Array (BGA) package is another widely used technology, particularly for applications requiring high pin counts and robust mechanical stability. BGA packages provide better heat dissipation and electrical performance compared to traditional leaded packages, making them suitable for processors, memory modules, and RF components. BGA packages can be classified based on the die to substrate bonding method, such as wire-bonded BGA and flip-chip BGA. Compared to wire-bonded BGA, Flip-Chip BGA enhances signal integrity and reduces parasitic inductance by flipping the die and connecting it directly to the substrate using solder bumps, which shortens the signal path and improves high frequency performance [3]. Figure 1.1-1 shows a cross-sectional vies of BGA package which is classified based on the die to substrate bonding method.

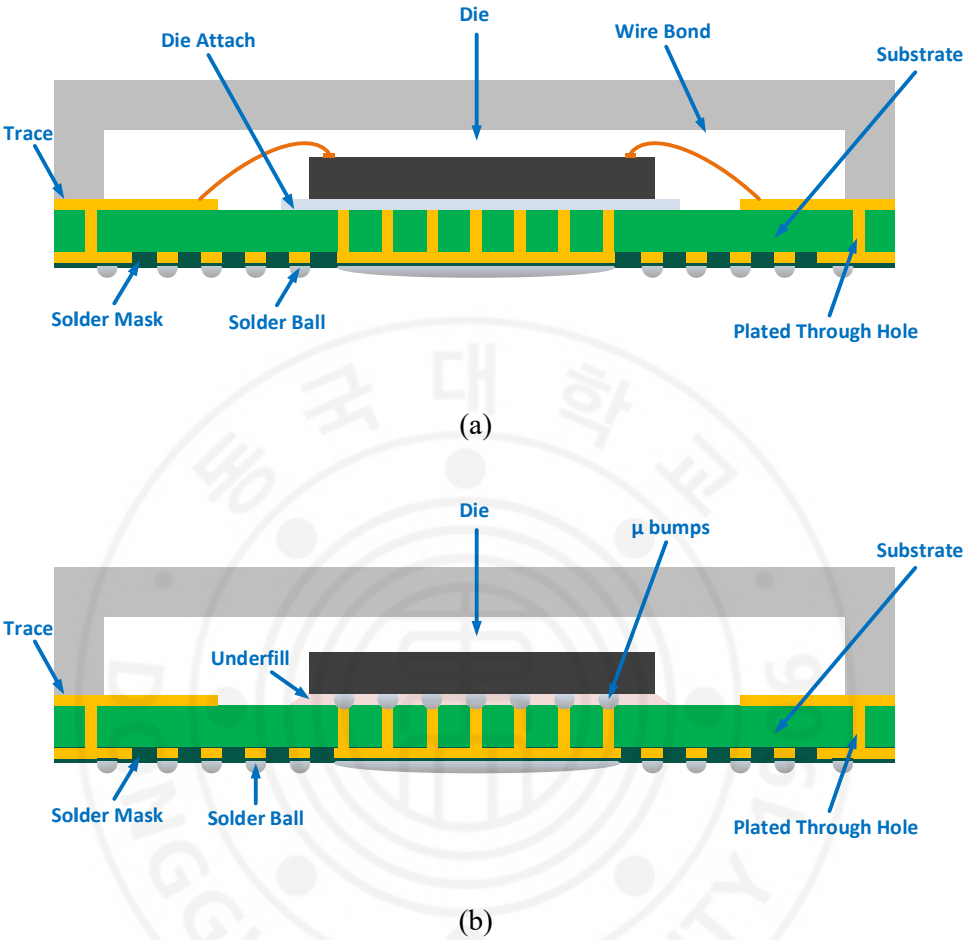


Figure 1.1-1 Cross-sectional view of BGA(Ball Grid Array) package ; (a) Wire-bonded BGA, (b) Flip-chip BGA

Recently, Wafer-Level Packaging (WLP) is classified into 2.5D and 3D packaging depending on the method of interconnection between chips. Figure 1.1-2 shows a Classification of Wafer-Level Packaging(WLP) [4]. In 2.5D packaging, chips are arranged horizontally, and the interconnections are established through

Redistribution Layer (RDL) and Through Silicon Via (TSV) within an interposer. Various types of interposers are used in this structure, including silicon interposers, organic dielectric based interposers, and glass based interposers. In contrast, 3D packaging stacks chips vertically, directly connecting them without the use of an interposer. Traditionally, μ bumps have been used for vertical interconnection, but more recently, Cu–Cu hybrid bonding has emerged as a promising alternative, offering lower contact resistance and higher alignment precision. 2.5D and 3D packaging stack or arrange chips on an interposer significantly improving bandwidth and reducing delay, which are critical for data centers and AI systems [5].

These advanced packaging technologies play a vital role in enhancing the performance, integration, and scalability of modern electronic systems. In this thesis, SiP and LGA package are each independently studied, focusing on structural optimization and performance enhancement for high frequency RF applications.

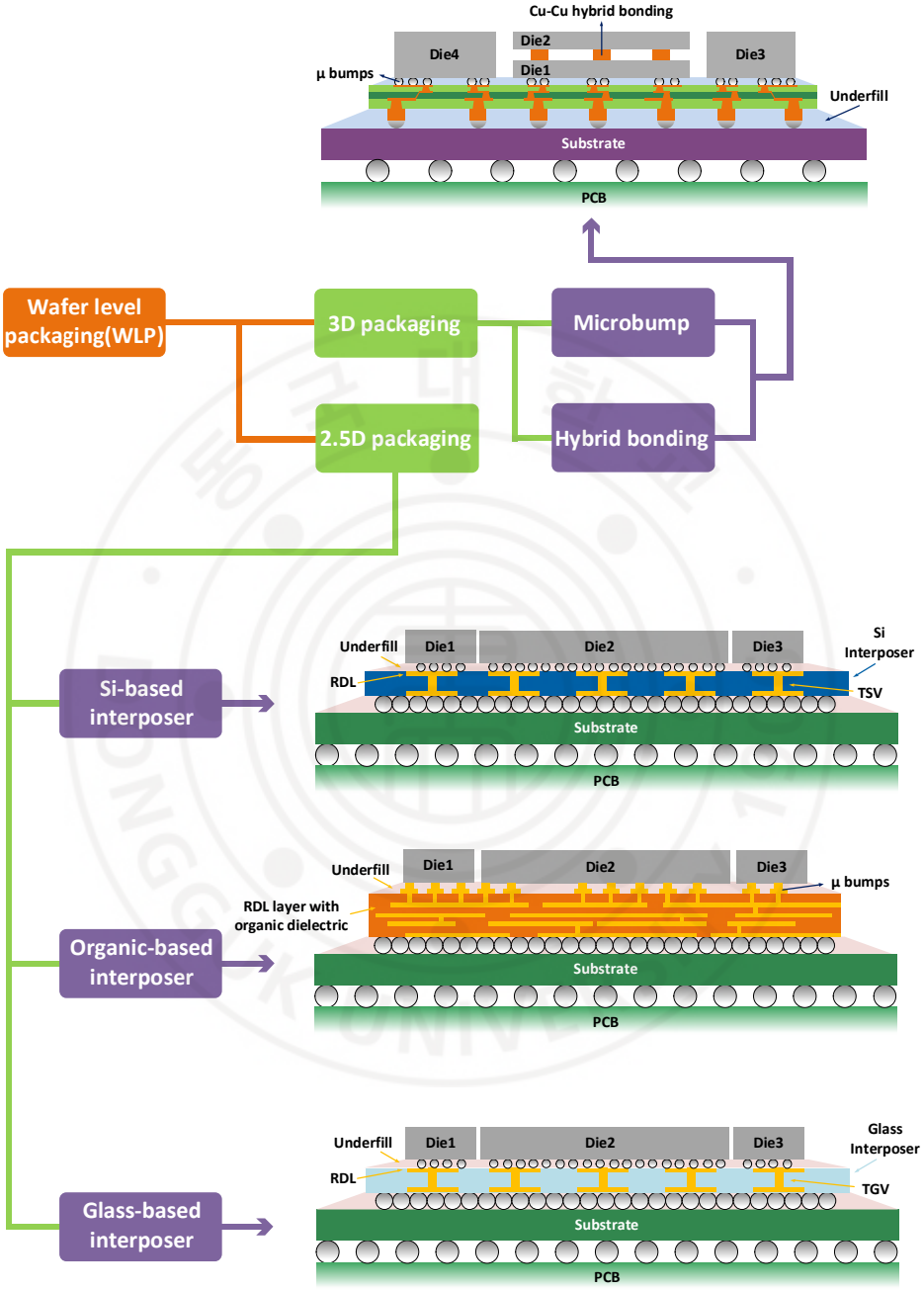


Figure 1.1-2 Classification of Wafer-Level Packaging(WLP)

1.2 Thesis Organization

In Chapter 2, the detailed implementation of the SiP QFN package structure is introduced. It explains the package level integration strategy, the composition of substrate, via, and bonding techniques, and discusses key structural elements such as the cavity substrate, wire bonding, and coaxial vias with emphasis on signal integrity. Additionally, methodologies for improving simulation accuracy, such as modeling surface roughness, SMA connectors, and applying realistic physical parameters to align simulations with measurements, are also covered in this chapter.

Chapter 3 compares simulation and measurement results. Both bare chip and integrated structures are analyzed, and the consistency between S-parameters, large-signal simulation results, and reliability assessments is evaluated.

Chapter 4 presents the design and optimization of the LGA package. It focuses on minimizing parasitic inductance, ensuring channel to channel path symmetry, and achieving delay matching for multi-channel RF systems. The performance of the proposed LGA design is evaluated through 3D EM simulations and experimental validation.

Chapter 5 concludes the thesis and suggests future research directions.

Chapter II. Design of X-band SiP QFN Package

2.1 QFN Package for X-band Transceiver

In general, System-in-Package (SiP) architectures offer greater design flexibility than System-on-Chip (SoC) in low frequency applications [6]. This is because multiple functional blocks implemented using different semiconductor processes can be integrated into a single package, thereby reducing development time and overall cost. The X-band transceiver proposed in this study also adopts a highly integrated single package structure, characterized by the integration of three heterogeneous semiconductor chips: a GaN based SPDT switch, high power amplifier, and a GaAs based low noise amplifier. Unlike SiP designs for low frequency applications, however, high frequency package design is more sensitive to parasitic effects, signal coupling, and insertion loss. For this reason, this study adopts the QFN (Quad Flat No Lead) package among various SiP packaging methods. QFN is a compact, flat type package without leads extending from its sides and features a structure in which the chip is directly bonded to the substrate. It was developed in the late 1990s in response to the growing demand for miniaturization and high integration. Thanks to its low profile,

excellent thermal dissipation, and low parasitic inductance, QFN has been increasingly used in various high frequency applications. Moreover, because of its short chip to substrate interconnect length and planar structure, QFN is well suited for maintaining low insertion loss even in high frequency bands [7].

2.1.1 Substrate Structure and Multi-Layer Configuration

In high density integration environment, it is physically impossible to implement RF signal lines, DC bias lines, and GND planes simultaneously using a single metal layer. Moreover, increased pattern density and signal coupling may lead to degradation in electromagnetic performance [8]. Therefore, multi-layer structure consisting of 4 metal layers was designed, with each layer clearly defined according to its electrical function.

2.1.1.1 Characteristics of Metal Layers

The bottommost layer, 'Metal 1', serves as the reference ground for the CPWG (Coplanar Waveguide with Ground) based RF signal lines implemented in the upper layers. This layer also functions as the soldering interface that connects the package to the external PCB, featuring an OSP (Organic Solderability Preservative) surface treatment. It provides a low impedance ground path while ensuring mechanical stability.

'Metal 1' is connected to the upper layers through vias, effectively forming the return current path. Figure 2.1-1 shows a 3D-EM model based on HFSS, designed using the structure of 'Metal 1', and is used to verify the current distribution and shielding effectiveness of the ground plane.

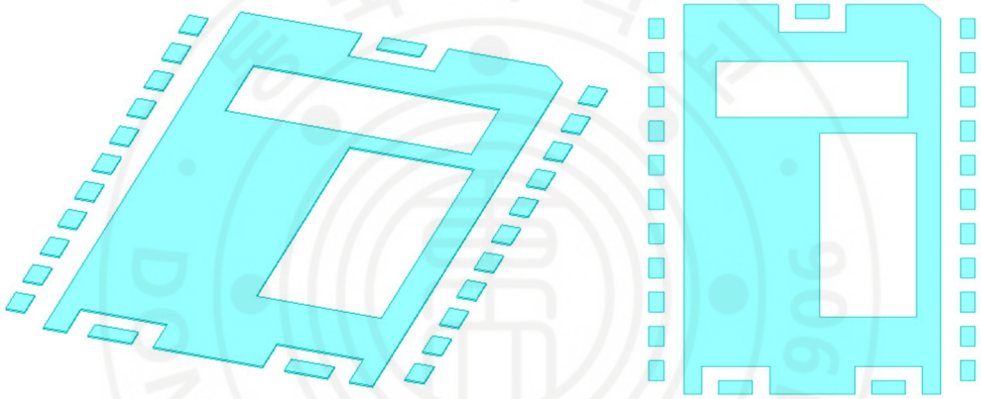


Figure 2.1-1 3D-EM Model Using HFSS ('Metal 1') ; (a) 3D view of 'Metal 1', (b) Top views of 'Metal 1'

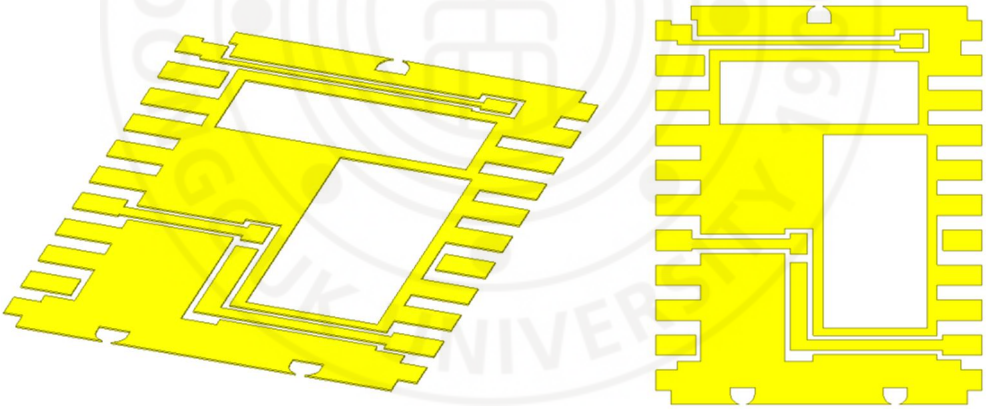
The two holes located at the center of the 'Metal 1' are designated for thermal design and indicate the placement of Cu coins. These Cu coins must be connected from the bottom surface of the lowest layer up to the 'Metal 3', where the chip is mounted.

The second layer, 'Metal 2' is responsible for routing the bias supply lines such as VDD, VGG, and VC for the GaN based SPDT

switch, high power amplifier, and GaAs based low noise amplifier

To minimize interference with RF signal lines, this layer is designed to carry only bias currents independently, and it is configured together with appropriate decoupling capacitors and ground structures. This design minimizes DC noise and coupling effects between DC and RF signals, thereby ensuring the linearity and stability of the overall system.

Figure 2.1-2 shows a 3D-EM model based on HFSS, designed using the structure of 'Metal 2', which was used to evaluate coupling with adjacent layers and to ensure power integrity.



(a) (b)

Figure 2.1-2 3D-EM Model Using HFSS ('Metal 2') ; (a) 3D view of 'Metal 2', (b) Top views of 'Metal 2'

VC bias for the TX path of the SPDT, VDD bias for the HPA, VGG bias for the LNA are all routed through 'Metal 2'. These bias lines

are positioned close to the corresponding pads of each chip to minimize wire-bonding distance, and they are connected through vias to 'Metal 4', where the chips are mounted, in order to supply the required bias voltages.

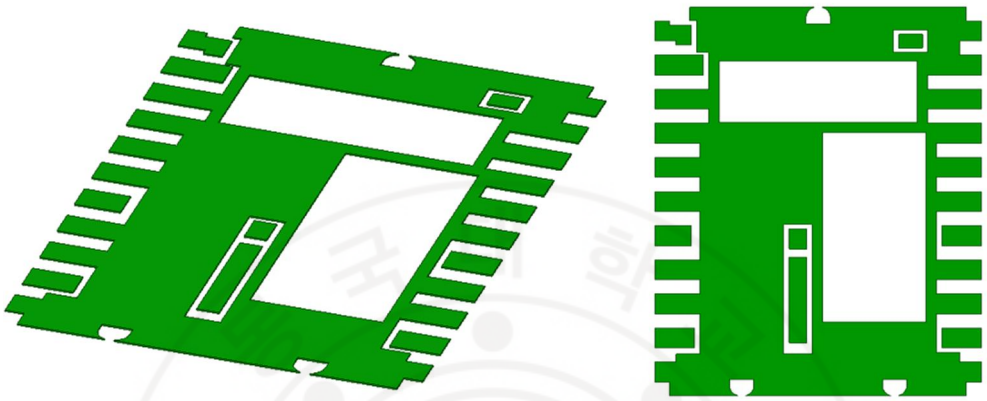
The semicircular holes located RF ports are designed to serve as ground paths for forming coaxial vias. These semicircular openings enable the implementation of symmetrical ground connections surrounding the central signal via, thereby forming a coaxial structure. This configuration helps ensure signal integrity by providing a low inductance return path and effective electromagnetic shielding, especially critical at RF interfaces.

The third layer, 'Metal 3' serves as an intermediate ground plane for the upper RF routing layer, 'Metal 4'. This layer provides the return path for CPWG signal lines while also acting as a shielding layer between RF signals and DC bias lines, thereby suppressing interlayer electromagnetic interference.

In multi-layer substrate structures, parasitic coupling through the substrate can occur, and Metal 3 plays a key role in mitigating such parasitic effects by confining electromagnetic energy locally. This contributes to the stability of the system's RF performance.

Figure 2.1-3 shows a 3D-EM model based on HFSS, designed

using the structure of 'Metal 3', which was used to optimize for ground coverage and via density.



(a) (b)

Figure 2.1-3 3D-EM Model Using HFSS ('Metal 3') ; (a) 3D view of 'Metal 3', (b) Top views of 'Metal 3'

The topmost layer, 'Metal 4' is the primary layer where RF signal routing is implemented, and it includes bonding pads for wire connections between the package board and the chips.

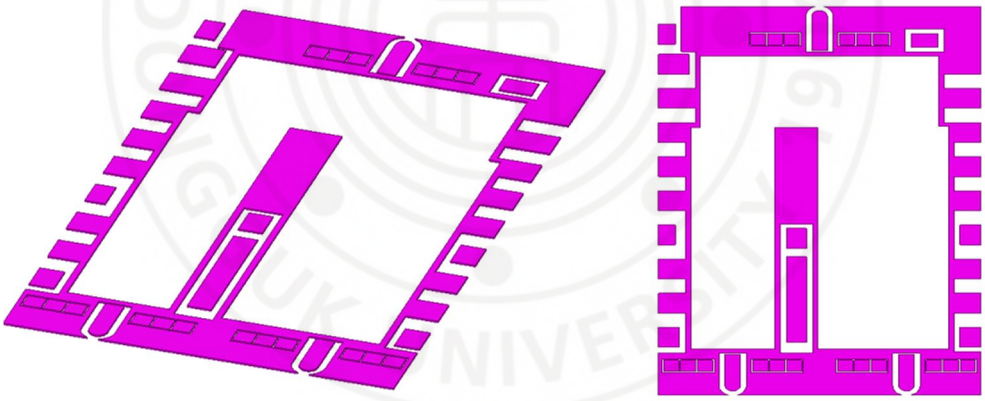
To ensure reliable wire bonding, ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold) surface finish is applied to the bonding pads. This surface treatment provides excellent bond-ability and corrosion resistance, while maintaining electrical performance suitable for high frequency applications [9].

This layer connects the RF signal pads of the GaN/GaAs chips to the corresponding package side pads, and each signal is routed to

external lead pads for interfacing with the system.

The signal traces on this layer are designed to maintain a 50Ω impedance, with optimized trace width, spacing, and routing paths to minimize insertion loss. Additionally, the positions of the bonding pads and wire lengths were carefully considered to suppress resonances within the package.

Figure 2.1-4 shows a 3D-EM model based on HFSS, designed using the structure of 'Metal 4', which was used to evaluate the adequacy of the signal line structure, pad layout, and surrounding ground configuration.



(a) (b)

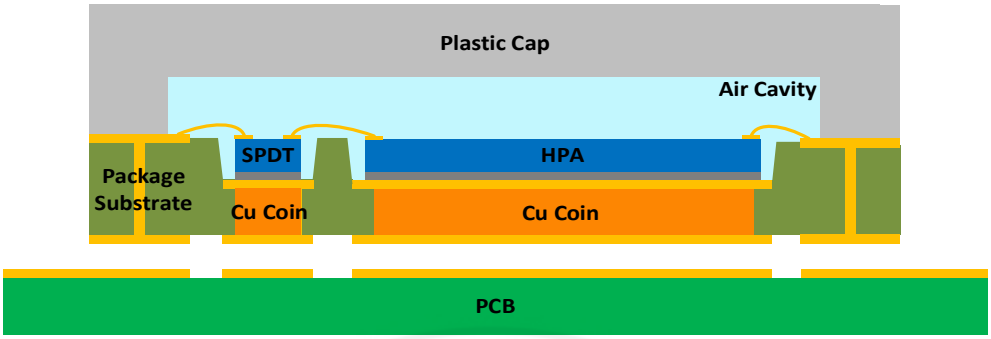
Figure 2.1-4 3D-EM Model Using HFSS ('Metal 4') ; (a) 3D view of 'Metal 4', (b) Top views of 'Metal 4'

The RF port region is routed starting from the rounded section designed for coaxial vias, extending toward the chip pads to ensure

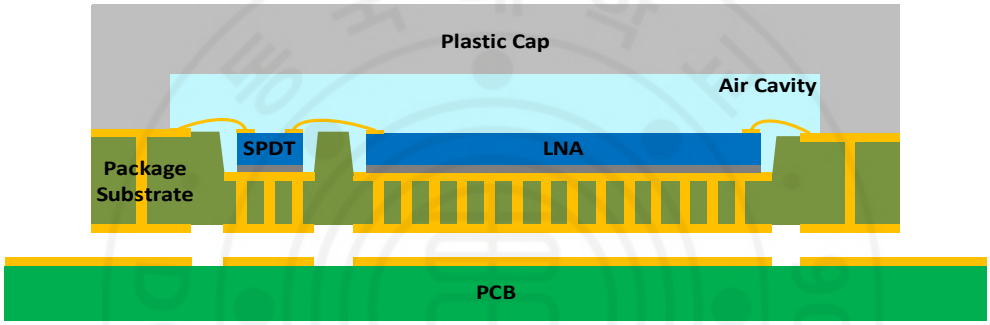
a short and efficient signal path. Around the RF signal lines, tuning pads are strategically placed near the bonding area, utilizing open stubs to form capacitive elements that allow for fine impedance adjustment. At the center, a hole is reserved for chip mounting. To accommodate potential epoxy overflow during the assembly process, the design secures 120μm clearance between the chip and the wall, ensuring both mechanical reliability and ease of manufacturing [10].

2.1.1.2 Introduction of Cavity Substrate & Cu Coin

In this study, to effectively address the thermal issues associated with high power GaN based chips, 200μm thickness of Cu coin was designed to extend from the bottom metal layer, 'Metal 1' to the chip mounted metal layer, 'Metal 3', thereby securing a direct heat conduction path. This structure minimizes the thermal resistance between the chip and the heatsink, enabling stable thermal management even during high power operation [11]. Figure 2.1-5 shows the cross-sectional view of the designed package.



(a)



(b)

Figure 2.1-5 Cross-sectional view of designed package ; (a) Tx Side, (b) Rx Side

The Cu coin beneath the HPA was designed with dimensions of 3.3 mm × 1.45 mm, while the coin beneath the SPDT was designed with dimensions of 1 mm × 2.85 mm.

Additionally, to mitigate the degradation of high frequency signal integrity caused by increased wire bonding length due to chip height, a cavity substrate structure was introduced by forming a cavity in the chip mounting area. The cavity depth was precisely designed to be 100μm, matching with the chip height, in order to minimize the

vertical offset between the chip and the bonding pads. This approach reduces bonding wire length and inductance, thereby suppressing impedance mismatch and resonance phenomena at high frequencies.

To minimize signal loss and ensure stable dielectric characteristics in the high frequency domain, BT resin was used as the substrate material instead of the commonly used FR-4. BT resin offers low signal attenuation even at high frequencies and allows for precise and uniform control of interlayer thickness $80\mu m$ or $100\mu m$, which is advantageous for designing characteristic impedance matching of transmission lines within the package [12].

Furthermore, all metal layers from 'Metal 1' to 'Metal 4' were formed using $18\mu m$ thick copper. A multi-layer metal stack was adopted, in which each layer is functionally separated to prevent interference between RF signal lines, bias lines, and ground planes, ensuring overall electromagnetic stability of the package.

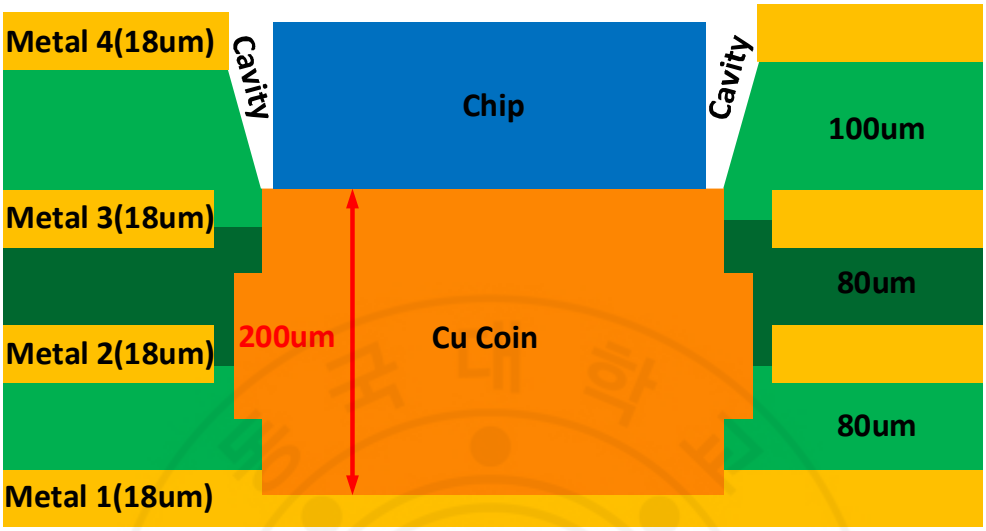
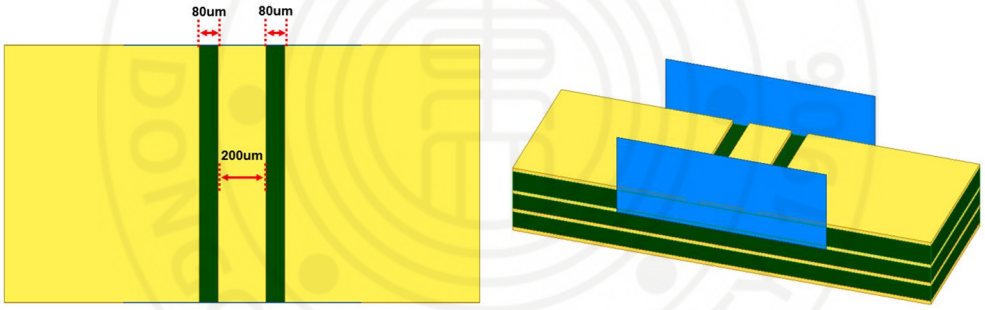


Figure 2.1-6 Layer stack of designed package

Figure 2.1-6 shows the layer stack of the designed package. The Cu coin was designed with a minimum possible thickness of 200μm, which corresponds to the minimum manufacturable thickness based on actual PCB fabrication constraints. This decision was made to minimize the via length between Metal 1, where the RF signal is supplied, and Metal 4, where the chip pad is located. Since the RF signal is transmitted from Metal 1 to the chip pad through vertical vias, a longer via length would result in more insertion loss. Therefore, reducing the thickness of the Cu coin helps to shorten the via path and improve RF transmission efficiency.

2.1.1.3 Impedance Matching and Signal Integrity

Considering the role of Metal 4, the routing from the bonding pad where wire bonding is performed to the edge lead pad functions as an RF signal line and must maintain signal integrity through 50Ω impedance matching. Therefore, Metal 4 was designed as a Coplanar Waveguide with Ground (CPWG) structure, using the underlying Metal 3 layer as the ground reference. This configuration ensures controlled impedance and effective electromagnetic confinement, which are essential for high frequency signal transmission.



(a) (b)

Figure 2.1-7 3D-EM Model Using HFSS ; (a) Top view of 50Ω CPWG line, (b) Model for Extracting the Impedance of a 50Ω CPWG Line

Figure 2.1-7 shows the HFSS 3D-EM Model used to extract the impedance of a 50Ω CPWG line. Subfigure (a) shows the top view of the CPWG structure, which is designed with a signal line width of 200μm and a gap of 80μm between the signal line and the adjacent ground planes, while subfigure (b) shows the simulation model used

to analyze its impedance characteristics. This model was configured to evaluate the effects of line width, ground spacing, and substrate properties on characteristic impedance, and served as the reference geometry for designing matched RF lines within the SiP package.

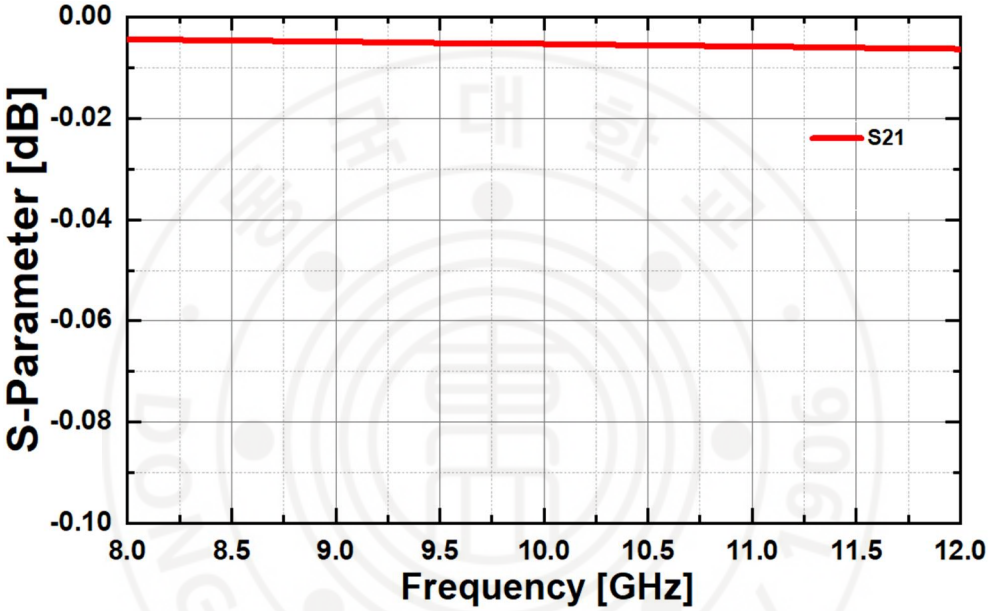


Figure 2.1-8 Simulation results of insertion loss for the 50Ω CPWG line

Figure 2.1-8 shows the insertion loss for the designed 50Ω CPWG line. Simulation results indicate that the insertion loss remains consistently low across the X-band, with values below 0.01dB, demonstrating excellent transmission efficiency and minimal signal attenuation. This confirms the effectiveness of the CPWG design for high frequency applications.

2.1.2 Proposed Wire-Bonding Structure

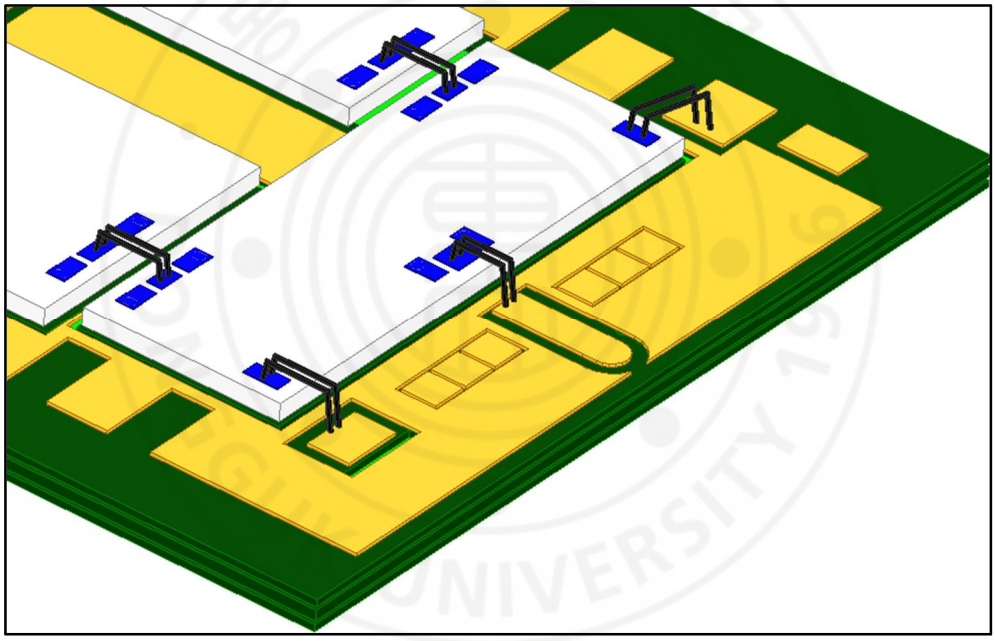
Among the various parasitic elements present in the package structure, wire-bonding was found to have the greatest impact on both insertion loss and inductance. This is because wire-bonding serves as the final electrical connection between the chip and the package substrate, located at the termination of the signal path. It is also a physically flexible and geometrically variable interconnect, making it highly sensitive to layout and assembly conditions.

In high frequency environments, the parasitic inductance introduced by wire-bonding increases significantly with wire length and height, becoming a major contributor to insertion loss. Typically, wire bonds can introduce inductance which is substantially higher than the parasitic caused by vias, transmission lines, or metal layers within the package [13].

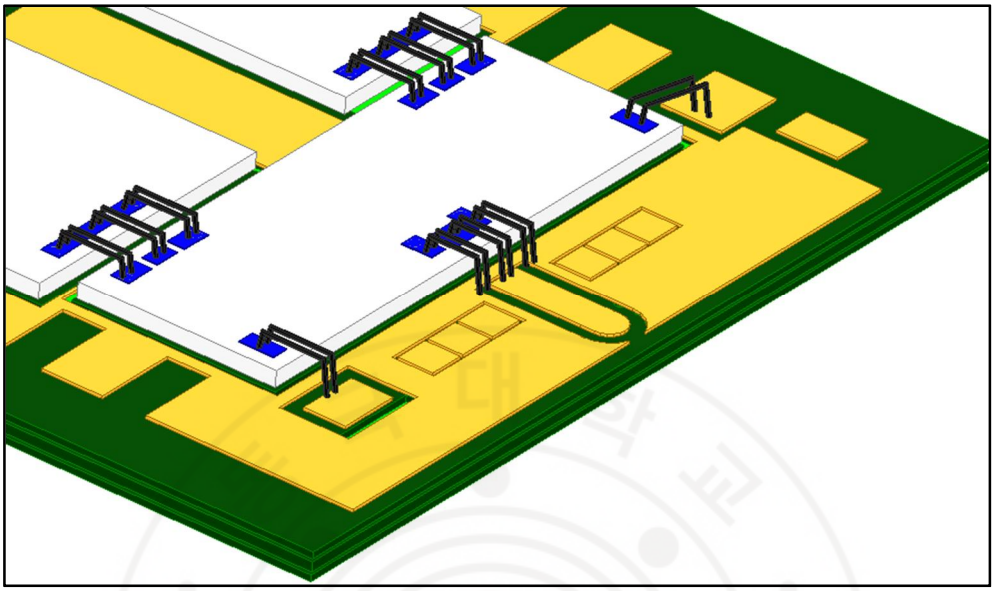
To minimize these effects, the proposed design implemented short bond wires, as well as double bonding and ground reinforcement bonding structures. These approaches reduce the current loop area and strengthen the return path, thereby effectively lowering both insertion loss and inductance.

2.1.2.1 Inductance and Insertion Loss According to Wire Bonding Height and Supplementary Ground Wire-Bonding

To optimize RF performance in SiP, various wire-bonding techniques were applied focusing on bonding height, length, and supplementary ground bonding [14]. Figure 2.1-9 shows the step by step structural improvement process, showing that a total of three different bonding configurations were applied.



(a)



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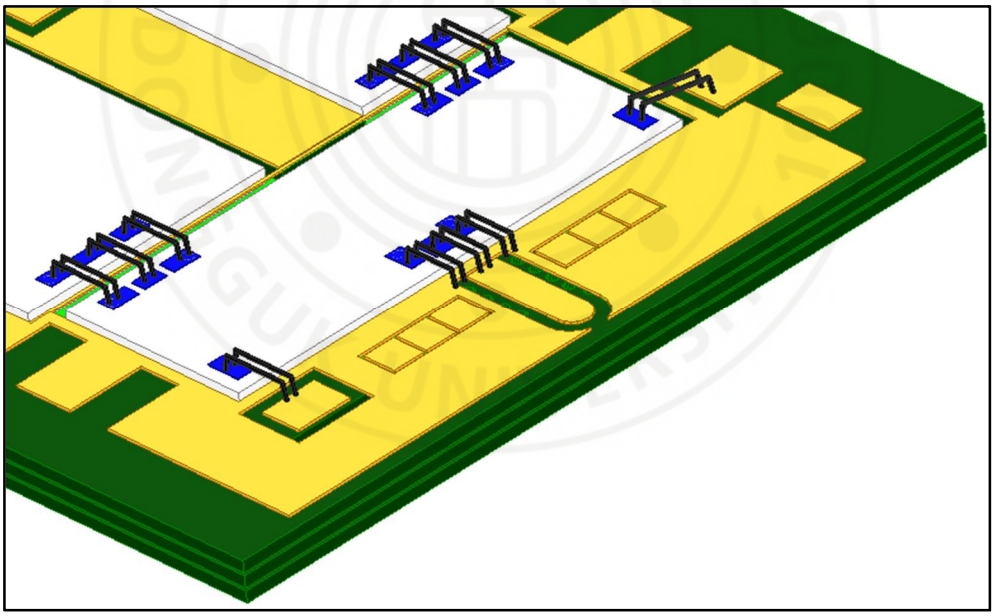


(c)

Figure 2.1-9 Step-by-Step Structural Evolution of Wire-bonding Configurations

First, to minimize the parasitic inductance and insertion loss of wire-bonding at high frequencies, the straight line distance between RF pads was designed to be less than 300μm. Assuming that R_{load} and R_{chip} are impedance matched at 50Ω, the insertion loss as a function of bonding wire length can be expressed by the following equation.

$$IL_{dB} \approx 20\log_{10}\left|\frac{2R_{load}}{R_{chip} + j\omega L_{wire} + R_{load}}\right| \quad \textbf{(2.1.1)}$$

L_{wire} denotes the inductance of the bonding wire, which is generally proportional to its length.

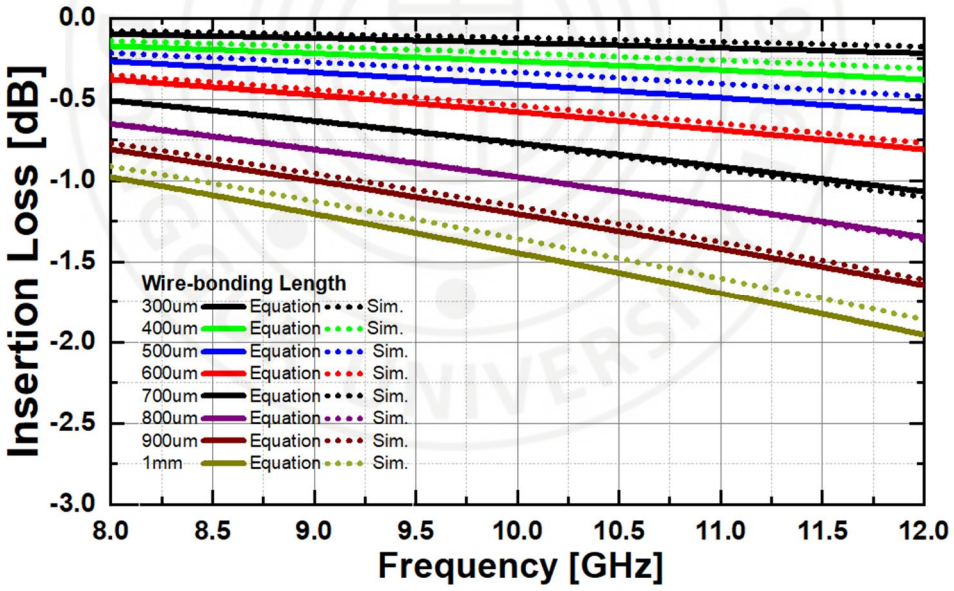


Figure 2.1-10 Insertion loss as a function of bonding wire length

Figure 2.1-10 shows the insertion loss as a function of bonding wire length, obtained by applying the equation. When the bonding length exceeds $500\mu m$, a significant increase in insertion loss is observed in the X-band frequency range. This is because, at high frequencies, the inductance introduced by the long bonding wire adds meaningful impedance to the circuit, causing reflections and losses. Such effects become more pronounced as the frequency increases.

Next, as shown in Figure 2.1-11(b), to further enhance electrical performance, supplementary ground wire-bonding was introduced. This method involves adding additional wire-bonding between the ground pads of the chip and the surrounding ground structures of the package. These supplementary ground wire-bonding provides multiple low inductance return paths, which help suppress ground bounce and minimize coupling between RF signals and bias lines or adjacent signal traces. As a result, unwanted resonances are mitigated, RF/DC isolation is improved, and electromagnetic fields around the signal lines are more effectively confined [15].

Finally, as shown in Figure 2.1-11(c), the entire bonding structure benefits directly from the implementation of a cavity substrate. By forming a recessed cavity in the chip mounting area, the vertical distance between the top surface of the chip and the bonding pads on

the package is reduced [16]. As a result, both the height and length of the bonding wires are minimized. This structure is highly effective in further reducing parasitic inductance and insertion loss, and it is particularly advantageous in suppressing wire induced resonances that may occur in the upper X-band.

Figure 2.1-11 shows the simulation results of inductance and insertion loss for each bonding configuration. According to the simulation results, in the X-band, the configuration that incorporates both the cavity substrate used to reduce bonding height and supplementary ground wire-bonding exhibits approximately 700 pH of parasitic inductance, with an insertion loss is from 0.7 to 0.8 dB. This demonstrates the effectiveness of the proposed enhancements in minimizing signal degradation at high frequencies.

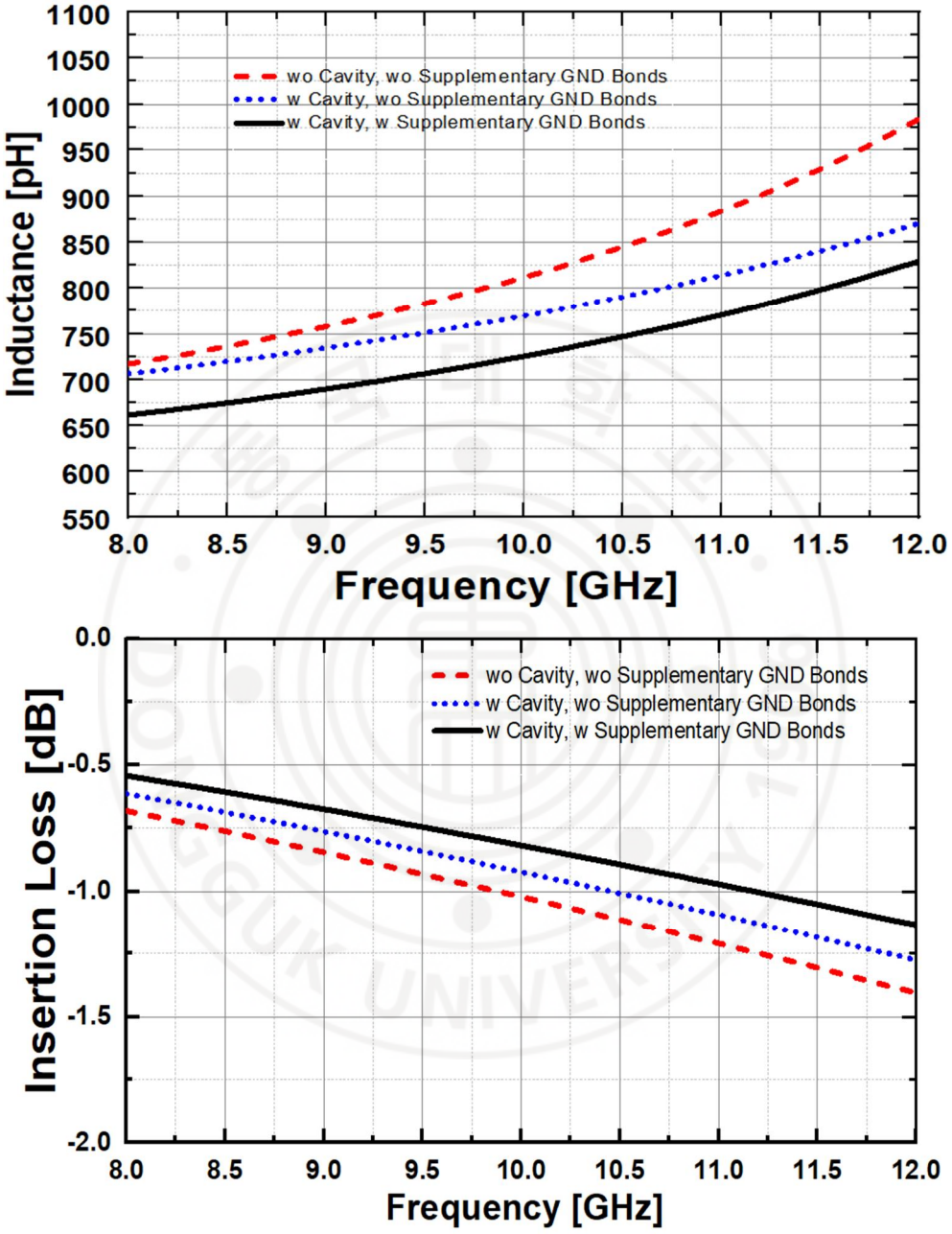


Figure 2.1-11 Simulation results of inductance and insertion loss for each bonding configuration.

The following equation quantitatively describes the impact of reflection coefficients on insertion loss.

$$IL_{dB} = 10\log_{10}\left[\frac{\left|1-\Gamma_s\right|^2\left(1-\left|\Gamma_{in}\right|^2\right)}{\left|1-\Gamma_s\Gamma_{in}\right|^2}\right] \quad \textbf{(2.1.2)}$$

$$\Gamma_{in} = \frac{\left(Z_L + j\omega L_{wire}\right) - Z_0}{\left(Z_L + j\omega L_{wire}\right) + Z_0} \quad \textbf{(2.1.3)}$$

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \quad \textbf{(2.1.4)}$$

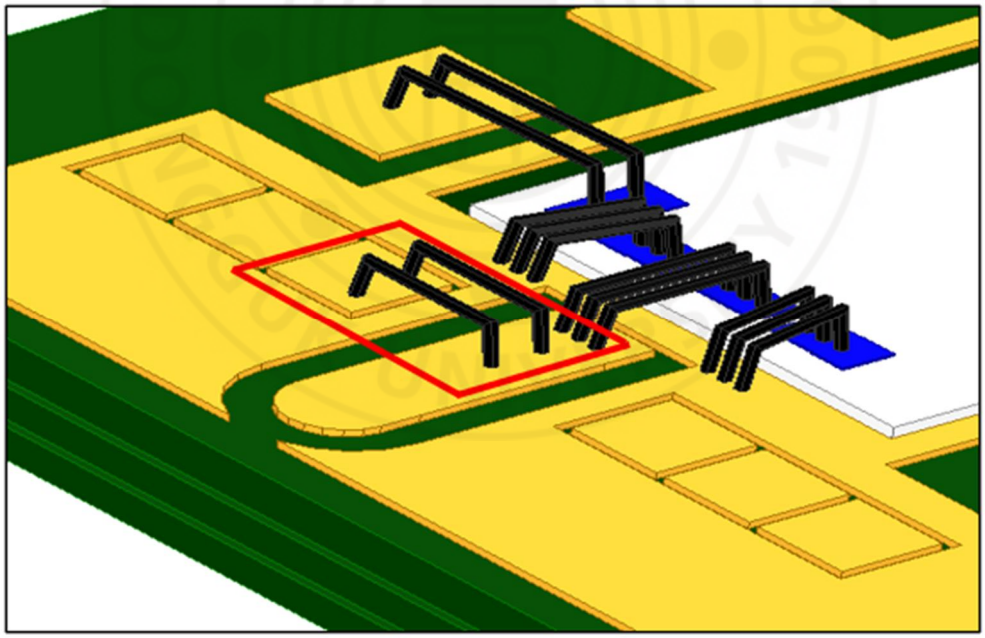
The insertion loss is determined by the interaction between the source reflection coefficient, Γ_s and the input reflection coefficient, Γ_{in} where Γ_{in} is defined by incorporating the inductance L_{wire} introduced by wire bonding. In high frequency operation, the term $j\omega L_{wire}$ significantly affects impedance matching, thereby contributing to the overall reflection characteristics and insertion loss of the system. Furthermore, the optimal source impedance, $Z_{s(opt)}$ is defined as the complex conjugate of the total impedance including the load impedance, Z_L and the bonding inductance.

$$Z_{s(opt)} = \left[Z_L + j\omega L_{wire}\right]^* \quad \textbf{(2.1.5)}$$

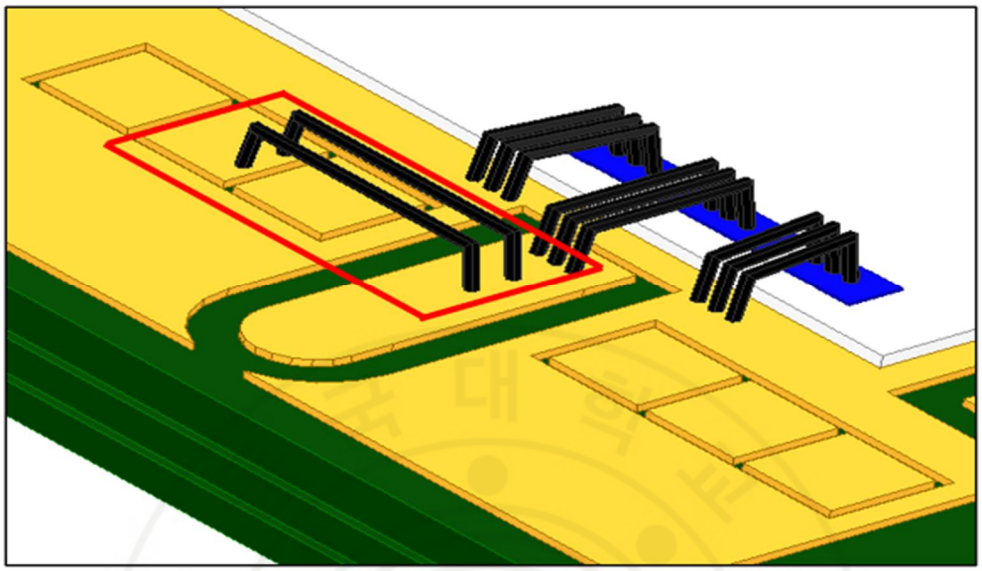
Therefore, the output impedance matching of a chip connected through wire-bonding can be carried out based on the above equations.

2.1.2.2 Inductance and Insertion Loss Compensation effect of Open Stub Formed by Wire-Bonding

In high frequency SiP transceivers, impedance mismatch at the RF interface can lead to significant reflection loss and degradation in signal integrity. To address this, the proposed package incorporates a wire-bonding based open stub structure as a fine impedance matching technique [17]. Figure 2.1-12 shows the implementation of this approach, where bonding wires are intentionally connected to the RF signal line and open-ended, forming open stubs within the package layout.



(a)



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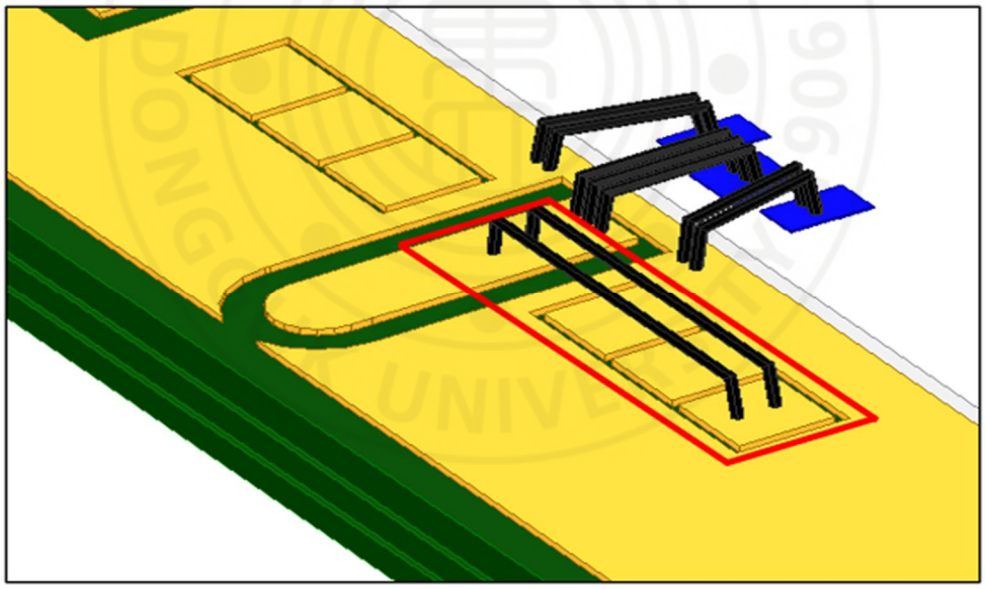


(c)

Figure 2.1-12 Implementation of Open Stub Structures Using Wire Bonding with Bonding Lengths

These wire bonds are designed to behave as open-ended transmission lines, introducing reactive elements either inductive or capacitive depending on the electrical length into the signal path. This enables compensation for minor impedance mismatches and enhances impedance continuity across the frequency band of interest. The reactance X_{stub} contributed by the open stub can be approximately modeled by

$$X_{stub} = -Z_0 \cdot \cot\left(\frac{2\pi l}{\lambda}\right) \quad \textbf{(2.1.6)}$$

where l is the stub length, λ is the wavelength at the design frequency, and Z_0 is the characteristic impedance. As the stub length increases, the reactance becomes more capacitive, effectively tuning the impedance at lower frequencies. Conversely, shorter stubs are better suited for tuning at higher frequencies.

In the proposed design, the length of the bonding stubs was carefully optimized to introduce a target capacitance for fine tuning in the upper X-band range. Moreover, the position and proximity of the stub to the ground plane were also considered, as the effective capacitance between the stub and ground increases as the vertical spacing d decreases. The effective capacitance can be approximated as

$$C_{eff} \approx \frac{\varepsilon_r \varepsilon_0 A}{d} \quad \textbf{(2.1.7)}$$

where ε_r is the relative permittivity of the BT resin, ε_0 is the vacuum permittivity, A is the overlapping area between the stub and the ground plane, and d is the vertical distance.

To suppress parasitic coupling and maintain matching accuracy, the stub was placed parallel to the signal line with controlled spacing, and the ground plane was positioned directly below with sufficient via stitching. Simulation results confirmed that this structure provided effective tuning with minimal insertion loss, contributing to the overall RF performance of the system.

By incorporating this open stub matching structure within the bonding design, the proposed package demonstrates enhanced flexibility in high frequency impedance control, particularly beneficial for multi-chip integration in SiP architectures operating in the X-band.

Figure 2.1-13 shows the simulation results of inductance and insertion loss according to the bonding wire length used in the open stub matching structure.

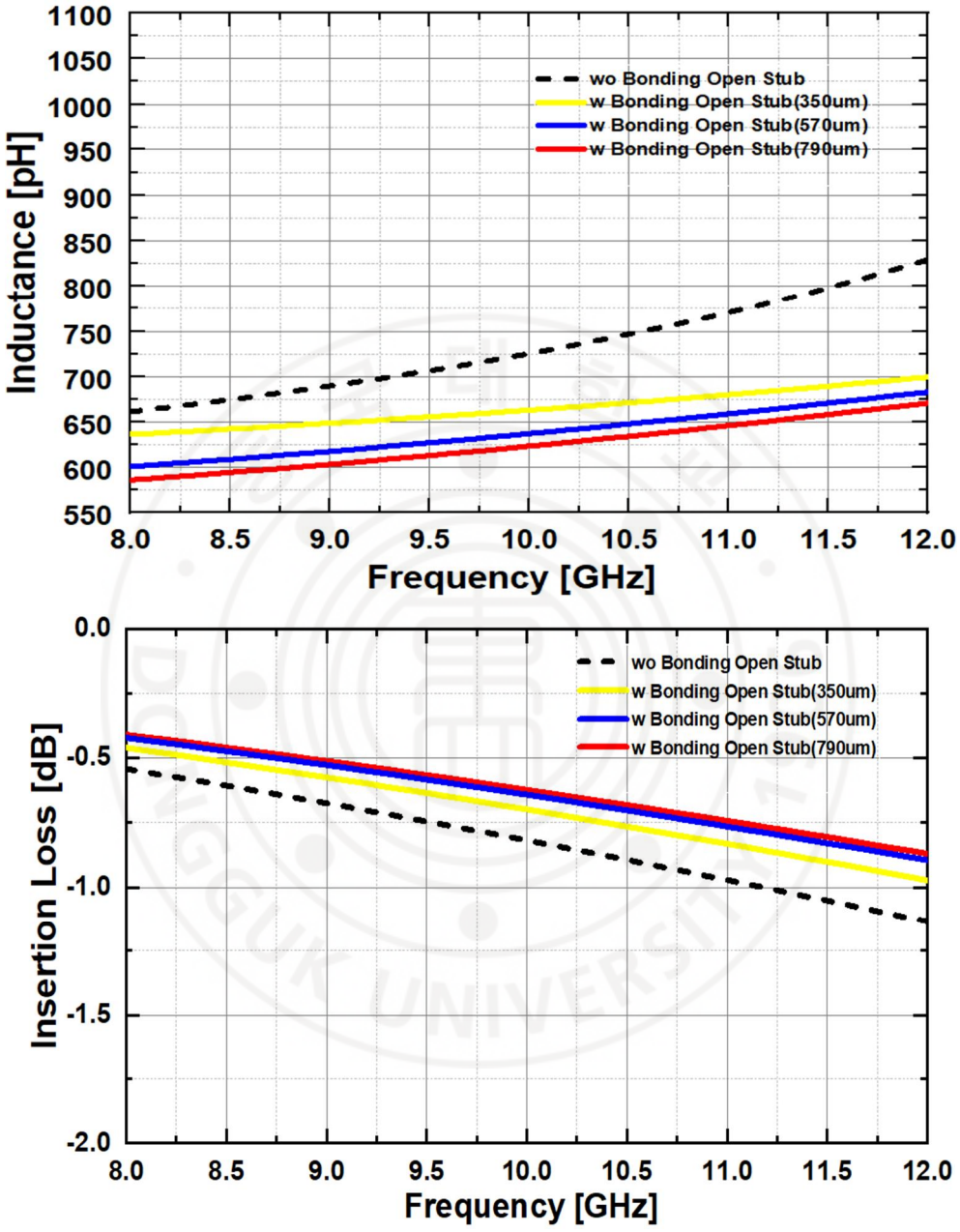


Figure 2.1-13 Simulation results of inductance and insertion loss according to the bonding wire length used in open stub matching

According to the simulation results, the impedance matching characteristics were found to vary significantly depending on the length of the wire-bonded open stubs within the X-band. In this study, tuning regions were implemented using bonding wire lengths of 350μm, 570μm, and 790μm , each exhibiting distinct impedance compensation behavior. In the baseline structure with approximately 700 pH of parasitic inductance, the open stubs were able to offset up to 100 pH, depending on their length, thereby improving impedance matching as verified through simulation.

This inductance compensation effect contributed to a reduction in reflection loss along the RF signal path. As a result, the insertion loss was also improved, maintaining a level of approximately 0.6 to 0.7 dB. These findings clearly demonstrate that the electrical impact of wire-bonding can be precisely controlled in high frequency package design.

2.1.3 Proposed RF Via Structure

Vias used within the package can be broadly classified into two categories based on their function vias for supplying DC bias voltage, and vias for transmitting high frequency signals. In particular, the vias used in RF signal paths must be structurally optimized to minimize high frequency signal loss and maintain signal integrity.

Conventional single via structures tend to exhibit increased parasitic inductance at high frequencies, which can lead to higher insertion loss, signal reflections. To address these issues, this study adopts a coaxial via structure. In this configuration, a central signal via is surrounded symmetrically by multiple ground vias, forming a uniform return current path. This significantly reduces the inductance in the signal transmission path and suppresses unwanted electromagnetic interference. Moreover, the coaxial via structure is advantageous for maintaining the characteristic impedance of the transmission line [18].

To compare the electrical performance of coaxial and conventional via structures, a 3D electromagnetic simulation model was developed using Ansys HFSS. The simulation evaluates the frequency response characteristics of each structure, focusing on insertion loss, return loss, and current distribution in the X-band.

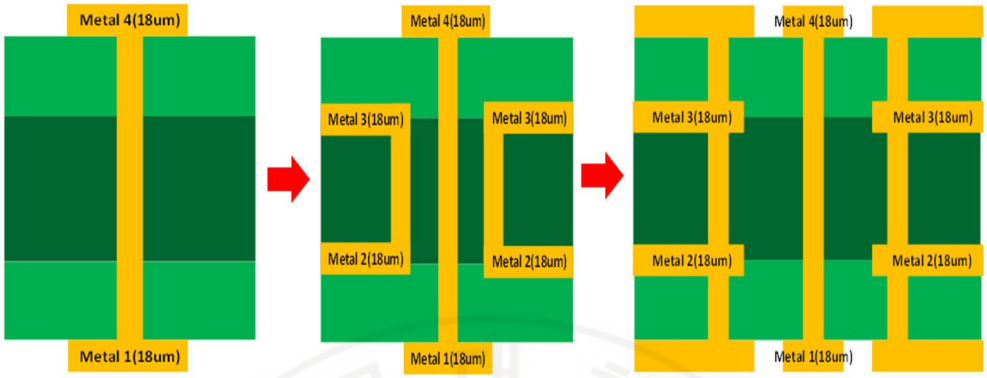


Figure 2.1-14 Cross-sectional views of the coaxial via and conventional single via structures

Figure 2.1-14 shows cross-sectional views of the coaxial via and conventional single via structures, clearly illustrating the differences in grounding configuration and layout, which lead to distinct electromagnetic behaviors.

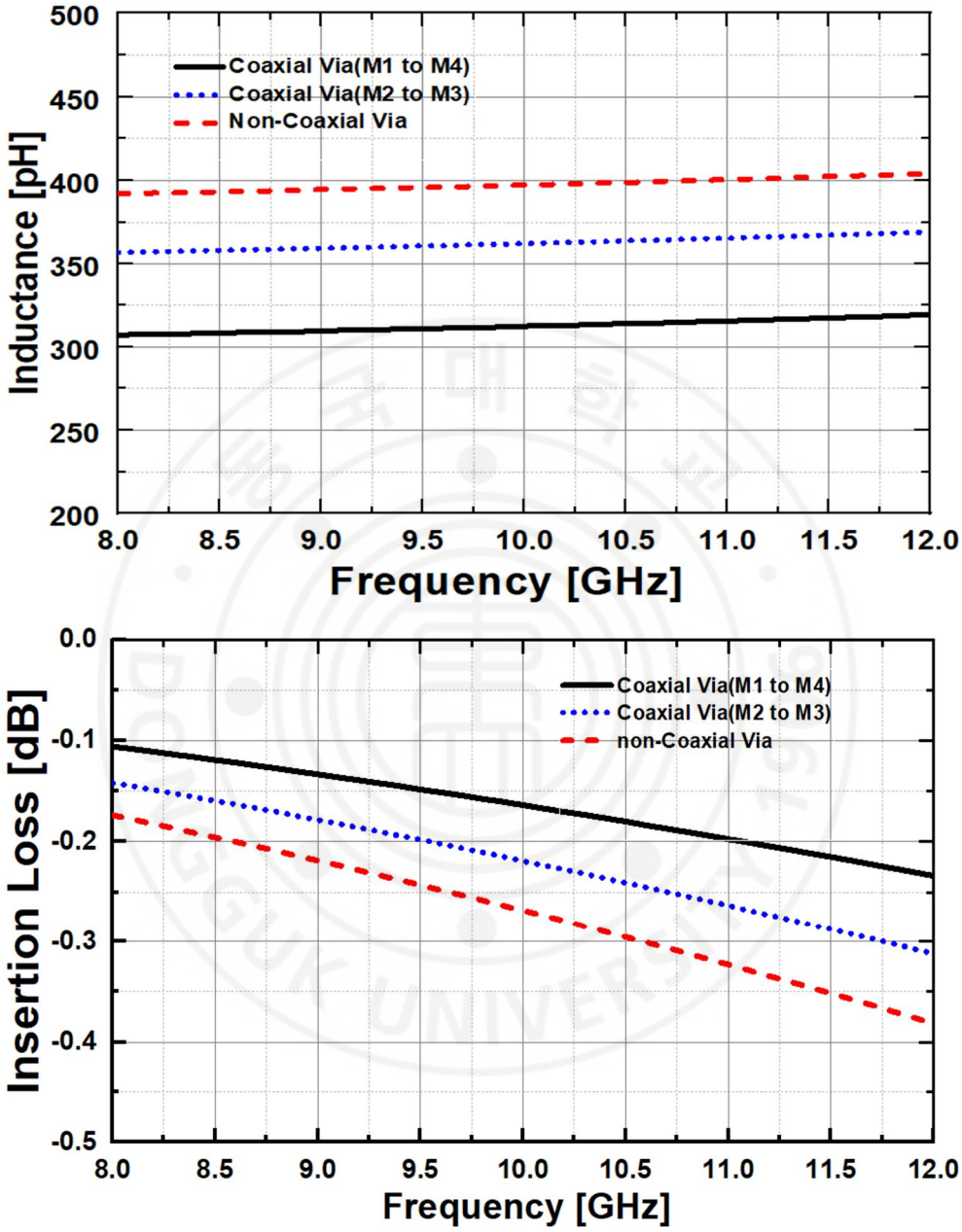


Figure 2.1-15 Simulation results of inductance and insertion loss according to the height of the ground return path

Figure 2.1-15 shows the simulation results analyze the variation in electrical characteristics with respect to the height of the ground return path within the X-band. The analysis showed that as the height of the ground path increases, the amount of canceled parasitic inductance also increases. This is attributed to the improved quality of the return current path formed by the ground vias, which shortens the overall current loop and reduces its inductance.

In particular, by forming a coaxial via type ground structure, it was confirmed that up to approximately 100 pH of inductance reduction can be achieved in the X-band compared to a conventional single via structure. This contributes to mitigating electromagnetic reflections and impedance discontinuities, which are critical factors in high frequency design.

Furthermore, along with the reduction in inductance, insertion loss also showed improvement, with up to approximately 0.1 dB of insertion loss reduction observed as the height of the ground path increased. These results demonstrate that even minor geometrical adjustments, such as increasing the height of the ground vias, can significantly enhance transmission efficiency and signal quality in high frequency package designs.

Similar to the structure used in conventional coaxial cables,

surrounding a signal via with a fully cylindrical ground shield represents the theoretically ideal coaxial via configuration. However, implementing such a structure directly within package substrate is practically challenging due to structural limitations inherent in the manufacturing process. In high density circuits in particular, forming a continuous circular ground wall is constrained by via pitch limitations, layout restrictions, and the complexity of drilling processes [19].

Therefore, this study proposes a manufacturable coaxial via structure that accounts for these practical constraints. The proposed design arranges multiple ground vias symmetrically or at equal intervals around a central signal via, thereby enabling effective ground shielding at high frequencies. A critical design criterion in this configuration is that the spacing between adjacent ground vias must be sufficiently small compared to the effective wavelength of the signal. In other words, the structure is effective when the maximum spacing d between ground vias satisfies the following condition

$$d \square \ \lambda_{eff} = \frac{c}{f\sqrt{\varepsilon_{eff}}} \tag{2.1.8}$$

When this condition is met, electromagnetic leakage and interference between the gaps of the ground vias become negligible,

allowing the structure to provide a grounding effect similar to that of an ideal cylindrical shield. In fact, a 3D electromagnetic simulation using HFSS was performed on the proposed structure, and the results confirmed that there was no significant difference in inductance or insertion loss compared to the ideal cylindrical ground shield. This outcome is attributed to the skin effect, where electromagnetic energy propagates primarily along the metal surface at high frequencies, and to the localized concentration of electromagnetic fields. In other words, rather than requiring a continuous ground wall, a sufficiently dense array of ground vias can effectively form an electromagnetic shield in practice. Figure 2.1−16 shows the coaxial via structure as implemented in this study.

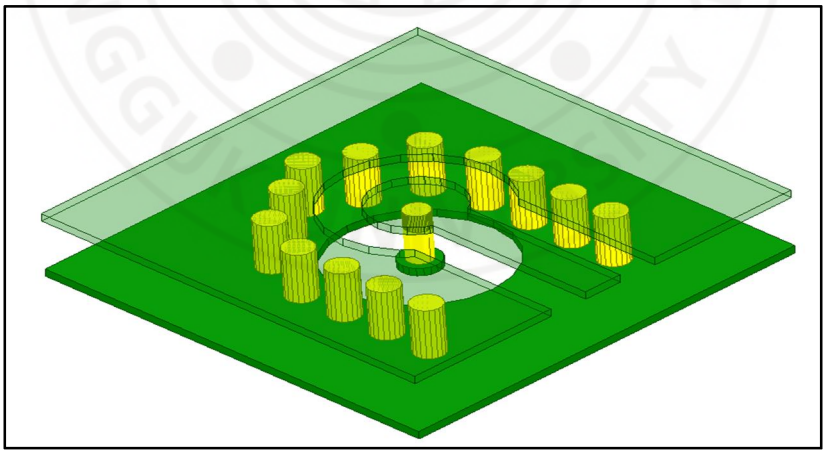


Figure 2.1-16 Coaxial via structure implemented in this study

2.2 Integrated Design of X-band SiP QFN Package

X-band transceiver SiP, which integrates both transmit and receive functions within a single package, is significantly influenced by system level interactions rather than just the performance of individual circuit blocks. Since components such as the SPDT switch, high power amplifier, and low noise amplifier each with different operating conditions and electrical characteristics are integrated on a single substrate, the overall system performance can be affected by factors such as parasitic coupling, return path interference, common ground noise, and thermal crosstalk between components [20]. Therefore, simulations of individual circuit blocks alone are not sufficient to guarantee the reliability of the entire package. A comprehensive evaluation must be conducted through full package 3D electromagnetic simulations, which take into account the interactions among all components within the integrated structure. This is especially critical for high frequency transceiver modules, where even small structural variations can lead to impedance mismatches, increased insertion loss, and unwanted resonances. For this reason, accurate EM based validation at the package level is essential prior to fabrication.

2.2.1 Structure of Integrated SiP QFN Package

Figure 2.2-1 shows the overall chip placement and pad layout of the transceiver SiP (System-in-Package) proposed in this study.

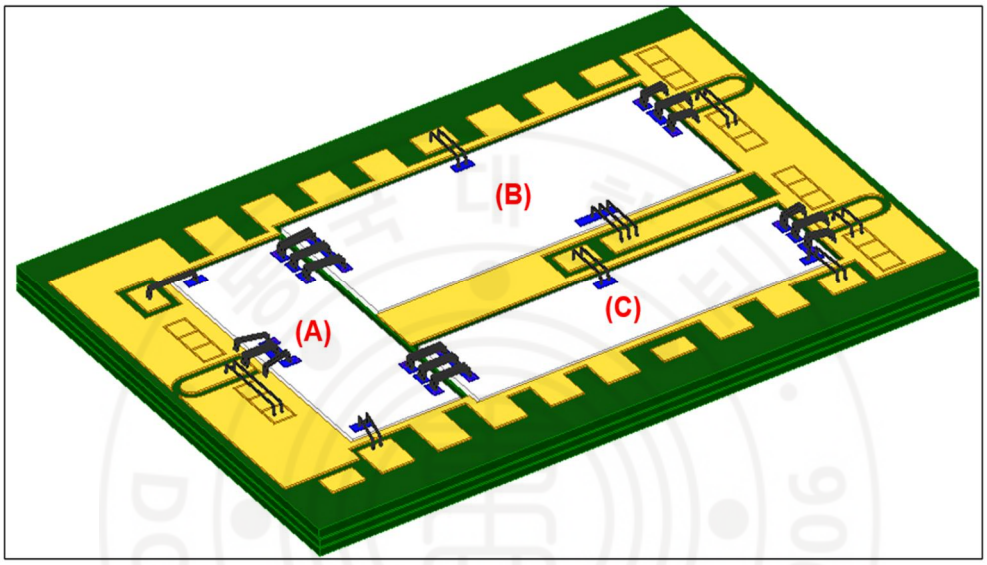


Figure 2.2-1 Chip placement and layout of the transceiver SiP proposed in this study

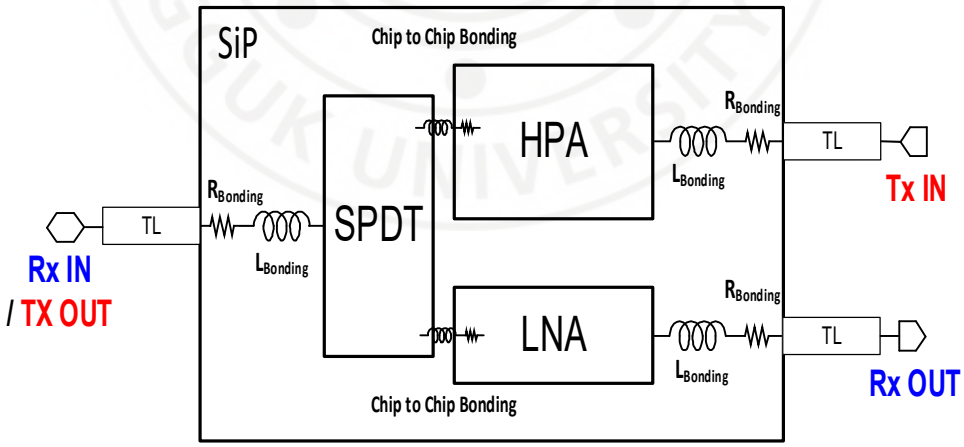


Figure 2.2-2 Block Diagram of the transceiver SiP proposed in this study

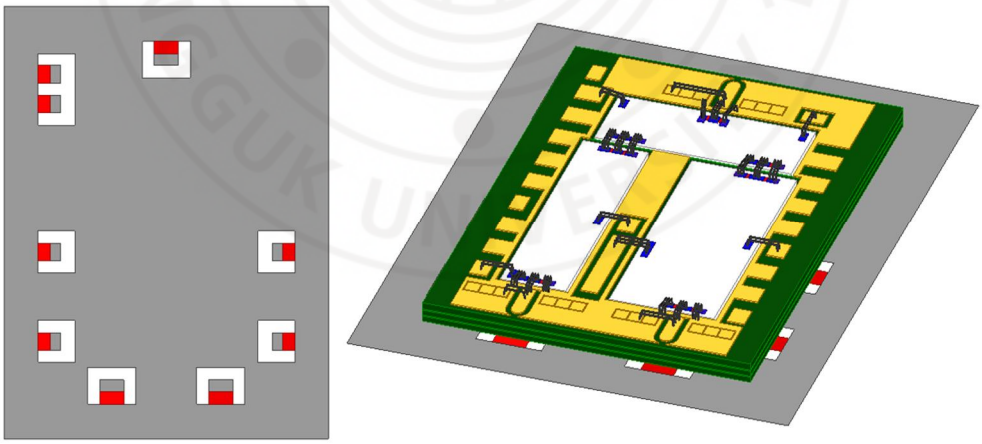
Figure 2.2-2 shows the block diagram of the transceiver SiP proposed in this study. The structure integrates multiple heterogeneous semiconductor chips, each fabricated using different processes, into a single high density package. The functional blocks are arranged as follows: At position (A) is the SPDT switch, fabricated using Winsemi's NP25-02 GaN process. At position (B) is the high power amplifier, also based on the same GaN process. At position (C) is the low noise amplifier, fabricated using Winsemi's NP25-02 GaAs process.

The dimensions of each chip are as follows the SPDT is 1.14 mm × 3 mm, the HPA is 3.8 mm × 1.6 mm, and the LNA is 3.8 mm × 1 mm. Since these heterogeneous chips are densely integrated within a limited area, efficient layout and structural considerations for minimizing signal interference are essential. The entire package is configured as a compact module with dimensions of 7 mm × 5 mm, optimized for high frequency communication systems requiring miniaturization and high integration.

2.2.2 Simulation Results of Integrated SiP QFN Package

Considering the characteristics of the package, it is essential to account for interlayer electromagnetic interference, as well as the signal transmission behavior of vias, Cu coins, and wire bonding, in

order to preserve the RF performance of the chip after packaging. Therefore, to evaluate the signal transmission characteristics from the bottom layer of the package to the chip pads, a full package simulation must be conducted using HFSS, including a ring shaped virtual ground plane [21]. This virtual ground plane was designed with a width of $700\mu m$, which corresponds to tenth of the total package width $7\,mm$. This dimension was carefully chosen to minimize parasitic effects that may arise from the ground structure itself, allowing it to function as an effective reference ground. Figure 2.2-3 shows the HFSS model of the fully integrated package, which was used to simulate and analyze the inductance and insertion loss characteristics of the proposed structure.



(a) (b)

Figure 2.2-3 HFSS 3D-EM Model of the fully integrated package ; (a) Virtual ground plane with port, (b) Model of the fully integrated package

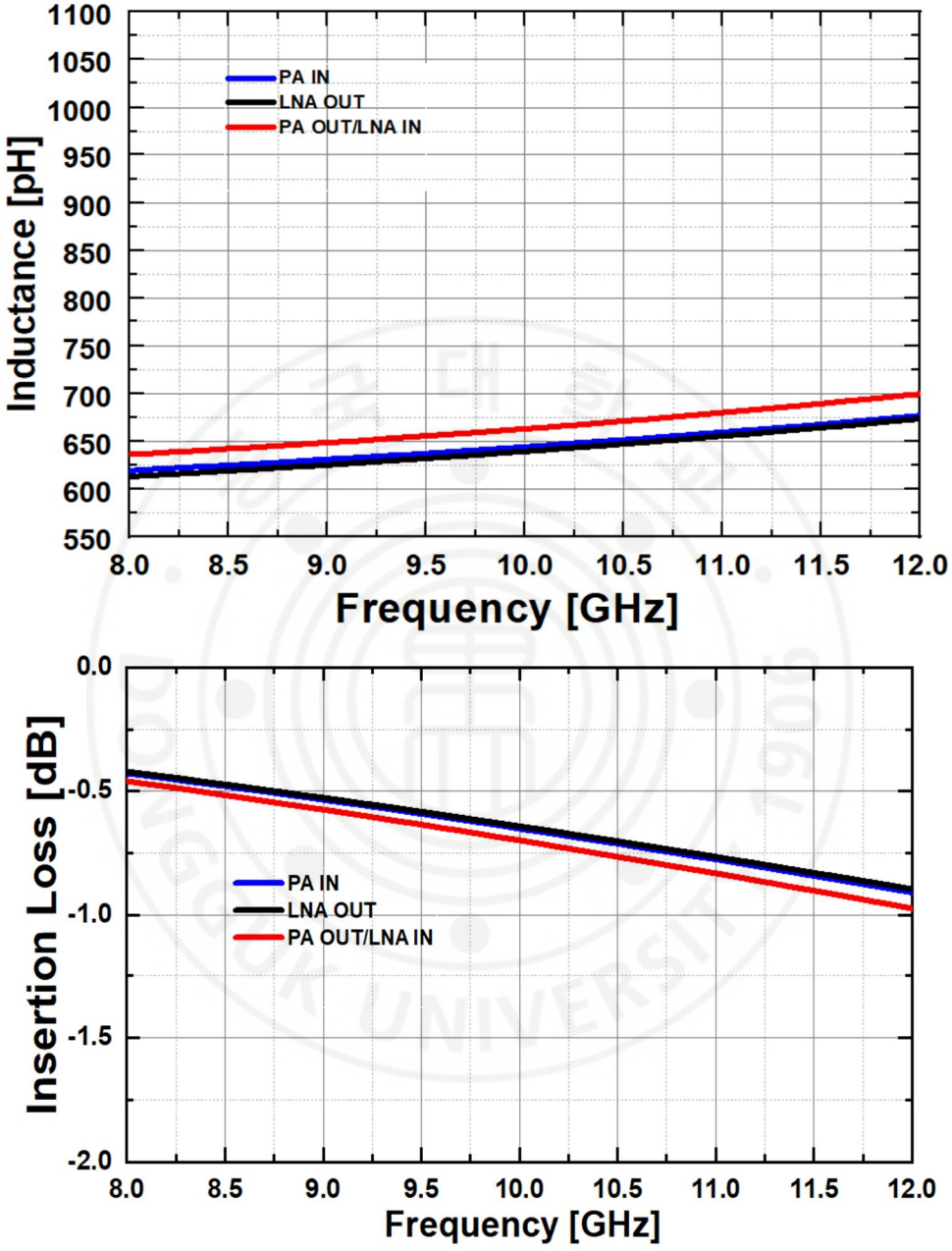


Figure 2.2-4 Simulation results of the inductance and insertion loss for the integrated package structure

Figure 2.2-4 shows the simulation results of the inductance and insertion loss for the proposed integrated package structure. In the X-band, the insertion loss at both the input and output ports is approximately 0.7 dB, while the inductance is measured to be around 700 pH. The PA input and LNA output exhibit slightly lower inductance values compared to the combined PA output and LNA input, which consistently shows the highest inductance across the entire frequency range from 8 to 12 GHz. This difference is primarily attributed to the longer routing lines associated with the PA output and LNA input paths, which inherently contribute additional parasitic inductance.

2.3 Methods for improving Simulation Accuracy

To improve simulation accuracy in high frequency environments, this study includes detailed modeling of external interface elements, particularly the SMA connector and PCB RF transmission line. A 3D EM model of the SMA connector was developed to capture parasitic effects and impedance mismatches at the connector to board interface. A calibration board replicating the assembled SMA connector and RF line was fabricated. Insertion loss and return loss were measured and compared with simulation results, allowing refinement of the model and alignment with actual performance. This approach enhances the reliability of simulation results, ensuring closer agreement with real world measurements.

2.3.1 Calibration of the SMA Connector

At high frequencies, the structural characteristics of the SMA connector such as the length of the center pin, the contact area between the outer shield and the PCB can introduce parasitic capacitance and inductance at the interface with the transmission lines and pads.

If these effects are not accounted for in the simulation, idealized port impedance is assumed, which can result in discrepancies between

simulation and measurement. Therefore, in the HFSS model, the physical geometry, contact location, and electrical boundary conditions of the SMA connector were implemented to match the actual measurement setup. This approach significantly improved the accuracy of predicted insertion loss and return loss characteristics.

Such connector modeling plays a key role in accurately reflecting port matching conditions at high frequencies, and it can also be applied to the design of interconnection structures between the package and the PCB in future implementations.

2.3.1.1 Methods of Modelling SMA Connector

Figure 2.3−1 shows the external appearance of the SMA connector used in the actual measurement, along with the corresponding HFSS simulation model developed based on it. To ensure consistency with the real measurement environment, the model was precisely constructed to match the actual connector specifications, including the diameter of the center pin, the thickness of the dielectric, and the contact area between the outer shield and the PCB [22]. The purpose of this model is to accurately account for parasitic effects that may occur at the interface between the transmission line and the SMA connector, thereby improving the overall reliability of the simulation results.

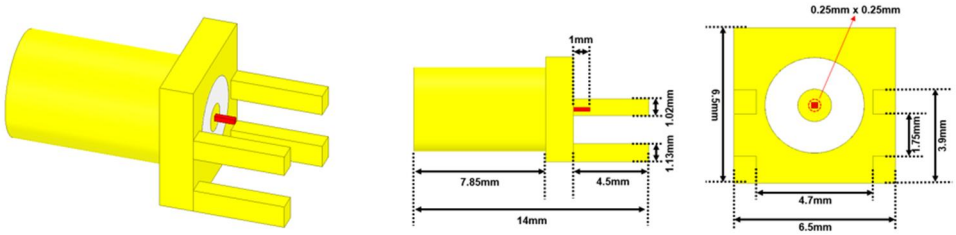


Figure 2.3-1 Appearance of the SMA connector used in the actual measurement

The SMA connector is used as the reference port in system level measurements and must satisfy an accurate characteristic impedance of 50 Ω. Accordingly, in this study, the impedance matching characteristics of the designed SMA model were verified through HFSS simulations, and S-parameter analysis confirmed that the model achieved proper matching at 50Ω. In particular, the reflection coefficient remained below -20 dB, indicating that impedance mismatch at the connector interface is minimal.

Based on this model, it becomes possible to more accurately predict the transmission characteristics at the package to board interface. This modeling approach can also be applied to other connectors or probe based measurement setups in the future and contributes to improving the accuracy of high frequency measurement environments.

2.3.2 Correction for Surface Roughness

To accurately predict the characteristics of high frequency transmission lines, it is essential to consider not only idealized simulation models, but also the surface roughness of metal conductors that arises from actual PCB manufacturing processes. When the surface of a transmission line becomes rough, the electric field distribution at the metal dielectric interface becomes non-uniform, which distorts the field path and directly affects key parameters such as the effective dielectric constant, dielectric thickness, and line capacitance [23]. To account for these effects, this study incorporated actual PCB manufacturing parameters such as plating thickness, surface profilometer data, and copper grain size into the HFSS simulation model. The model was corrected using the parameters D_{k,eff_rough} and C_{rough}, representing the effective dielectric constant and capacitance adjusted for surface roughness. This approach allowed for improved accuracy in predicting the electrical length, insertion loss, and reflection characteristics of the transmission lines, thereby reducing discrepancies between simulation and measurement results. Such correction techniques are especially critical in high frequency regions beyond the X-band, where even minor variations in surface roughness can significantly

affect system performance. Therefore, it is essential to incorporate material properties that reflect surface roughness and apply appropriate correction models during simulation.

2.3.2.1 Theory of Surface Roughness

Figure 2.3-2 shows the actual surface roughness of a PCB, while the right figure shows the modeling approach that accounts for this roughness.

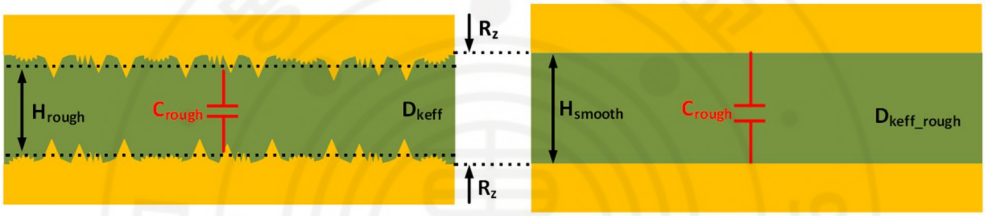


Figure 2.3-2 (a) Actual surface roughness of a PCB, (b) Modeling approach that accounts for roughness

The above parameters follow the equations shown below. First, in the ideal (smooth) case, the capacitance can be expressed as:

$$C_{rough} = D_{keff} \cdot \frac{\varepsilon_0 A}{H_{rough}} \qquad \textbf{(2.3.1)}$$

Where ε_0 is the vacuum permittivity, A is the effective area between conductors, H_{rough} is the effective dielectric height including surface roughness. To maintain the same capacitance while modeling the roughness effect as a correction to the permittivity, we

define a corrected effective dielectric constant, yielding:

$$C_{rough} = D_{keff\_rough} \cdot \frac{\varepsilon_0 A}{H_{smooth}} \quad \textbf{(2.3.2)}$$

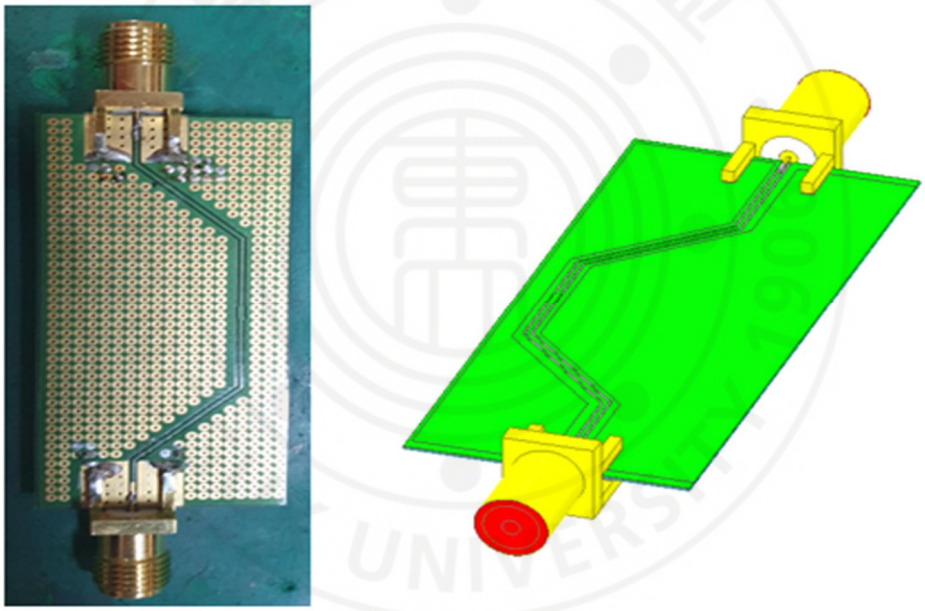
By equating the two expressions, the relationship between the uncorrected and corrected dielectric constants becomes:

$$D_{keff\_rough} = D_{keff} \cdot \frac{H_{smooth}}{(H_{smooth} - 2R_z)} \quad \textbf{(2.3.3)}$$

Where R_z represents the average surface roughness height. This expression indicates that surface roughness effectively reduces the distance between the conductor and dielectric, which increases the effective permittivity needed to maintain the same capacitance. By applying this model, simulation tools such as HFSS or ADS can incorporate roughness corrected dielectric constants D_{k,eff_rough}, allowing for more accurate prediction of electrical behavior. This correction method is especially critical in X-band and higher frequency designs, where even small variations in surface roughness can lead to measurable performance deviations.

2.3.2.2 Comparison of Simulation and Measurement Results

Figure 2.3-3 shows the test PCB fabricated for comparison between the proposed simulation model and actual measurement set-up, along with the external view of the SMA connectors soldered to the board. The actual measurements were performed using a Vector Network Analyzer(VNA), focusing on the comparison of S-parameter characteristics, particularly insertion loss and return loss.



(a) (b)

Figure 2.3-3 (a) Actual measurement set-up, (b) Model with surface roughness

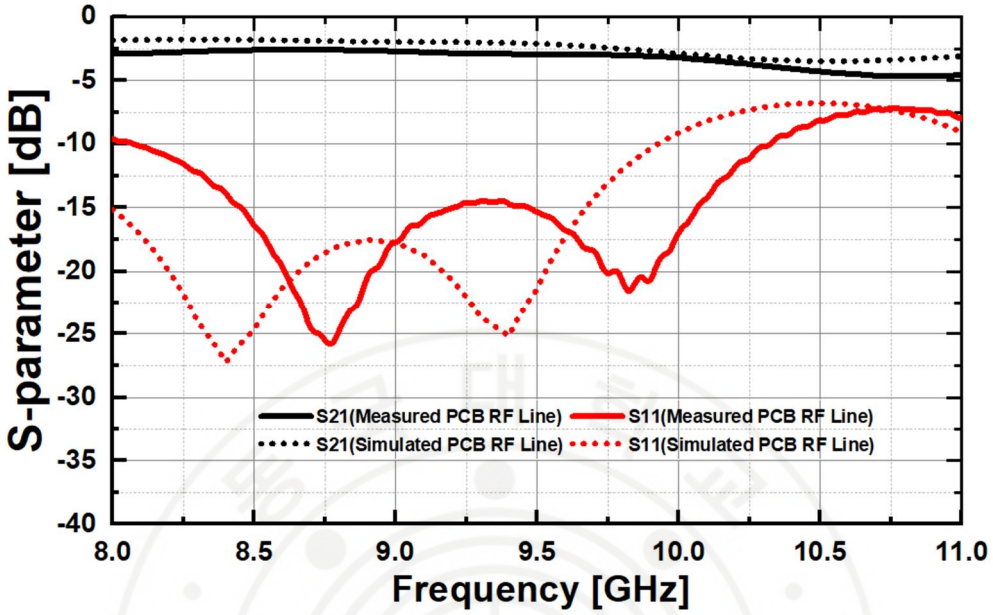


Figure 2.3-4 Comparison between the simulation results without corrected model and the actual measured values

First, the discrepancy between the initial HFSS model without surface roughness correction and the measured results is shown in Figure 2.3-4. Some mismatches were observed in both insertion loss and phase characteristics. This deviation is attributed to the difference in electromagnetic wave propagation and transmission line capacitance caused by metal surface roughness introduced during the PCB manufacturing process. Accordingly, in this study, the previously described correction equations were applied to the simulation to incorporate the effects of PCB surface roughness by adjusting the effective dielectric constant and capacitance. The

comparison between the simulation results using the corrected model and the actual measured values is shown in Figure2.3-5, where a significant reduction in the discrepancy between the two results can be observed.

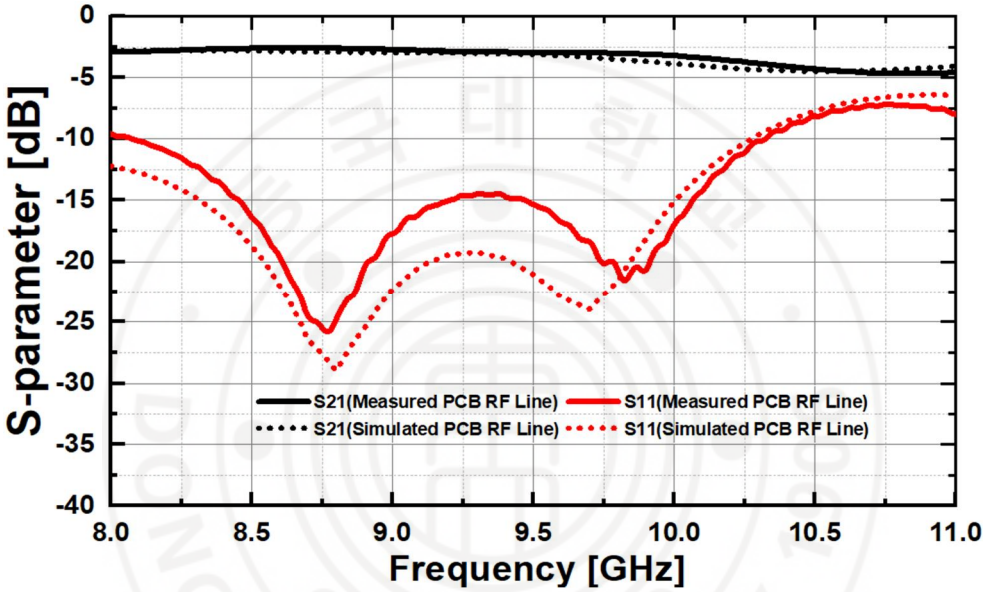


Figure 2.3-5 Comparison between the simulation results with corrected model and the actual measured values

As a result, the application of correction formulas that account for surface roughness was proven to be effective in improving simulation accuracy and provided high reliability in predicting transmission line characteristics at the actual PCB level. This approach is particularly useful for high frequency designs beyond the X-band and can be directly applied to transmission line analysis within SiP structures.

Chapter III. Integrated Simulation Including the Full Package

3.1 Full Package Simulation of Tx

The package structure proposed in 'Chapter 2' was designed to integrate multiple chips at high density within a single package. The performance of this integrated structure must be evaluated not only at the circuit level, but also through full package simulations that account for the complete electromagnetic environment. Since the package behaves as a passive structure from an RF perspective, its performance can be quantitatively assessed using key transmission characteristics such as insertion loss and parasitic inductance. In particular, the combined effects of internal metal routing, via structures, wire bonding, and thermal management components can significantly influence the electrical behavior of the signal path. To accurately capture these effects, this study first extracted the electromagnetic characteristics of the standalone package using HFSS 3D EM simulation, and then performed chip to package co-simulation by integrating the individual functional blocks into the model. This approach allows for the inclusion of chip to package interconnection effects that can occur in real world conditions and

provides a comprehensive prediction of the overall RF performance of the SiP structure.

3.1.1 Small signal simulation results of Tx

Figure 3.1−1 shows the simulation results of S−parameter used to evaluate the small−signal characteristics of the transmitter circuit. The performance was compared between the bare chip condition and packaged full SiP structure.

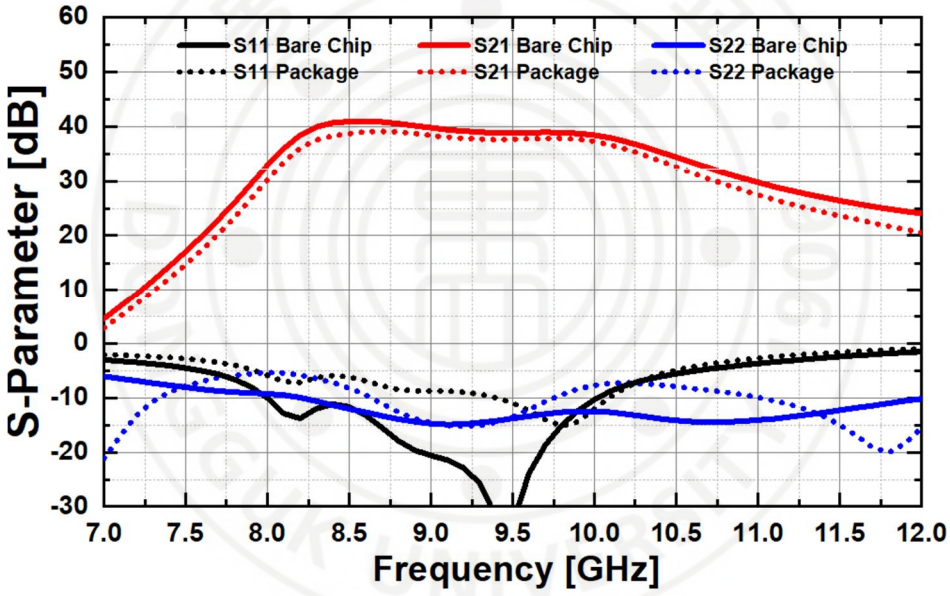


Figure 3.1-1 Comparison between the small-signal simulation results Bare chip and packaged full SiP

Table 3.1-1 Comparison between the small-signal simulation results Bare chip and full SiP

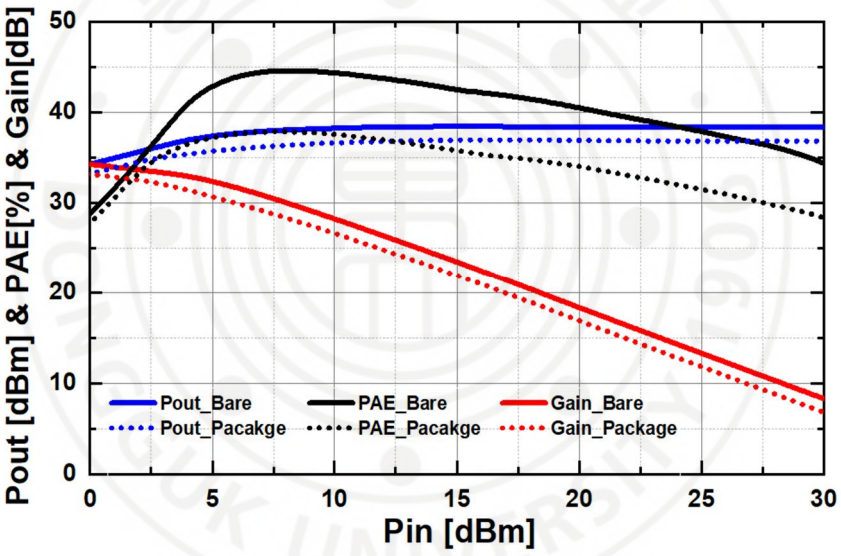
	Bare Chip			Package		
Frequency	**9GHz**	**9.5GHz**	**10GHz**	**9GHz**	**9.5GHz**	**10GHz**
S11(dB)	-20.6	-33.2	-10.31	-8.72	-10.96	-12.03
S21(dB)	39.78	38.86	38.4	38.35	37.67	37.29
S22(dB)	-14.74	-13.78	-12.5	-14.6	-13.45	-7.66

According to the simulation results, the bare chip exhibited excellent input matching with an S11 of −33.2dB at 9.5 GHz, while the packaged state still maintained a reasonable input matching level of −10.96dB. The output matching, S22 was also comparable, showing −13.78dB for the bare chip and −13.45dB for the package. On the other hand, the insertion loss, S21 slightly decreased due to the packaging. For instance, at 9.5 GHz, the gain dropped from 38.86dB in the bare chip to 37.67dB in the packaged structure, indicating a loss of approximately 1.2dB. This degradation is presumed to be caused by external factors such as the SMA connector, bonding wires, and internal routing within the package. However, the 1.2dB loss is considered to be well controlled, especially given the packaging environment in the X−band, indicating that the overall package design is effective in suppressing high frequency losses.

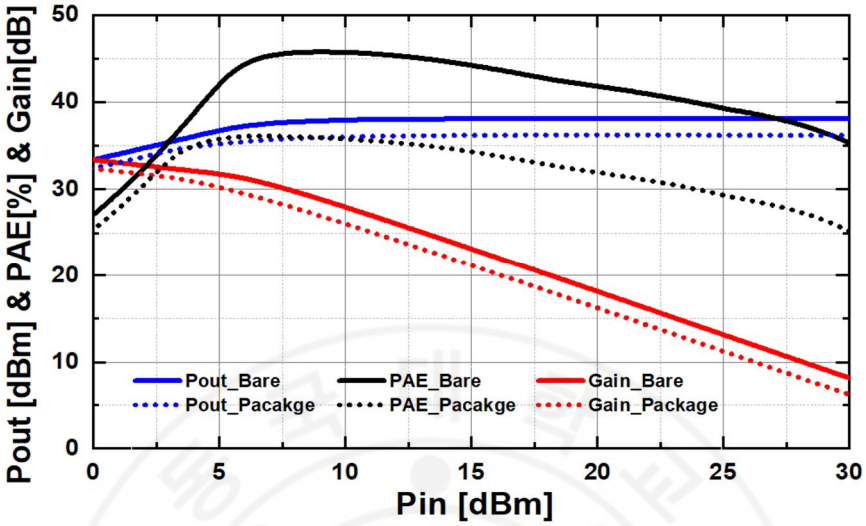
These results underscore the importance of quantifying insertion loss within the package structure and highlight the necessity of design optimization to minimize high frequency performance degradation during the packaging stage.

3.1.2 Large signal simulation results of Tx

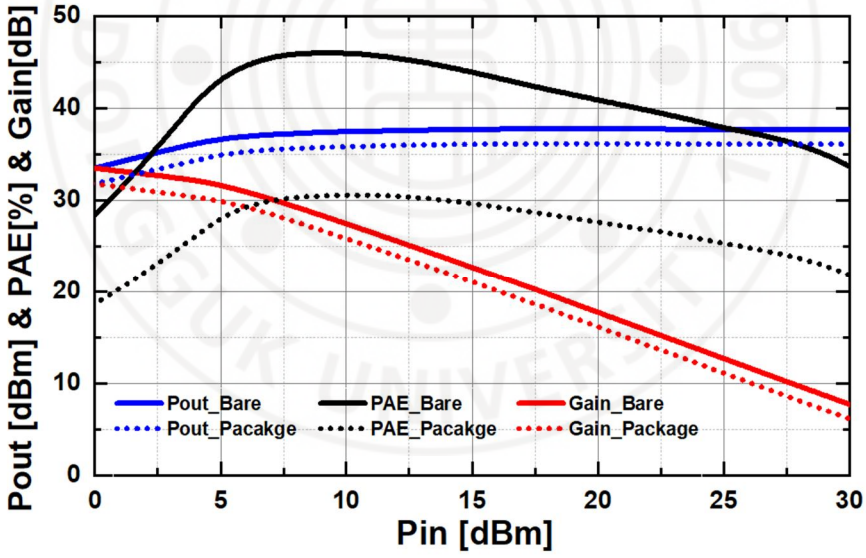
Figure 3.1-2 shows the large-signal performance of the transmitter circuit, showing the variations in output power (Pout), gain, and power-added efficiency (PAE) with respect to the input power (Pin). The measurements were conducted under identical conditions to compare the performance between the bare chip and the packaged full SiP structure.



(a)



(b)



(c)

Figure 3.1-2 Comparison between the large-signal simulation results Bare chip and packaged full SiP

Table 3.2-2 Comparison between the large-signal simulation results Bare chip and full SiP

9GHz				9.5GHz				10GHz			
Pout[dBm]		PAE[%]		Pout[dBm]		PAE[%]		Pout[dBm]		PAE[%]	
Bare Chip	PKG	Bare Chip	PKG	Bare Chip	PKG	Bare Chip	PKG	Bare Chip	PKG	Bare Chip	PKG
38.3	36.8	44.5	37.8	38.1	36.2	45.6	36.1	37.6	36.1	45.9	30.5

At 9.5 GHz, the bare chip achieved a peak output power of 38.15 dBm and a maximum PAE of 45.6%, whereas the packaged version showed a slightly degraded performance with 36.2 dBm of output power and 36.1% PAE. This corresponds to approximately a 2 dB drop in output power and a 9.5% reduction in efficiency, which can be attributed to additional insertion loss and parasitic effects introduced by the SMA connectors, bonding wires, and internal transmission lines within the package. Nevertheless, maintaining 36.2 dBm of output power and 36.1% PAE in the packaged structure is still considered a favorable result, indicating that the high frequency packaging was relatively well designed. These findings highlight the critical importance of packaging technology in preserving high output power and efficiency in real world system implementations. Figure 3.1−3 shows the variation in drain current with respect to the input power (Pin), comparing the current consumption characteristics between the bare chip and the packaged structure.

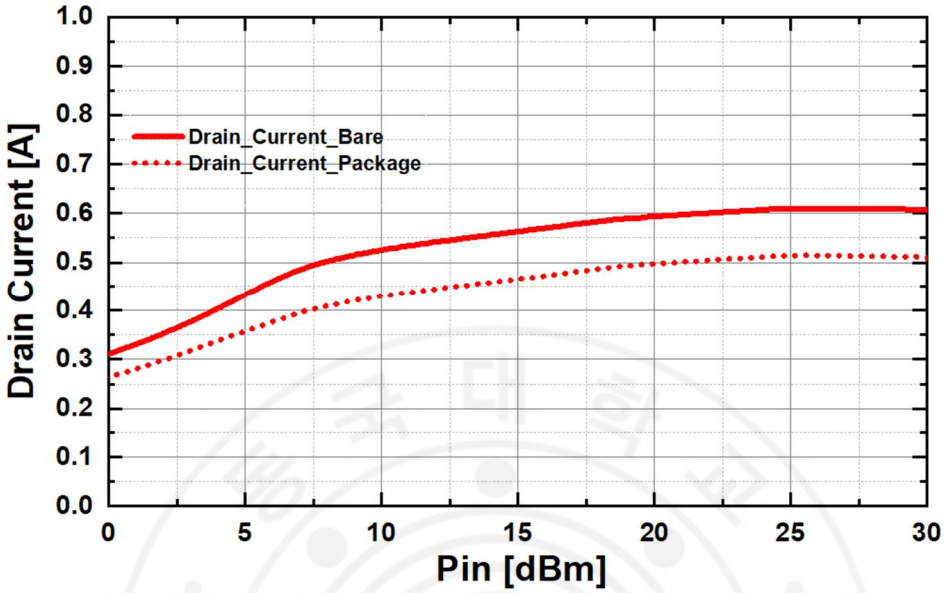


Figure 3.1-3 Comparison between the drain current simulation results Bare chip and packaged full SiP

Across the entire input power range, the bare chip exhibits higher drain current than the packaged version. This trend aligns with the previously observed reductions in output power and power-added efficiency, confirming that the degraded output performance due to packaging results in lower current consumption at the same input power level. Specifically, near the maximum input power, the bare chip draws approximately 0.66 A, whereas the packaged structure draws around 0.58 A. This difference is primarily attributed to the insertion loss and additional impedance introduced by the internal transmission paths within the package.

3.2 Full Package Simulation of Rx

The small-signal characteristics and noise figure of the receiver circuit could not be independently simulated or measured in the bare chip state. This is because the Rx path was designed by an external academic institution, and the design data was not accessible. Therefore, in this section, the performance of the Rx block is evaluated based solely on the measurement results obtained from the packaged full SiP structure.

3.2.1 Small signal simulation results of Rx

Figure 3.2-1 shows the simulation results of S-parameter used to evaluate the small-signal characteristics of the receiver circuit.

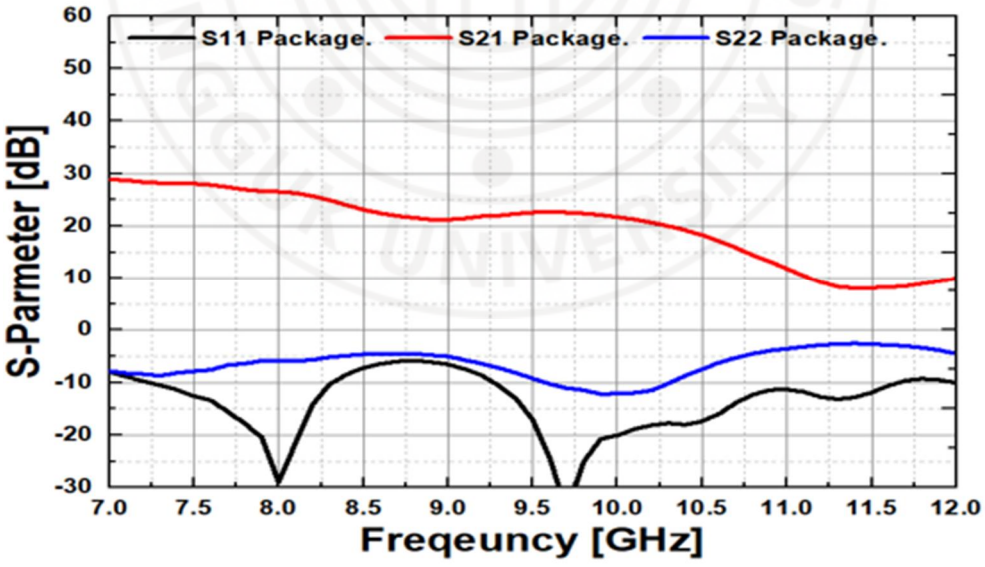


Figure 3.2-1 Small-signal measurement for Rx of SiP

The input matching characteristic, S11 exhibits deep dips of approximately −25dB near 8.3 GHz and −28dB near 9.6 GHz, indicating excellent matching at these frequencies. Across the entire band, S11 remains mostly below −10dB, demonstrating stable input matching performance. The output matching, S22 also stays below 10dB over the full frequency range, confirming that the output port maintains good matching as well. S21 remains around 22~26dB in the central frequency range of 8–10 GHz and reaches up to nearly 28 dB. This gain performance indicates that the receiver circuit provides sufficient amplification of the input signal. Overall, the receiver maintains good matching and high gain characteristics even in the packaged state, suggesting strong performance in practical system integration environments.

3.2.2 Noise Figure simulation results of Rx

Figure 3.2-2 shows the frequency dependent noise figure (NF) of the receiver circuit.

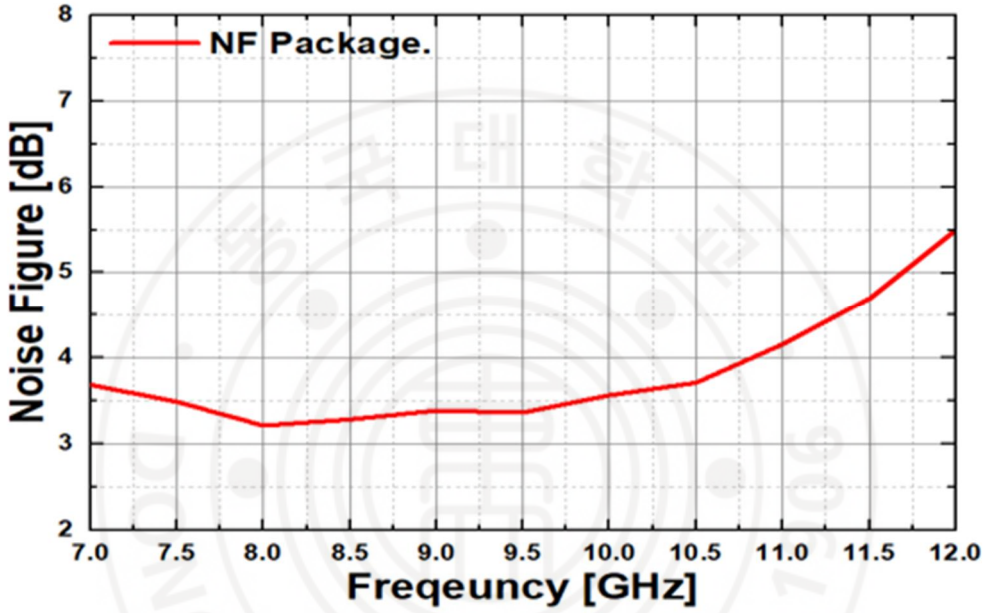


Figure 3.2-2 Noise figure measurement for Rx of SiP

Across the entire 7-12 GHz band, the receiver demonstrates relatively stable NF characteristics, particularly maintaining a low level of approximately 3.2-3.5dB in the primary operating range of 8-10 GHz. In the lower frequency region near 7.5 GHz, the NF starts at around 3.7dB and decreases to approximately 3.2dB within the 8-10 GHz range, exhibiting a relatively flat response. Beyond 10 GHz, the noise figure gradually increases with frequency, reaching

approximately 5.5dB at 12 GHz. This trend is likely due to transmission loss and parasitic elements present in the packaging structure that become more pronounced at higher frequencies.

In conclusion, the receiver maintains a low noise figure within the main operating band of 8–10 GHz, suggesting that it can meet the high–sensitivity requirements of communication and radar systems.

3.3 Measurement Set-Up of SiP QFN Package

This measurement plan describes the experimental setup for evaluating the small-signal and large-signal characteristics of the transmitter path in the SiP QFN package.

3.3.1 Components of Evaluation Board

This measurement plan describes the experimental setup for evaluating the small-signal and large-signal characteristics of the designed SiP QFN Package at the transmitter path. The measurement is conducted to precisely verify the performance of the RF circuit, and it is especially critical to ensure power supply stability when using high power devices based on GaN and GaAs technologies. Since these devices operate at high voltages, they are susceptible to oscillation or noise coupling within the system due to unstable power supply or external interference. To prevent such issues and secure circuit stability, de-Qing resistors and bypass capacitors must be inserted in the power supply lines. The position of SMT capacitors and resistors are shown in Figure 3.3-1. Table 3.3-1 summarizes list of the components value of SMT capacitors and resistors.

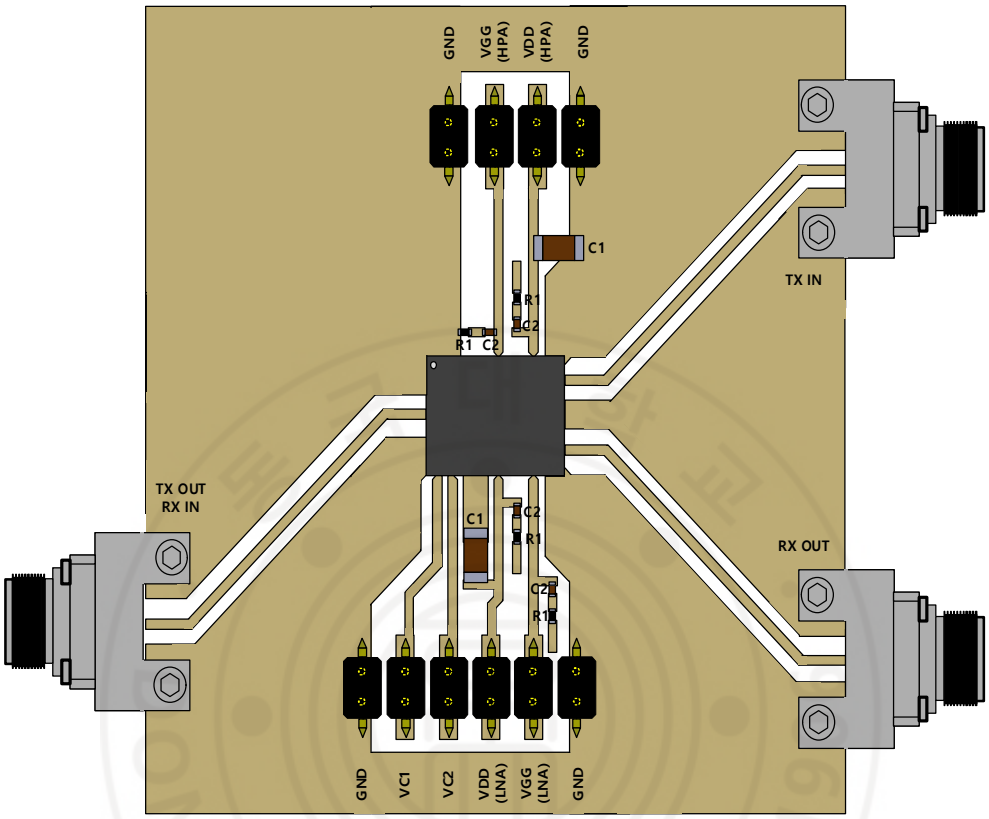


Figure 3.3-1 Position of SMT capacitors and resistors

Table 3.3-1 Components value of SMT capacitors and resistors

Ref. Des.	Component	Value
C1	SMT Cap	1206, 10uF, +/-20%, 50V
C2	SMT Cap	0402, 0.1uF, +/-10%, 50V
R1	SMT Res	0402, 10OHM, 5%

3.3.2 Measurement Set-Up of Evaluation Board

For small-signal characterization, Vector Network Analyzer (VNA) is used to measure S-parameters. For large-signal measurements, an Agilent 83623B signal generator is used to provide the desired input power at each frequency. The corresponding output power is measured using the Agilent E4407B spectrum analyzer.

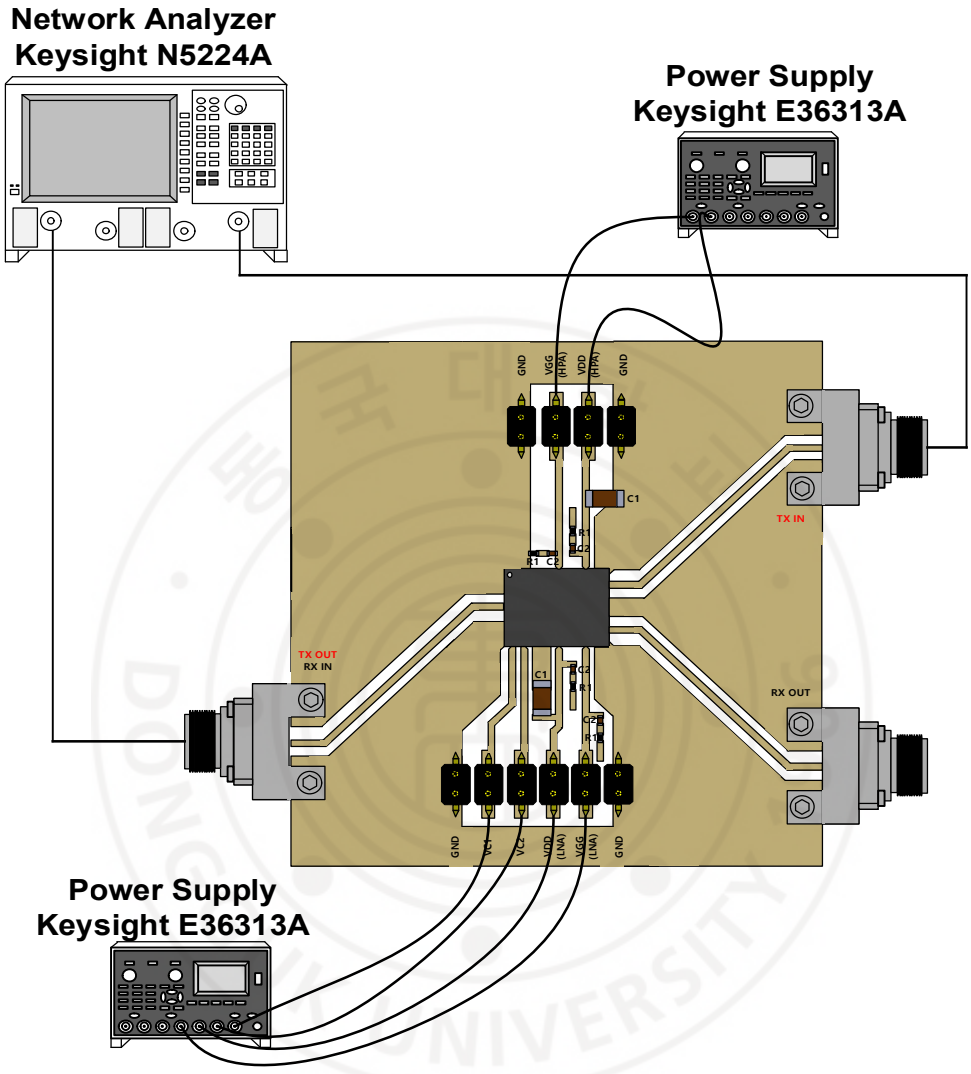


Figure 3.3-2 Small-signal measurement set-up for Tx of SiP

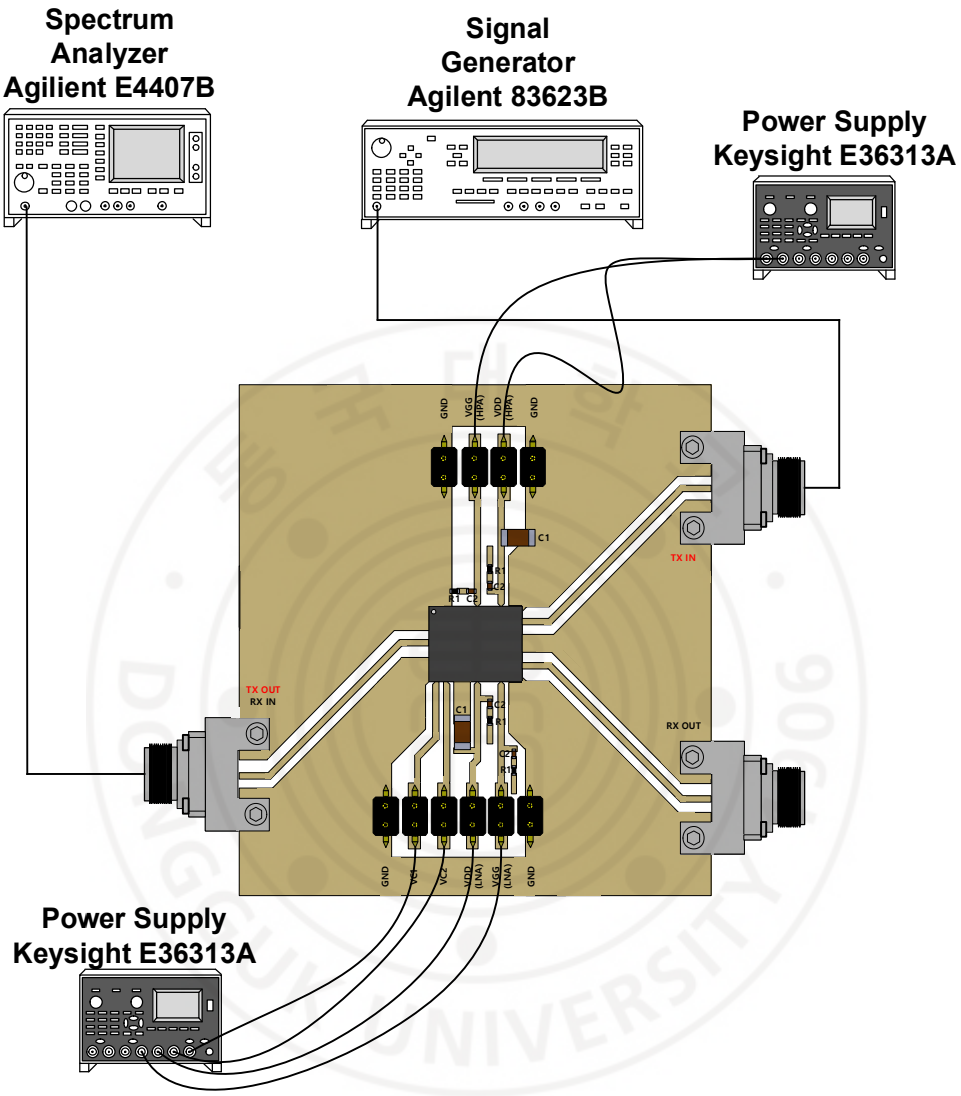


Figure 3.3-3 Large-signal measurement set-up for Tx of SiP

Chapter Ⅳ. Design of X-band Land-Grid-Array(LGA) Package

4.1 Core Structural Design of X-band LGA Package

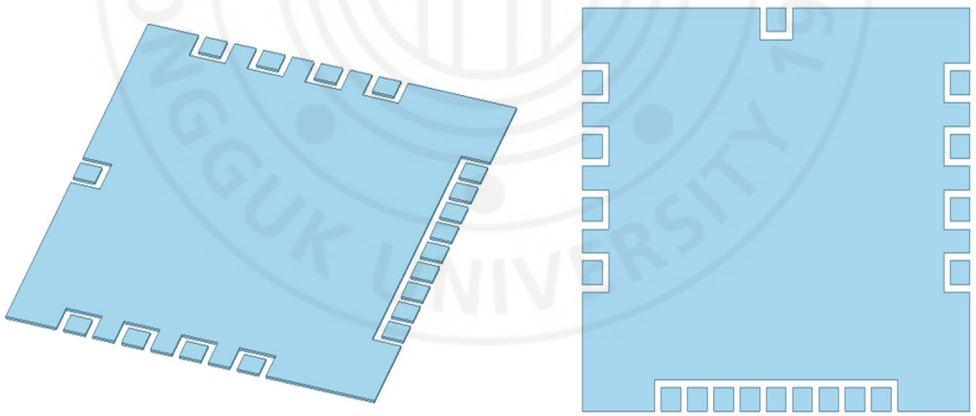
Land Grid Array (LGA) package offers a favorable structure for precise signal path control required in high speed signal transmission and multi-channel integrated systems. In this study, a 4-channel Multi-functional Chip (MFC) fabricated using the TSMC 65nm process is embedded within LGA package. Each channel includes a phase shifter and an attenuator. In such a configuration, it is essential to minimize the variations in inductance and signal propagation delay among the four channels to ensure precise matching of phase and attenuation characteristics across all channel [24].

LGA package connects to the PCB via flat metal pads instead of solder balls, which shortens the interconnection length and reduces parasitic inductance. This contributes to consistent signal delay across channels. Furthermore, the high input/output (I/O) density supported by the LGA structure enables symmetric and repeatable routing for all four channels, providing design flexibility. These characteristics play a critical role in maintaining circuit integrity and operational stability, especially in systems like the MFC chip, where

channel-to-channel matching of phase and attenuation directly impacts overall system performance.

4.1.1 Characteristics of Each Metal Layer

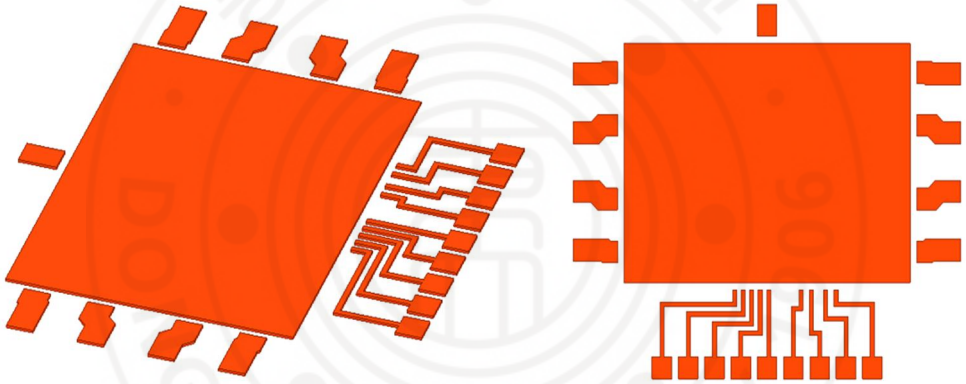
Considering the complexity of the 4-channel MFC, the package board used for the LGA package was simplified by adopting a conventional 2 layers structure with MSTL based routing. In this structure, the bottom copper layer, 'Metal 1' serves as the ground plane for the MSTL signal traces on the upper layer, 'Metal 2'. Figure 4.1-1 shows a 3D-EM model based on HFSS, designed using the structure of 'Metal 1', and is used to verify the current distribution and shielding effectiveness of the ground plane.



(a) (b)

Figure 4.1-1 3D-EM Model Using HFSS ('Metal 1') ; (a) 3D view of 'Metal 1', (b) Top views of 'Metal 1'

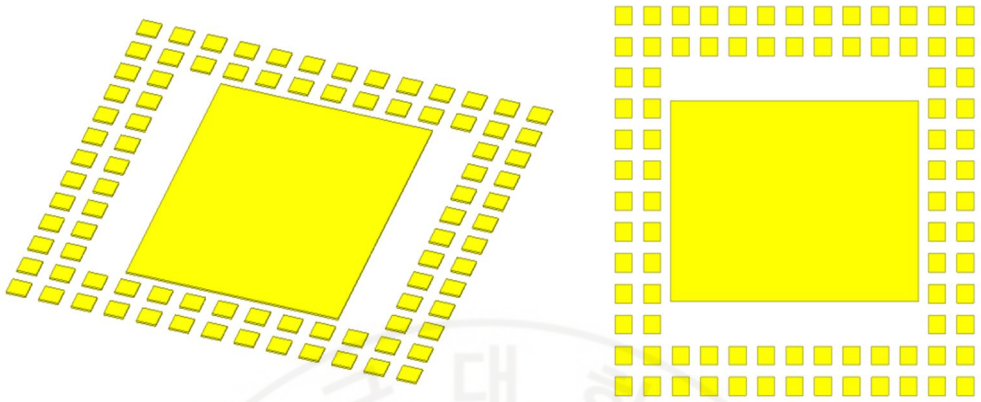
The second copper layer, 'Metal 2' contains the routing for supplying DC bias to the VDD of the 4-channel MFC and the SPI module, as well as the signal traces for transmitting the output signals of the PA and LNA for each channel. Figure 4.1-2 shows a 3D-EM model based on HFSS, designed using the structure of 'Metal 2', which was used to evaluate coupling with adjacent layers, the adequacy of the signal line structure and to ensure power integrity.



(a) (b)

Figure 4.1-2 3D-EM Model Using HFSS ('Metal 2') ; (a) 3D view of 'Metal 2', (b) Top views of 'Metal 2'

In the LGA package, the bottom copper layer is not directly soldered to the PCB. Instead, a land grid composed of solder bumps is located beneath it for connection to the PCB. Figure 4.1-3 shows the 3D EM model of the land grid simulated using HFSS.



(a) (b)

Figure 4.1-3 3D-EM Model Using HFSS (‘Land Grid’) ; (a) 3D view of ‘Land Grid’, (b) Top views of ‘Land Grid’

4.1.2 4−Channel Inductance and Delay Matching

One of the most critical design considerations in the LGA package integrating a 4−channel MFC is ensuring that the signal propagation delay across all channels is identical. This guarantees that the phase measured at each channel remains perfectly aligned. Even slight discrepancies in delay or phase between channels can significantly degrade overall system performance, particularly in applications where precise phase alignment is essential. To prevent such issues, the internal routing of the package is carefully designed so that all channels exhibit matching inductance and signal propagation characteristics, thereby ensuring precise alignment of phase and attenuation across the four channels. Figure 4.1−4 shows the overall

pad layout of the 4−channel MFC, which is arranged symmetrically to support balanced signal routing for all channels. This pad configuration plays a crucial role in facilitating uniform signal paths within the LGA package, minimizing variations in delay and inductance among channels.

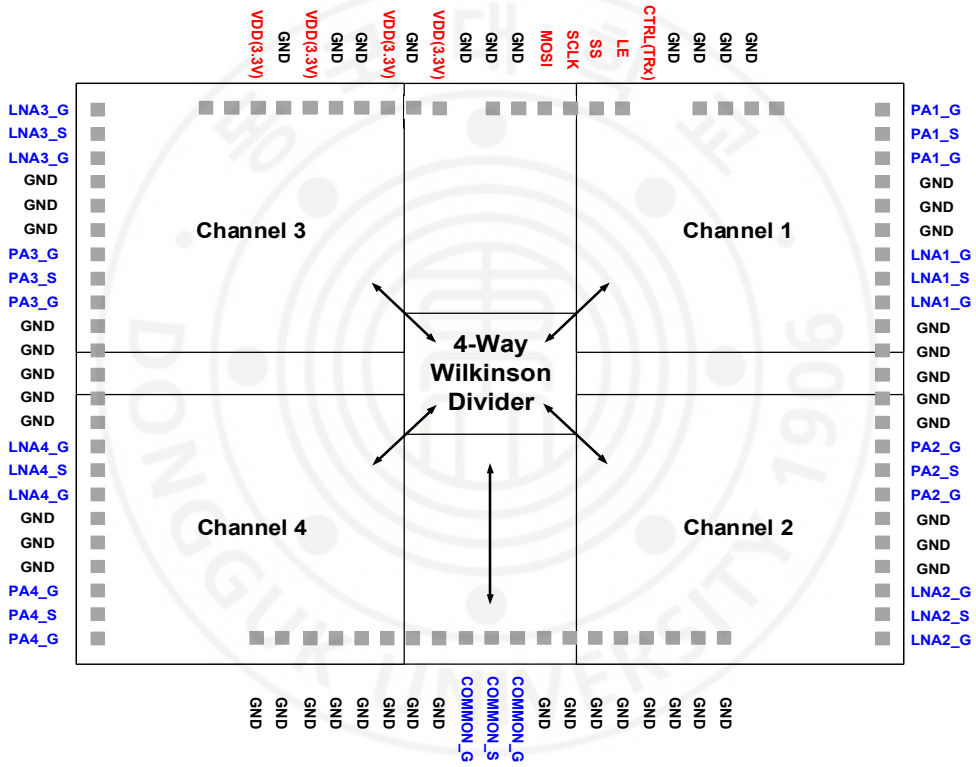


Figure 4.1-4 4-Channel MFC Pad Layout

Considering the role of the package board routing for transmitting the PA and LNA output signals of the 4-channel MFC, it is essential to maintain signal integrity through 50Ω impedance matching. Therefore, 'Metal 2' is designed as an MSTL based routing layer, with 'Metal 1' directly beneath it serving as the ground plane. Figure 4.1-5 shows the lumped port simulation setup performed using HFSS.

(a) (b)

Figure 4.1-5 3D-EM Model Using HFSS (‘Board Routing line’) ; (a) for transmitting the signals of LNA1, PA2, PA3, and LNA4, (b) for transmitting the signals of PA1, LNA2, LNA3, and PA4

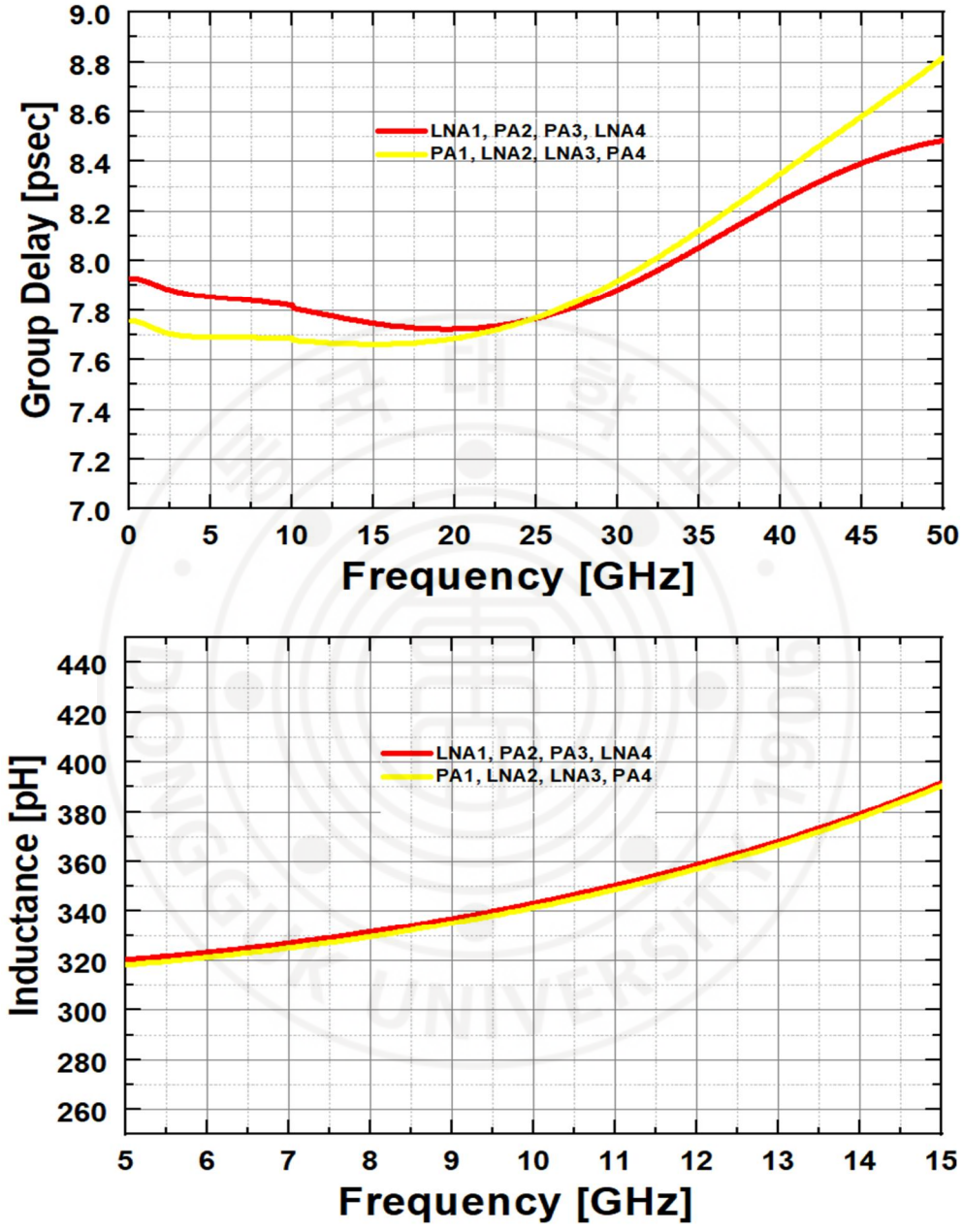


Figure 4.1-6 Simulation results of Group Delay and inductance for each routing line

Figure 4.1-6 shows the results of the group delay and inductance simulations performed with equalized routing lengths in the package board. These simulations were conducted to verify the consistency of delay time and inductance characteristics across channels and to evaluate the signal path properties of the output routes for the 4-channel MFC chip within the LGA package. In X-band, the group delay for the package board routing transmitting the output signals of LNA1, PA2, PA3, and LNA4 was approximately 7.8psec, while the group delay for the routing transmitting the output signals of PA1, LNA2, LNA3, and PA4 was measured at 7.7psec. The minimal group delay variation between these two routes confirms that the uniformity of delay time required for phase alignment across channels has been successfully achieved. Furthermore, in terms of inductance characteristics, the two routing paths exhibited approximately 341 pH and 343 pH, respectively, indicating that the equalization of routing lengths and inductance matching were successfully implemented. These results are critical for ensuring phase and attenuation alignment across the four channels, which is vital for stable performance in high frequency applications.

4.2 Integrated Design of LGA Package

In LGA package, overall system performance is influenced not only by the characteristics of individual circuit blocks but also by system level interactions. When a multi-channel MFC chip with varying operating conditions and electrical properties is integrated on a single substrate, factors such as parasitic coupling, return path interference, and common ground noise can degrade signal quality and system stability. Therefore, simulations limited to individual blocks are insufficient to ensure the reliability of the complete LGA package. A comprehensive full package 3D electromagnetic simulation is essential to account for the interactions among all components. This is particularly critical in high frequency communication systems, where even minor structural imbalances can lead to impedance mismatches, increased insertion loss, and unintended resonances. For this reason, accurate EM based validation at the package level must be performed prior to fabrication.

4.2.1 Structure of Integrated LGA Package

Figure 4.2−1 shows the chip placement and pad layout of the LGA Package proposed in this study.

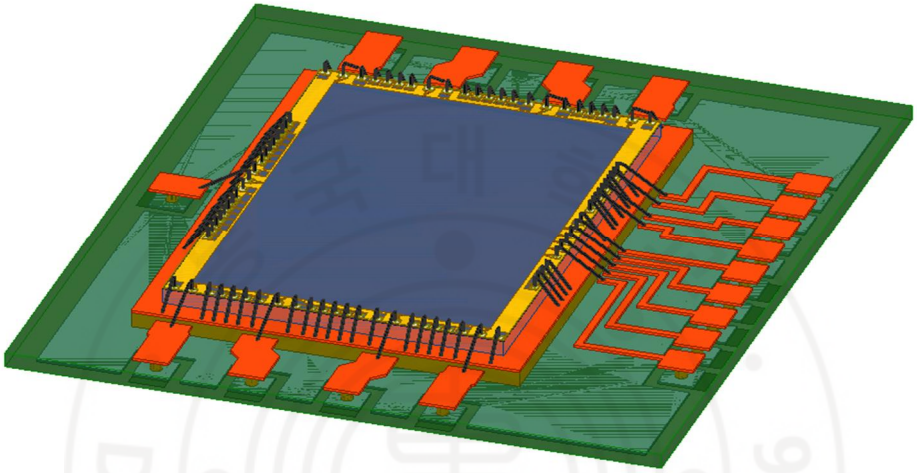


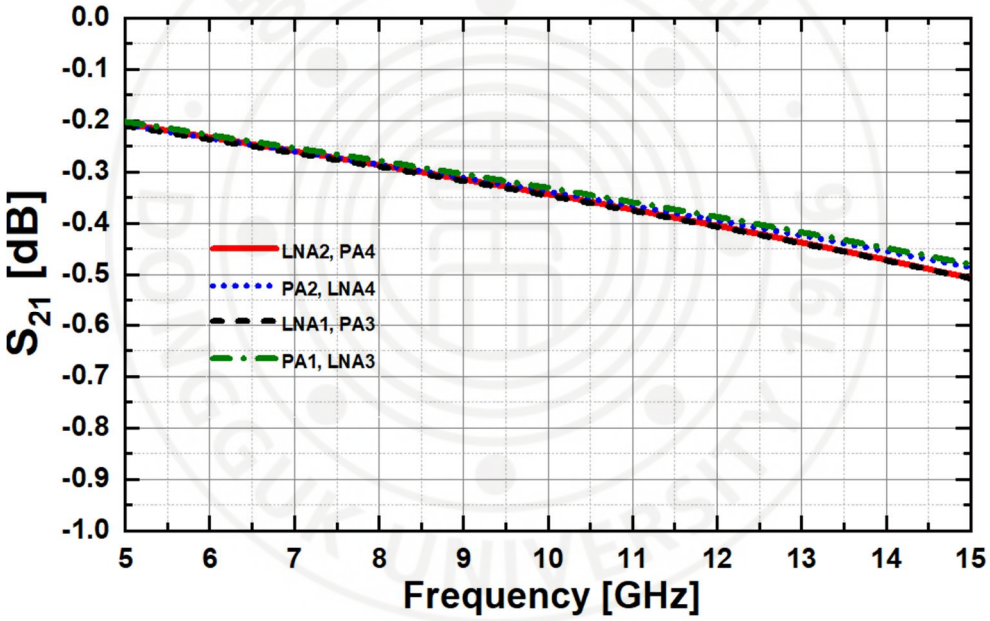
Figure 4.2-1 Chip placement and layout of the LGA Package

On the top metal layer of the package, a 4−channel MFC fabricated using TSMC's 65nm CMOS process is placed. The chip is 4 mm × 3 mm, and due to the limited available area, an efficient layout and structural design are essential to minimize signal interference. The entire package is implemented as a compact, module with dimensions of 6.5 mm × 5.5 mm, optimized for high frequency communication systems requiring miniaturization and high integration.

4.2.2 Simulation Results of Integrated LGA Package

Figure 4.2-2 shows the simulation results for insertion loss, inductance, and group delay of the proposed integrated package structure. In the X-band, the insertion loss remains below -0.4 dB across all signal paths, exhibiting minimal variation between different routes. This indicates that the internal routing of the package is effectively designed to maintain uniform transmission characteristics across channels. For inductance, values range from approximately 700 to 1000 pH across the frequency band, showing a gradual increase as frequency rises. Among the routes, the PA1, LNA3 path exhibits the highest inductance, likely due to its relatively longer routing lines or structural factors contributing additional parasitic elements. In contrast, the LNA1, PA3 path demonstrates the lowest inductance, with the overall variation between paths controlled within approximately 50pH. Regarding group delay, all signal paths fall within a range of 10.26 to 10.44psec with the maximum variation between channels being around 0.18 psec. The PA1, LNA3 path shows the highest group delay, while the LNA1, PA3 path has the lowest. These differences reflect the slight variations in signal propagation time caused by differences in routing length and layout structure, but remain well controlled to ensure phase alignment

among channels. These simulation results confirm that the proposed package structure maintains signal integrity by minimizing variations in insertion loss, inductance, and group delay even in high frequency signal transmission scenarios. Such performance is essential in multi-channel high density systems, where precise matching of phase and attenuation characteristics between channels is critical.



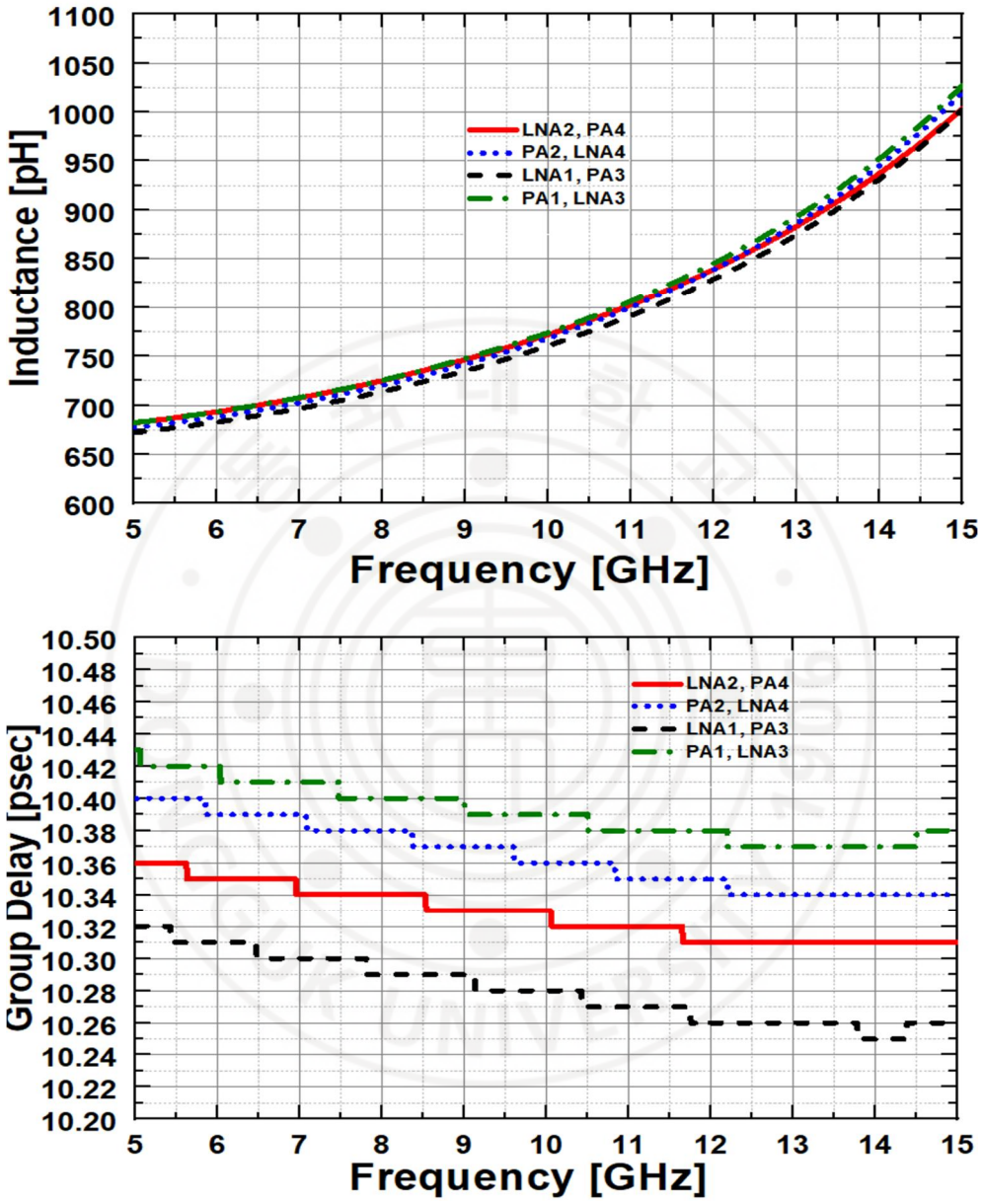


Figure 4.2-2 Simulation results of the insertion loss, inductance and Group delay for the integrated package structure

4.3 Measurement Set-Up of LGA Package

This measurement plan describes the experimental setup for evaluating the small-signal and large-signal characteristics of the transmitter path in the LGA package.

4.3.1 Components of Evaluation Board

The measurements are conducted to precisely verify the performance of the RF circuit, and ensuring power supply stability is particularly important in high frequency environments. In such systems, oscillation or noise coupling may occur due to power supply noise or external interference, which can degrade circuit stability. To prevent these issues and maintain stable operation, bypass capacitors are inserted in the power supply lines. Additionally, to supply a stable 2.5 V to the SPI module, a voltage divider circuit using resistors is implemented. This voltage divider ensures consistent control voltage even in high frequency conditions, contributing to overall power integrity within the system. The placement of SMT capacitors and resistors is illustrated in Figure 4.3-1, and Table 4.1-1 summarizes the component values of the SMT capacitors and resistors used.

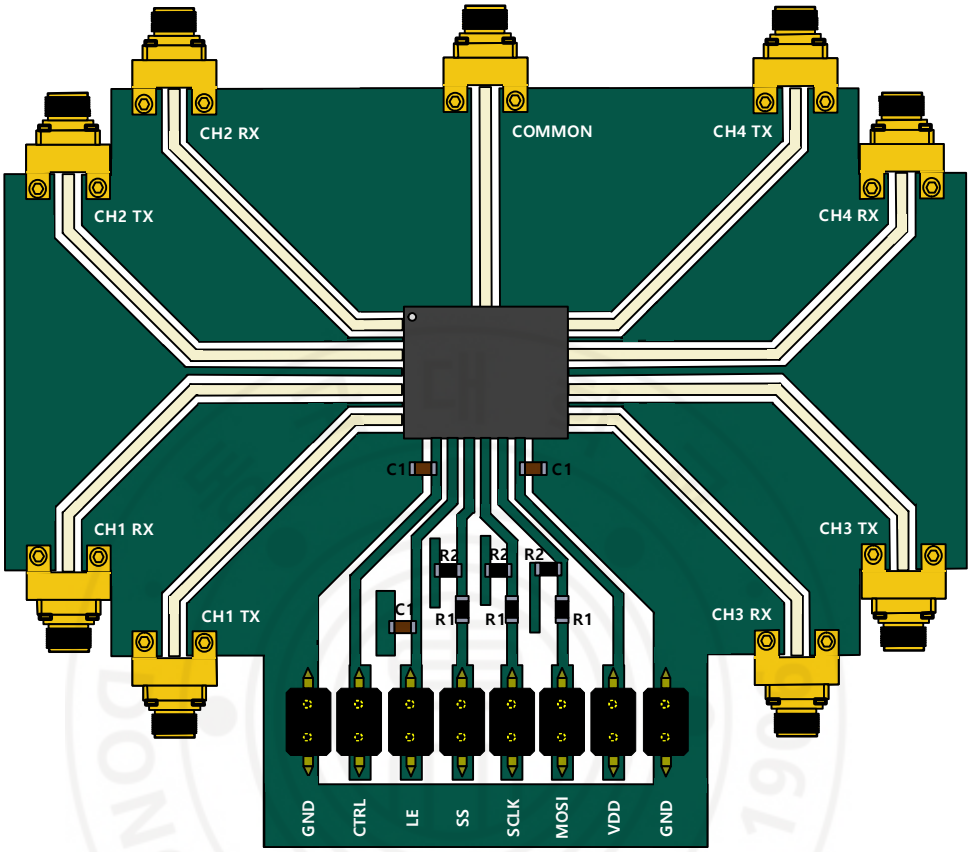


Figure 4.3-1 Position of SMT capacitors and resistors

Table 4.3-1 Components value of SMT capacitors and resistors

Ref. Des.	Component	Value
C1	**SMT Cap**	**0805, 10uF, +/-20%, 50V**
R1	**SMT Res**	**0805, 10KOHM, 5%**
R2	**SMT Res**	**0805, 20KOHM, 5%**

4.3.2 Measurement Set-Up of Evaluation Board

This measurement focuses on evaluating the small-signal and large-signal characteristics of the transmitter (TX) path in Channel 1 of the LGA package, and the same measurement methodology can be applied to the remaining three channels (Channels 2, 3, and 4) for consistent performance validation. For small-signal characterization, a Vector Network Analyzer (VNA) is used to measure the S-parameters, including insertion loss and return loss, which are critical for verifying impedance matching and signal transmission efficiency in the TX path. For large-signal characterization, an Agilent 83623B signal generator provides the desired input power at each frequency to the input port of Channel 1's TX path, and the corresponding output power is measured using an Agilent E4407B spectrum analyzer. This process evaluates output power levels, spectrum quality, and nonlinear characteristics of the transmitter. The measurement setup is specifically designed to accurately assess the high frequency performance of the TX path in the LGA package, ensuring reliable operation through key metrics such as insertion loss, output power, and spectral distortion. The same procedure can be replicated for Channels 2, 3, and 4 to verify uniform performance across all channels.

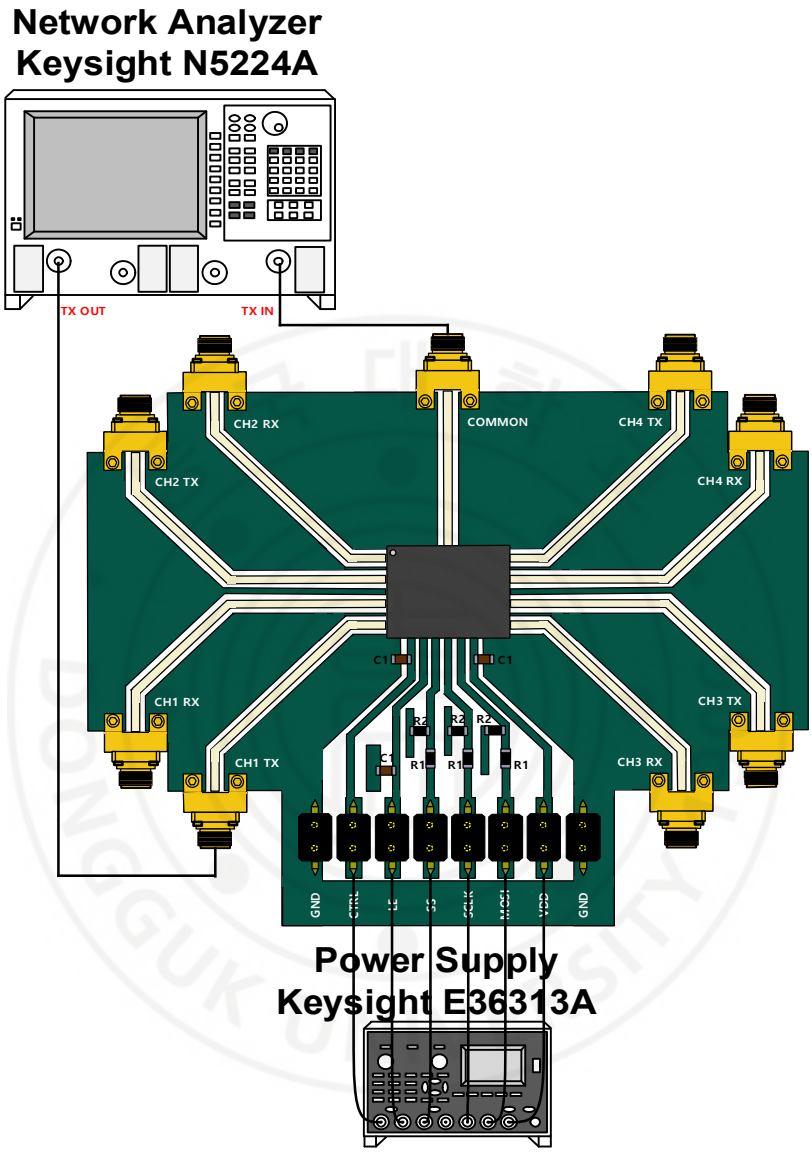


Figure 4.3-2 Small-signal measurement set-up for Tx of LGA Package

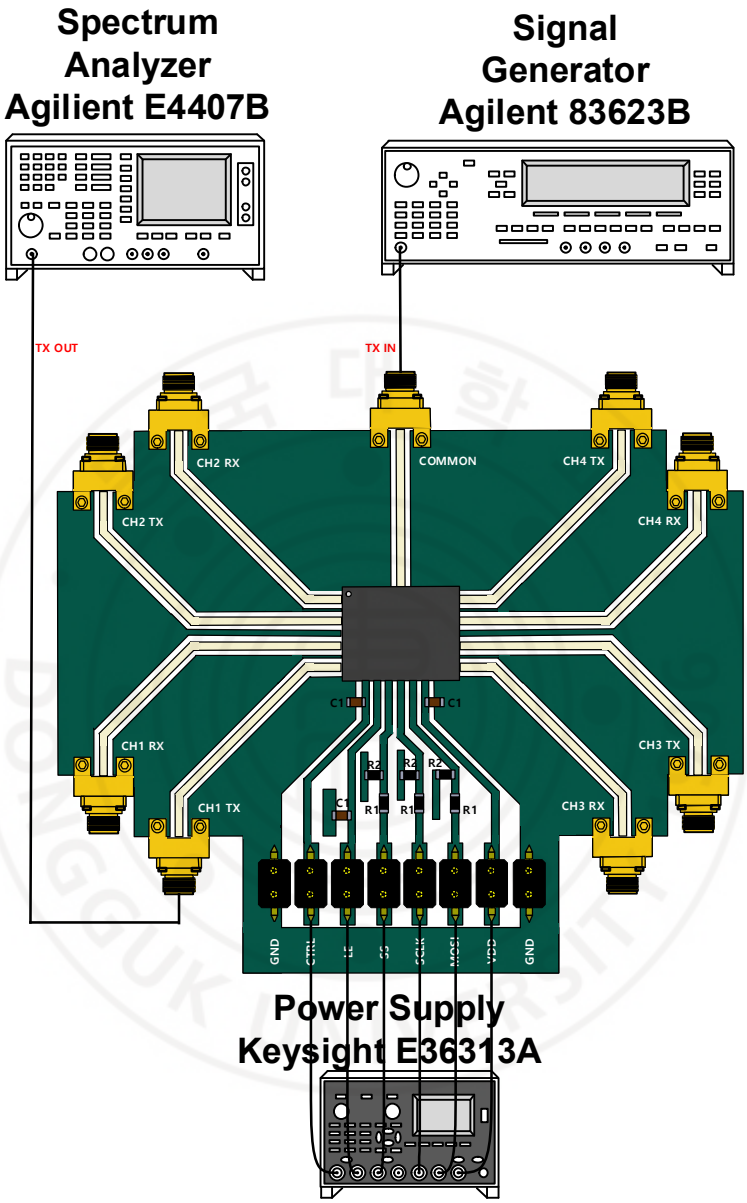


Figure 4.3-3 Large-signal measurement set-up for Tx of LGA Package

Chapter Ⅴ. Conclusion

This thesis presents a modeling and optimization framework for X-band System-in-Package (SiP) aimed at minimizing insertion loss and inductance in high frequency RF circuits. To achieve this, 3D electromagnetic simulations were conducted to evaluate the electrical performance of the proposed package structure, with particular focus on via configuration and wire-bonding design. The simulation results showed strong correlation with measurement data, validating the effectiveness of the modeling approach. Additionally, a calibration technique was introduced to reduce discrepancies between simulation and measurement, significantly improving model reliability. The final SiP design achieved low insertion loss and stable inductance across the 8-12 GHz band, supporting high quality signal transmission suitable for X-band applications. Furthermore, effective design strategies were proposed to minimize parasitic effects introduced during packaging, ensuring stable RF performance in real world environments. In addition, this study presents a high frequency optimization methodology for Land-Grid-Array (LGA) package structures. Leveraging the low parasitic inductance, short interconnection lengths, and high I/O density of the LGA architecture,

the proposed design ensures channel to channel path symmetry and delay matching, which are critical for multi-channel transceiver systems to maintain precise phase and attenuation alignment. A 4-channel Multifunction Core (MFC) chip fabricated using TSMC's 65nm CMOS process was integrated into the LGA package, and its performance was optimized through 3D EM simulation and experimental validation. This approach successfully minimized variations in insertion loss, inductance, and group delay across channels, ensuring signal integrity in high frequency environments. The proposed LGA package optimization methodology is applicable beyond the X-band, offering broad utility across various frequency ranges and contributing to the performance enhancement and commercialization of next generation high frequency RF packaging technologies. Together, the SiP and LGA optimization frameworks presented in this work provide a comprehensive approach that enhances accuracy, efficiency, and reliability, supporting the advancement of future RF packaging solutions.

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국문 초록

집적 회로 기술의 지속적인 발전에도 불구하고, 트랜지스터의 소형화는 한계에 도달하였으며, 이에 따라 배선 지연 및 고전력 소비와 같은 문제가 발생하고 있다. 이러한 한계를 극복하기 위해 기존 반도체 공정을 넘어서는 첨단 패키징 기술이 핵심 솔루션으로 주목받고 있다. 특히, 패키지 내부의 와이어 본딩 및 비아 구조 최적화는 삽입 손실과 인덕턴스를 효과적으로 저감하는 데 필수적이다. 고주파(RF) 회로, 특히 X-대역(8-12 GHz)에서 신호 전송 성능을 극대화하기 위해서는, 패키지 설계 시 더욱 정밀한 시뮬레이션 및 측정 기법이 요구된다. 이를 위해 기존 패키징 기술과는 차별화된 접근이 필요하며, RF 패키지의 특성에 맞춘 구조적 최적화가 중요하다. 본 논문에서는 X-대역 RF 패키지의 성능 향상을 위해 System-in-Package (SiP) 구조의 정밀한 시뮬레이션 및 모델링을 수행하였다. 이를 위해 3차원 전자기(EM) 시뮬레이션을 통해 삽입 손실과 인덕턴스 특성을 고정밀로 분석하였고, 시뮬레이션 결과와 실측 데이터를 비교하여 보다 정확한 모델링 기법을 개발하였다. 또한, 실험 데이터와 시뮬레이션 결과 간 오차를 최소화하기 위해 보정기법을 적용하여 모델의 신뢰성을 확보하였다.

한편, SiP 기술은 이종 반도체 칩을 단일 모듈 내에 집적할 수 있는 효과적인 방법을 제공하지만, 고주파 환경에서 신호 무결성 및 시스템 성능을 확보하기 위해서는 패키지 형태의 선택 또한 매우 중요하다. 다

양한 패키징 방식 중, Land-Grid-Array (LGA) 패키지는 낮은 기생 인덕턴스, 짧은 접속 거리, 고밀도 I/O 구조를 통해 RF 회로에 적합한 솔루션으로 주목받고 있다. 특히, LGA 패키지는 채널 간 경로 대칭성 확보와 지연 시간 정합이 용이하여, 다채널 송수신 시스템에서 위상 및 감쇠 정합을 유지하는 데 매우 유리하다. 본 연구에서는 TSMC 65nm CMOS 공정으로 제작된 4채널 MFC를 내장한 고집적 LGA 패키지 구조를 설계하였으며, X-대역 RF 성능 향상을 목표로 배선 길이와 층간 구성을 최적화하였다. 이를 통해 삽입 손실, 인덕턴스, 그룹 딜레이의 채널 간 편차를 최소화하여, 고주파 시스템에서 필요한 위상 및 감쇠 정합을 가능하게 하였다.

패키지 수준에서의 신호 무결성 확보를 위해 3D EM 시뮬레이션을 수행하였고, 시뮬레이션 결과와 측정 데이터를 비교하여 정밀 모델링 기법을 확립하였다. 또한, 시뮬레이션과 실측 간의 오차를 줄이기 위한 보정 기법을 적용하여 모델의 신뢰성을 향상시켰다. 본 논문에서 제시한 모델링 및 최적화 기법은 X-대역에 국한되지 않고 다양한 고주파 대역 RF 패키지 설계에 적용 가능하며, 이는 차세대 고주파 반도체 패키징 기술의 성능 향상 및 상용화에 기여할 수 있을 것으로 기대된다.