Master's Thesis

Study of High-Efficiency Transformer-Based CMOS Power Amplifiers for X-Band and D-Band Applications

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ABSTRACT

In power amplifier (PA) design, it is crucial not only to ensure sufficient output power but also to simultaneously meet various requirements such as miniaturization, low power consumption, and low cost. In particular, when designing PAs with CMOS processes, limitations in output power and challenges in impedance matching caused by low impedance are considered major design hurdles. To address these issues, the stacked power amplifier architecture has gained attention as an effective alternative, enabling higher output power and power-added efficiency (PAE) compared to conventional single-transistor-based PAs.

In this study, we propose various PA designs incorporating different techniques in 65nm and 40nm CMOS technologies. For the 40nm CMOS process, a dual-peaking Gmax technique based on a feedback structure was applied to maximize the PA's gain. This approach secures wide bandwidth and high gain performance at higher frequency ranges. Meanwhile, in the 65nm CMOS process, a stacked PA configuration using three serially connected MOSFETs is adopted to enhance output power and maximize PAE. By distributing the voltage across the transistors, this design enables high-voltage

operation and achieves superior performance compared to conventional CMOS PAs.

The X-band PA achieves a power gain of 23.2 dB, a 3-dB bandwidth of 1 GHz, a peak power-added efficiency (PAE) of 24%, and a saturated output power (Psat) of 20.9 dBm at 9.5GHz. Reliability tests confirm that the proposed architecture successfully meets JEDEC standards in both HTOL and HAST, thereby demonstrating stable and reliable performance.

The D-band PA achieves a power gain of 27 dB with a 3dB bandwidth of 35.4 GHz centered at 140 GHz, a peak Power-Added Efficiency (PAE) of 4.74%, and a saturated output power of 14.6 dBm at 128GHz.

The proposed PA design methods are expected to provide an effective solution for achieving both high output power and high efficiency in high-frequency bands. Moreover, they will contribute to increasing the practical applicability of CMOS-based wireless communication systems.

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Chapter 1. Introduction

1.1 Research Background

As a communication system has developed, a high-efficiency and high-gain, high power transmitter is essential for future 6G communication. The sub-THz and mid-upper band are the attractive candidate for 6G communication [1][2]. At sub-THz, power amplifier has suffered from low gain due to low-performance at high frequency of active device. The X-band power amplifier has suffered from low power and low efficiency than III-V semiconductor technologies like GaN, GaAs. Despite of this disadvantage, CMOS has advantage because of its high-integrity due to BEOL characteristic and low-cost.

In this thesis, Dual-peaking G-max technology at D-band power amplifier and three-stacked power in X-band are investigated. Dual-peaking G-max technology is applied to boost gain and to get wide bandwidth in D-band while three-stacked power amplifier is designed for high output power and high power added efficiency in X-band. The implemented D-band PA achieves the highest FOM among bulk CMOS, and X-band three-stacked power amplifier

successfully achieves 256-QAM modulation test with high reliability. Reliability tests have been performed to confirm the robustness of the proposed architecture, showing negligible degradation in Psat and I_{DD} over 100 hours of continuous operation under high-voltage conditions, thereby demonstrating stable and reliable performance.

1.2 Thesis Organization

In Chapter 2, transformer-based power amplifiers are discussed; this chapter covers the fundamentals of RF transformer modeling and introduces the basic concepts of gain-boosting and power-combining techniques. Chapter 3 describes the design procedure for an X-band three-stack power amplifier, whereas Chapter 4 presents a dual-peaking G_{max} core that employs a neutralization capacitor as a gain-boosting technique for D-band operation. Finally, Chapter 5 concludes the thesis.

Chapter 2. Transformer-Based Power Amplifiers

2.1 Fundamentals of Transformer Design in RF

Transformers play a vital role in radio frequency (RF) integrated circuit (IC) design, especially in power amplifier (PA) implementations, where they are used for impedance transformation, single-to-differential conversion, compact layout, and DC isolation.

RF transformers can be modeled as shown in Fig. 2.1-1 with key parameters, including inductance(L), coupling coefficient (k), quality factor (Q), and winding resistance (R), which can be calculated using equations from (2.1.1) to (2.1.4). A high coupling coefficient ensures efficient energy transfer between the primary and secondary coils, while a high Q minimizes loss. However, due to metal thickness constraints and substrate losses inherent to CMOS technology, it is challenging to achieve high k and Q values in on-chip transformers. Therefore, transformer design requires optimization through electromagnetic (EM) simulation and a careful layout to mitigate parasitic effects and ultimately achieve high k and Q for improved efficiency.

$$R_i = \mathrm{Re}\{Z_{ii}\} \tag{2.1.1}$$

$$L_i = \frac{\mathrm{Im}\{Z_{ii}\}}{\omega} \tag{2.1.2}$$

$$k = \frac{\sqrt{\mathrm{Im}\{Z_{12}\}\,\mathrm{Im}\{Z_{21}\}}}{\sqrt{\mathrm{Im}\{Z_{11}\}\,\mathrm{Im}\{Z_{22}\}}} \tag{2.1.3}$$

$$Q_i = \frac{\omega L_i}{R_i} \tag{2.1.4}$$

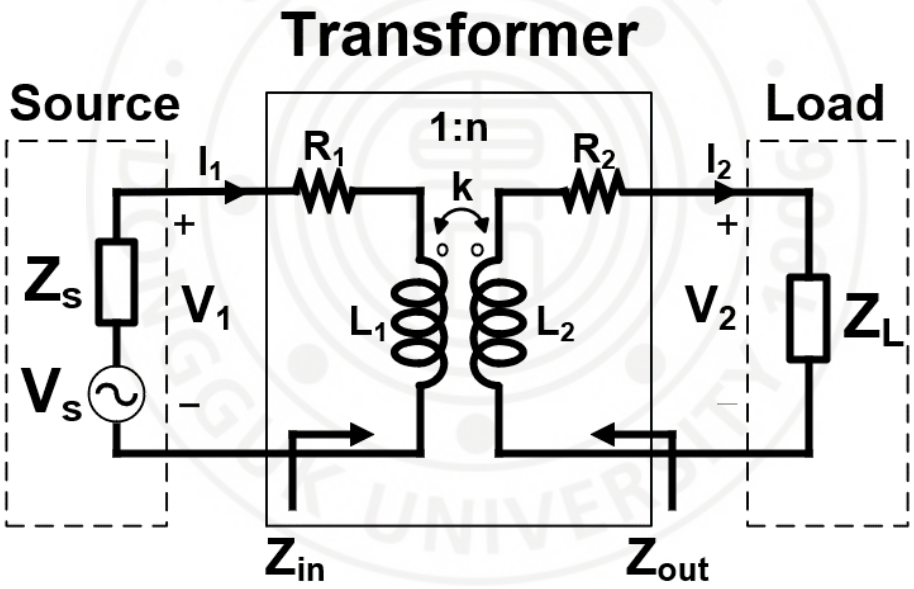


Figure 2.1-1 Transformer Model with circuit parameters

2.2 Transformer Modeling and Simulation

Transformer can be modeled using T-equivalent circuits that include mutual inductance(M), as shown in Fig. 2.2-1. These models are essential for circuit-level simulations, as they help verify design feasibility and simplify hand analysis of transformer behavior. However, at high frequencies, lumped models often lack accuracy due to the presence of distributed effects and layout dependent parasitics.

To improve modeling accuracy, full-wave EM simulators such as Ansys HFSS or Cadence EMX are used to extract the S-parameters of the transformer structure, as shown in Fig. 2.2-2. These EM simulators account for layout-related parasitics and material parameters such as metal thickness and the permittivity of the dielectric layer. Therefore, BEOL layers and the substrate must be accurately modeled using the foundry-provided PDK. The extracted SNP files from HFSS can then be imported into Cadence for co-simulation with active circuit components, enabling more reliable system-level verification.

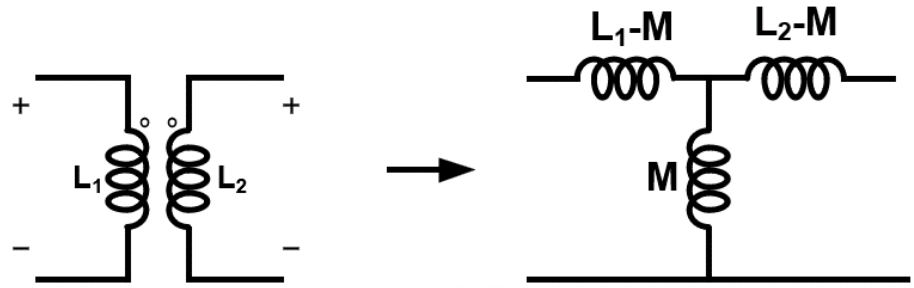


Figure 2.2-1 T-equivalent circuit with mutual inductance

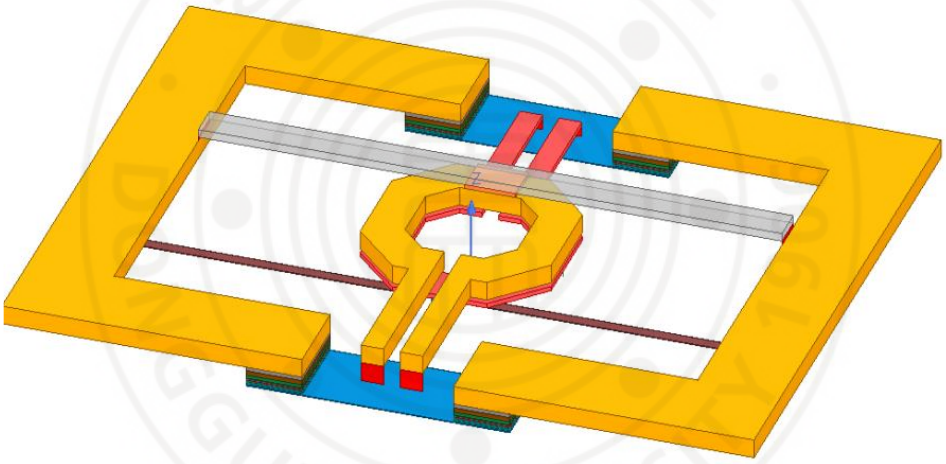


Figure 2.2-2 Transformer modeling in HFSS setup

2.3 Impedance matching utilizing transformer

In RF design, impedance matching is one of the most critical considerations. To transfer the maximum power from the source to the network and to the load, it is necessary to use conjugate matching[ref]. The source reflection coefficient can be described as equation 2.3.1.

$$\Gamma_s = \frac{Z_{in} - Z_s^*}{Z_{in} + Z_s}, \Gamma_L = \frac{Z_L - Z_{out}^*}{Z_L + Z_{out}} \quad \textbf{(2.3.1)}$$

Where Z_s, Z_{in}, Z_L, Z_{out} are impedances from Fig.2.1-1. The source and load impedances can be expressed in complex form as follows:

$$Z_s = R_s + jX_s \quad \textbf{(2.3.2)}$$

$$Z_L = R_L + jX_L \quad \textbf{(2.3.3)}$$

To make reflection coefficient to be zero, it is essential to ensure conjugate matching between Z_{in} and Z_s, as well as between Z_L and Z_{out}. In order to meet this requirement, Z_L and Z_s must satisfy the relationship derived in [3], shown in equations 2.3.4 and 2.3.5.

$$X_s = -\omega L_1, X_L = -\omega L_2 \quad \textbf{(2.3.4)}$$

$$R_s = R_1\sqrt{1+k^2Q_1Q_2}, R_L = R_2\sqrt{1+k^2Q_1Q_2} \quad \textbf{(2.3.5)}$$

Under these simultaneous conjugate matching conditions, the maximum available gain (Gmax) of the transformer can be expressed as equation 2.3.6, as discussed in [3].

$$G_{\max} = 1 - 2\frac{\sqrt{k^2 Q_1 Q_2 + 1} - 1}{k^2 Q_1 Q_2} \qquad \textbf{(2.3.6)}$$

Chapter 3. Enhancement Methods for CMOS PAs

Building upon the transformer principles established in Chapter 2, this chapter introduces enhancement methods that leverage transformer structures to overcome the limitations of CMOS power amplifiers. In particular, it presents techniques aimed at maximizing two key performance metrics in PA design—gain and output power—through transformer-based power combining and gain boosting approaches.

3.1 TF-Based Power Combining Techniques

In CMOS power amplifier (PA) design, transformer-based power combining techniques are widely employed to overcome the limited output power capability of individual amplifier cells due to low device breakdown voltages. By combining multiple PA cells, these techniques enable watt-level output while distributing the voltage and current stress across devices.

There are two principal transformer-based power combining architectures: voltage-mode combining and current-mode combining. The following sections compare these approaches and justify the selection of current-mode combining in this work.

3.1.1 TF-Based Voltage Power Combining

In the voltage combining approach, the secondary windings of the transformer are connected in series, allowing the individual voltage outputs from multiple power amplifier channels to be summed directly. This method inherently supports the realization of a high output voltage and can simplify the impedance matching process. As illustrated in Fig. 3.1-1, the optimum device resistance is given by

$$R_{optMOS} = \frac{R_L}{2mn^2} \quad \textbf{(3.1.1)}$$

where m is the number PA unit and n is the transformer turn ratio. This indicates that voltage mode power combining lets a larger output device keep good power matching to the load.

However, when combining a large number of channels, voltage combiner has disadvantage. When the number of channels is increased, the PA suffers from parasitics which can degrade the reliability of PA is in the presence of process and temperature variations [4].

Fig. 3.1-2 shows the layout implementation of voltage mode power combining for the two differential PA units.

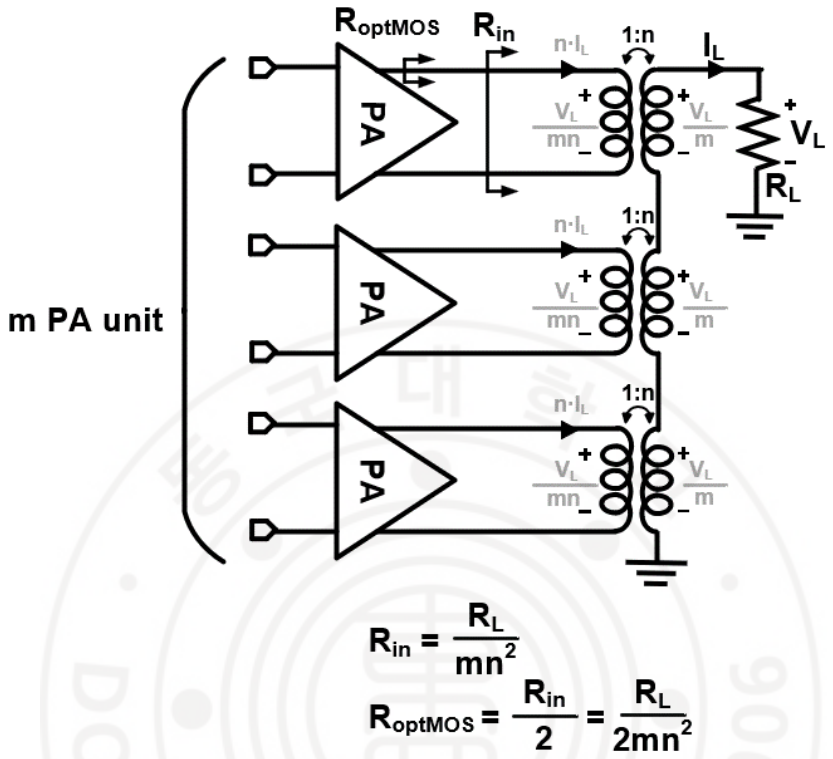


Figure 3.1-1 Impedance transformation of voltage mode power combining

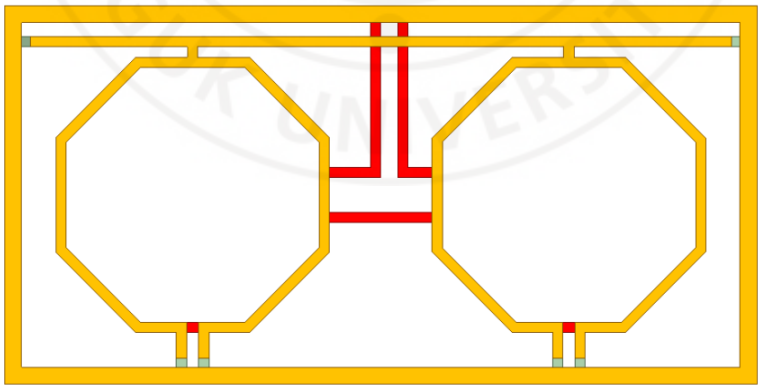


Figure 3.1-2 Layout implementation of voltage mode power combining

3.1.2 TF-Based Current Power Combining

There are two different ways for current power combining scheme: using multi secondary coil and using single secondary coil based on magnetic coupling.

3.1.2.1 Multi secondary coil

The current power combining scheme leverages a parallel summation of the currents from each power amplifier channel via a common secondary winding.

As illustrated in Fig. 3.1-3, for an arrangement of m PA units using a transformer with turn ratio n, the optimum load resistance per device is given by:

$$R_{optMOS} = \frac{mR_L}{2n^2} \quad \textbf{(3.1.2)}$$

This value is higher than that of voltage-mode combining, which can pose challenges for efficient power matching in large-size transistors that inherently favor lower load impedances due to their low output resistance.

Despite this limitation, current-mode combining is generally more favorable in practical high-frequency implementations. Its superior channel symmetry reduces the impact of layout-induced mismatches, which become increasingly critical at millimeter-wave

frequencies[4]. Furthermore, the current-mode architecture facilitates symmetric routing and transformer layout, minimizing parasitic imbalance and enabling more stable performance across varying operating conditions.

Fig. 3.1-4 shows the layout implementation of current-mode power combining using multiple secondary coils for two differential PA units.

3.1.2.2 Single secondary coil

Another current-mode combining method uses a single shared secondary coil, where each PA channel drives its own primary winding on a common transformer core, as illustrated in Fig. 3.1-5.

This architecture enables a compact layout but is more sensitive to layout-dependent parasitics such as interwinding coupling and phase mismatch.

Compared to the multi-secondary approach, the single-secondary combining offers higher integration, but requires more careful layout optimization to ensure consistent combining efficiency.

Fig. 3.1-6 shows the layout implementation of current-mode power combining using single secondary coil for two differential PA units.

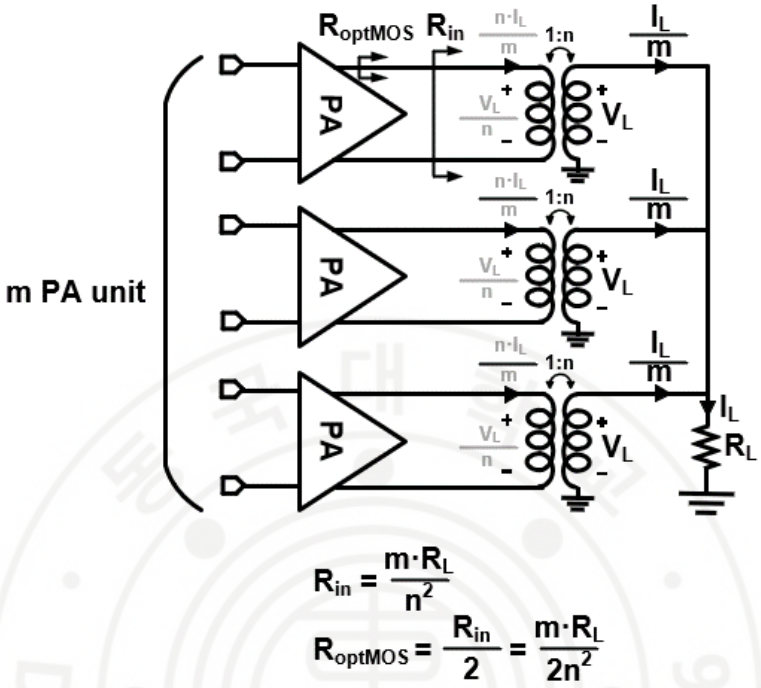


Figure 3.1-3 Impedance transformation of current mode power combining: Multi secondary coil

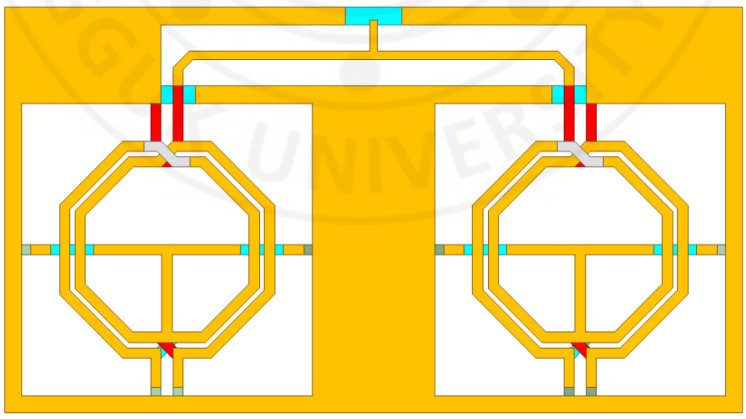


Figure 3.1-4 Layout implementation of current mode power combining: Multi secondary coil

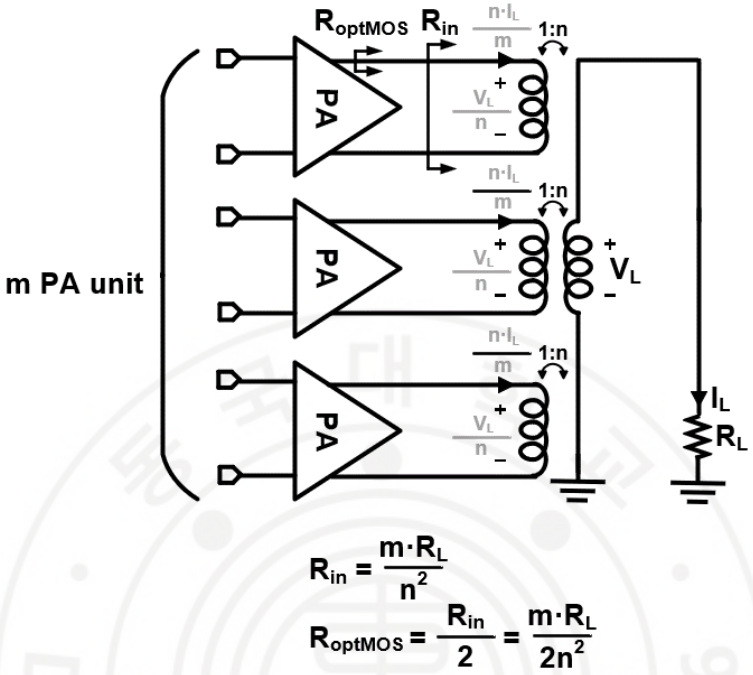


Figure 3.1-5 Impedance transformation of current mode power combining: Single secondary coil

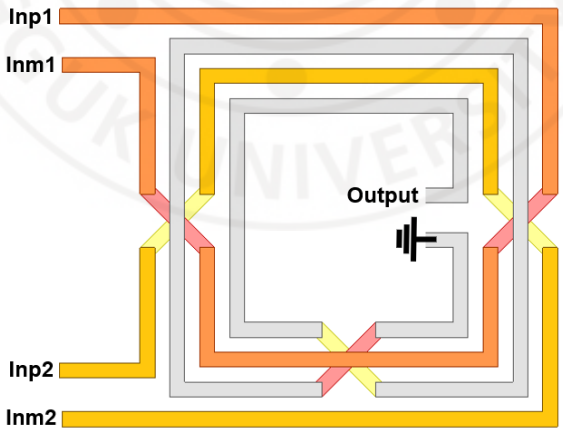


Figure 3.1-6 Layout implementation of current mode power combining: Single secondary coil

3.1.3 Comparison between two combining techniques

In transformer-based power combining networks, transformer efficiency(η) is a key performance, defined as the ratio of total output power(P2) to the total input power from m unit PA (MP1) as equation 3.1.3.

$$\eta = \frac{P_2}{mP_1} \tag{3.1.3}$$

Based on prior analytical studies [5], it has been observed that current-mode combining generally achieves higher transformer efficiency than voltage-mode combining, particularly in lossy CMOS processes. This is mainly due to the lower impact of parasitic resistance in the current-mode combining structure. In contrast, in voltage-mode combining, the parasitic resistance in the primary windings become dominant compared to the transformed load impedance, resulting in significant power consumes input power at the primary windings. Table 3.1-1 compares the key characteristics of these two combining schemes.

Table 3.1-1 Comparison of Transformer-Based Power Combining Techniques

Feature	Voltage Combining	Current Combining
Combining	Series	Parallel
Type	Voltage summation	Current summation
R_{optMOS}	$R_{optMOS} = \frac{R_L}{2mn^2}$	$R_{optMOS} = \frac{mR_L}{2n^2}$
Output current handling	High	Low
Sensitivity to parasitics	High	Low
Amplitude/Phase error	high	low
Output power Capability	High	Lower than voltage mode

3.1.4 Structure and Efficiency Considerations in This Work

In this work, current-mode transformer-based power combining was employed in both X-band and D-band CMOS power amplifiers. This architectural choice was motivated by the need for high channel symmetry, robustness against mismatch, and compatibility with reconfigurable or discretely controlled power structures.

For the X-band and D-band implementations, current-mode transformer-based combining was used to efficiently aggregate multiple PA outputs while minimizing amplitude and phase mismatches. In the X-band design, a three-stacked, four-way PA achieved high output power and efficiency under a 3.3 V supply. At D-band, where parasitic effects and layout asymmetry are more critical, a five-stage, eight-way PA was implemented using the current-mode scheme to enable stable multi-channel operation.

Overall, the current-mode transformer-based combining scheme adopted in this work enables robust, scalable, and efficient CMOS PA implementations at both microwave and millimeter-wave frequencies. The selected architecture balances practical layout constraints with performance needs, supporting the goals of power density, linearity, and reconfigurability in modern RF systems.

3.2 Gain Boosting Techniques in CMOS PAs

In sub-THz CMOS power amplifiers, the inherently low gain caused by device parasitics and the limited intrinsic performance of transistors necessitates the use of gain boosting techniques. Among various approaches, two prominent methods are Linear, Lossless, Reciprocal (LLR) embedding[6][7] and lossy capacitive over-neutralization[8].

LLR embedding maintains Mason's unilateral gain (U), which is defined in equation 3.2.1, while increasing the maximum available power gain (G_{ma}) up to 4U at the edge of stability. In contrast, lossy over-neutralization increases U itself, enabling G_{ma} to exceed the lossless limit even near the maximum oscillation frequency (fmax).

These two methods address the low-gain challenge through different mechanisms and present distinct trade-offs in terms of stability, implementation complexity, and achievable performance.

$$U = \frac{\left|y_{21} - y_{12}\right|^2}{4(\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12})\,\mathrm{Re}(y_{21}))} \qquad \textbf{(3.2.1)}$$

3.2.1 LLR embedding

The maximum available gain (G_{ma}) of a two-port network can be expressed in terms of the unilateral gain (U) and the gain ratio (A), as shown in the following equation:

$$\frac{G_{ma}}{U} = \left| \frac{A - G_{ma}}{A - 1} \right|^2 \qquad \textbf{(3.2.2)}$$

Here, U is the unilateral power gain, and A is defined as Y_{21}/Y_{12} or equivalently Z_{21}/Z_{12}. The maximum available gain G_{ma} can be controlled by adjusting both A and U. However, in LLR embedding as illustrated in Fig. 3.2-1, U is held constant while A is selectively varied, enabling G_{ma} to be boosted up to 4U under the edge-of-stability condition [9].

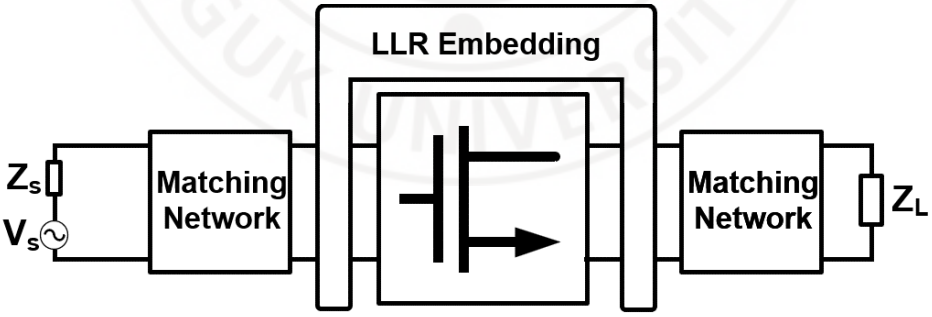


Figure 3.2-1 LLR embedding that increases G_{ma} to G_{max}

3.2.2 Lossy capacitive over-neutralization

As mentioned in 3.2.1 unilateral power gain(U) remains unchanged when using the LLR embedding structure. However, by employing a resistor in series with the conventional neutralization capacitor as illustrated in Fig. 3.2-2, U can be increased, as the added resistor effectively cancels a portion of the transistor's intrinsic gate resistance. This compensation increases the real part of the y-parameters, allowing $Re(y_{12})$ to shift from a negative to a positive value. As a result, the unilateral gain U increases, as described in Equation 3.2.1.

Using this technique, it was reported that a 190GHz amplifier was implemented in 28nm bulk CMOS technology, achieving 14.3dB of gain with 1.5dBm of PSAT and 2.6% of maximum PAE [8].

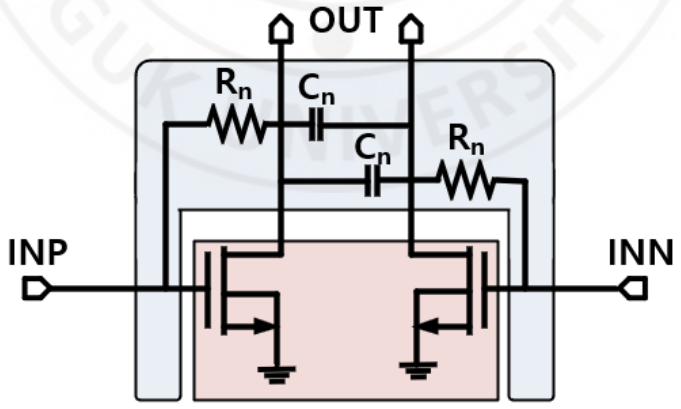


Figure 3.2-2 Lossy capacitive over-neutralization structure

3.2.3 Structure Implementation in this work

In this work, a dual-peaking G_{max} boosting technique [10] based on LLR embedding is applied. Due to the inherently low gain resulting from device parasitics and the limited intrinsic performance of transistors, gain enhancement techniques are essential in sub-THz CMOS PAs. By employing this dual-peaking G_{max} boosting technique, both high gain and wide bandwidth can be simultaneously achieved. Unlike the approach in [10], which utilizes a long transmission line in the feedback path, this work adopts an over-neutralized capacitor to achieve compact implementation. The detailed design of the proposed dual-peaking G_{max} boosting technique will be presented in Chapter 5.

Chapter 4. X-band Power Amplifier Design

4.1 Concept of stacked structure

The stacked power amplifier design involves literally stacking multiple MOSFETs in series to accommodate higher voltage swings. Since Bulk CMOS cannot inherently sustain large voltage swings, it typically delivers lower output power compared with III-V semiconductor technologies such as GaN, GaAs, and InP.

However, Bulk CMOS remains widely adopted due to its low cost and high integration density. In particular, its back-end-of-line (BEOL) process offers multiple metal layers that facilitate routing and enable on-chip integration without requiring external packaging.

To overcome Bulk CMOS's limitations in handling large voltage swings, the stacked structure has emerged as a compelling solution [11][12]. Unlike a common-source (CS) amplifier, stacking MOSFETs in series distributes voltage across each device, enabling higher voltage handling. This approach allows a bulk CMOS technology to achieve higher output power and improved power-added efficiency despite its inherent performance gaps relative to III-V technologies.

Stacked power amplifier (PA) configurations, such as 2−stack, 3−stack, or n−stack, are widely used to boost the output power by increasing the voltage swing. However, stacking excessive devices leads to significant losses, primarily due to parasitic capacitance. As illustrated in Fig. 4.1−1, we adopt a three−stack topology that achieves roughly 90 % stacking efficiency, offering an optimal balance between output power and efficiency [11].

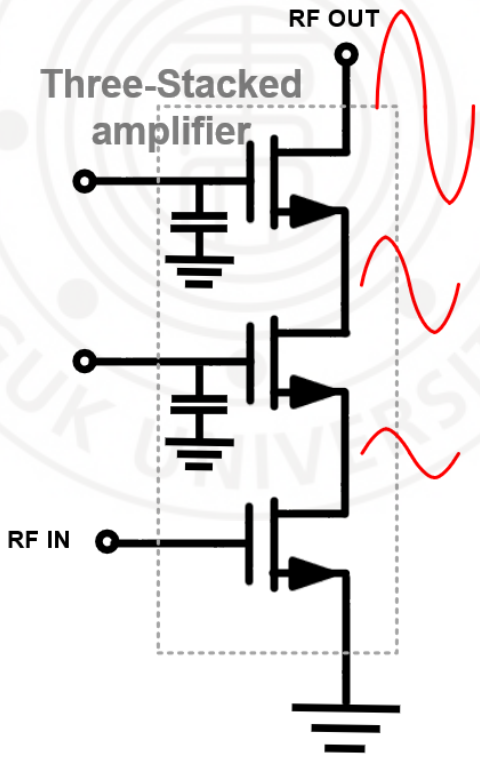


Figure 4.1-1 Schematic of three-stacked power amplifier

4.1.1 Hybrid stacked structure

Stacked amplifier has advantage of high voltage handling capacity but it can induce reliability issue due to the top device has to endure large voltage swing. As a result, this design introduces significant challenges associated with large voltage swings, including reliability concerns such as time dependent dielectric breakdown (TDDB), hot-carrier injection (HCI) which can cause impedance mismatch and output power degradation. To mitigate these issues, thick-oxide transistors which is commonly used as I/O devices can be applied at the top stack to endure high voltage swing. To evaluate the reliability of the device, Time-to-Failure (TTF) based on TDDB and accelerated-lifetime model based on HCI are widely used [13], which can be simplified as:

$$TTF_{TDDB} \propto \exp(1/E_{ox}) \quad \textbf{(4.1.1)}$$

$$Lifetime_{HCI} \propto W / I_{gate} \quad \textbf{(4.1.2)}$$

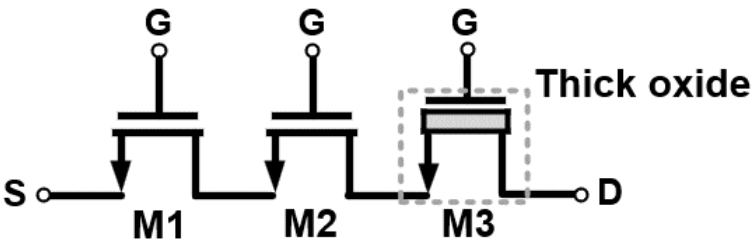
where E_{ox} is the applied electric field across the dielectric and W is the device gate width. Owing to their thicker dielectric layers and larger device size, thick-oxide devices experience lower electric fields under the same voltage, significantly reducing TDDB degradation rates and improving overall reliability. Additionally, it is

demonstrated that thick-oxide devices offer superior reliability, including higher breakdown voltage and longer mean time to failure under the same voltage conditions compared to their thin-oxide counterparts [14].

Fig. 4.1-2 shows the proposed hybrid structure and the performance comparison table is explained. The thick-oxide device has twice size of oxide thickness than thin-oxide device but has inferior performance. This issue will be discussed in chapter 4.1.2.

As illustrated in Fig. 4.1-3, drain-source voltage of top device reaches 3V, while the standard supply voltage of normal RF NMOS is only up to 1.2V. Considering AC/DC ratio as 2, the standard voltage swing would be 2xVDD, up to 2.4V. However, 3 V exceeds this value, potentially triggering reliability concerns and raising doubts about robust operation.

On the other hand, thick-oxide devices, rated for nominal voltages of 2.5 V, can handle voltages exceeding 5 V [14]. Thus, M3 as a thick-oxide FET effectively addresses the stress issue, enabling robust operation under higher voltage swing.



Device parameters

	Oxide Thickness	VDD	Channel length	g_m	Fmax (GHz)	Ft (GHz)
Thin oxide	<30Å	1.2V	60nm	0.34	203	188
Thick oxide	<60Å	2.5V	280nm	0.21	104	41

Figure 4.1-2 Proposed hybrid three-stack FETs configuration with device parameters between thick and thin oxide device

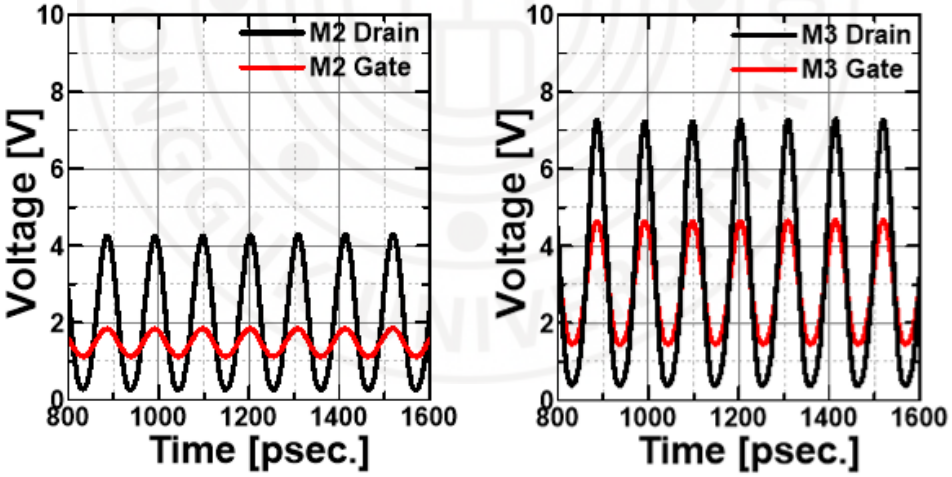


Figure 4.1-3 Simulated voltage swing of drain node and gate node of M2 and M3

4.1.2 Design approach of Hybrid stacked structure

The thick-oxide MOSFET offers reliability advantage but suffers from inferior performance due to its low F_{max} and F_t compared to a thin-oxide device. Moreover, it requires higher supply voltage and gate voltage to operate in saturation, which can disrupt uniform voltage distribution, and it draws more current. By placing this thick-oxide device only at the top, these drawbacks can be mitigated. The current consumption is determined by the bottom device(M1) and uniform voltage distribution can be achieved with proper bias condition. Additionally, the voltage gain of the stacked amplifier is dominantly determined by M1. Fig. 4.1-4 shows the simplified equivalent circuit of three-stacked amplifier and the voltage gain can be expressed by equation as follows:

$$A_v = -\frac{g_{m1} \cdot R_L}{\left(1+sC_{gs1} \cdot R_g\right)\left(1+\frac{sC_{gs2}}{g_{m2}}\right)\left(1+\frac{sC_{gs3}}{g_{m3}}\right)} \qquad \textbf{(4.1.3)}$$

Since sC_{gs2}/g_{m2} and sC_{gs3}/g_{m3} is relatively small than unity, the A_v can be approximately a function of parameter of M1 and R_L. The maximum available gain and voltage gain of the stacked structure with the thin-oxide FETs and that with the thick-oxide FETs are

illustrated in Fig. 4.1-5. It shows that the hybrid three-stack with thick oxide at the top is expected to improve reliability with about 0.5 dB trade-off in Gmax.

Also, the gate capacitor value is crucial in stacked amplifier design. Unlike a cascode structure, which has AC ground on gate node, stacked amplifier has gate voltage swing to avoid the gate-drain oxide breakdown. Also, the gate capacitors are utilized to achieve node impedance matching. The value of gate capacitors is selected from well-known equation from [11]:

$$C_{gk} = \frac{\left(C_{gs} + C_{gd}(1 + g_m Z_{opt})\right)}{(k-1)g_m Z_{opt} - 1}, k = 2,3 \qquad \textbf{(4.1.4)}$$

Z_{opt} is expressed at Fig 4.1-4, Cgs and C_{gd} are device gate-source and gate-drain capacitors, respectively. Considering this equation, C_{g1} is selected as 800fF and C_{g2} is determined as 499fF in this design.

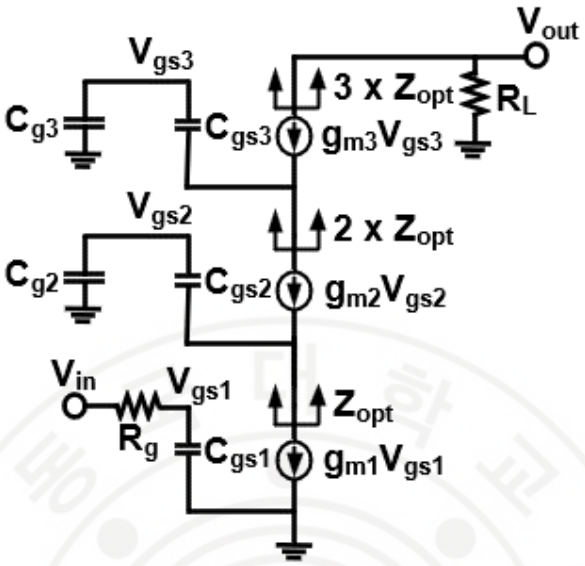


Figure 4.1-4 Simplified small signal equivalent circuit of three-stacked structure

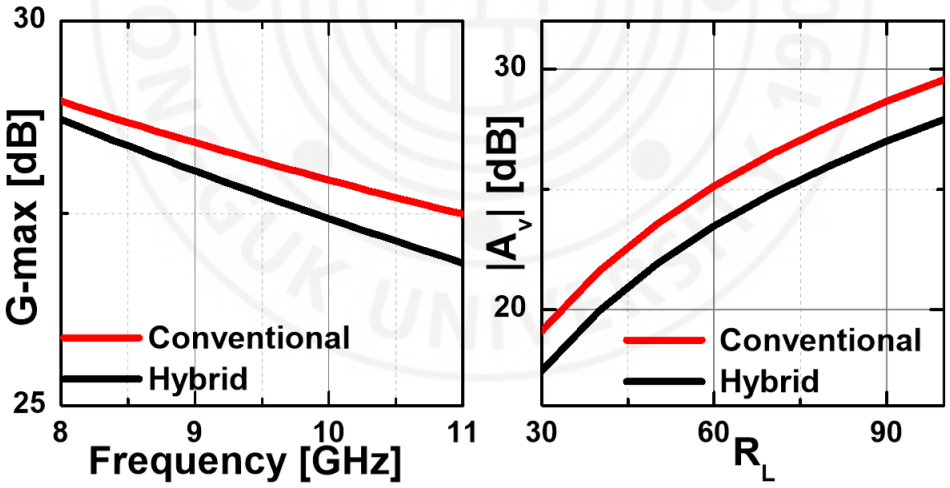


Figure 4.1-5 Simulation results of G-max and |Av| related to RL for the conventional and hybrid structure

4.2 Circuit Implementation in 65nm BULK CMOS

4.2.1 Device selection and layout

To implement a three-stacked structure in bulk CMOS, a deep n-well is used to isolate each device's bulk from the shared substrate, preventing junction breakdown and latch-up. This isolation also enables independent body biasing, reducing parasitic effects and enhancing reliability under high-voltage conditions. To achieve three-stacked structure in bulk CMOS technology, the deep n-well is applied in layout as illustrated in Fig. 4.2-1. In this design, we selected device widths of 192 μm for thin-oxide transistors and 756 μm for thick-oxide transistor. Each transistor's deep n-well is biased at V_{DD} to prevent junction breakdown which comes from p-n junction. Without this bias, the p-n junction could become forward bias, potentially leading to junction breakdown. Fig. 4.2-2 presents schematic of proposed three-stacked power amplifier with deep n-well and its layout implementation.

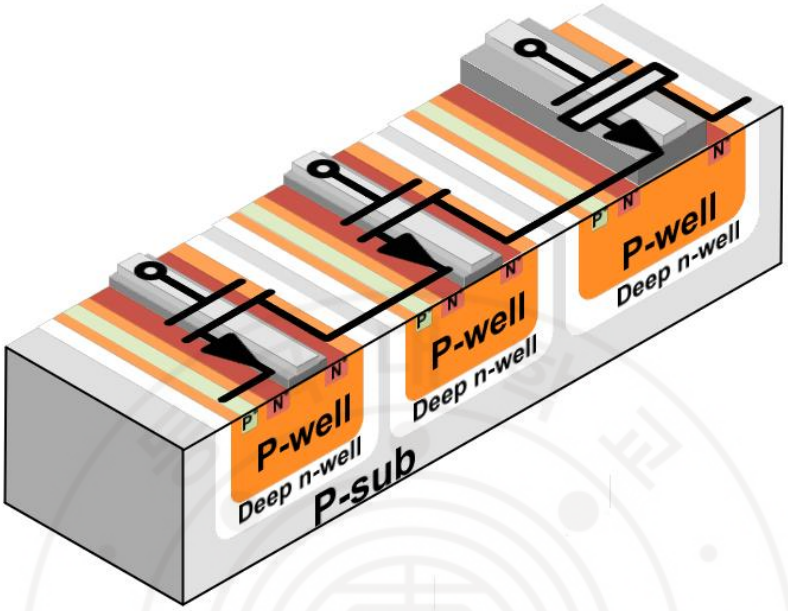


Figure 4.2-1 3D-model of hybrid stacked FETs.

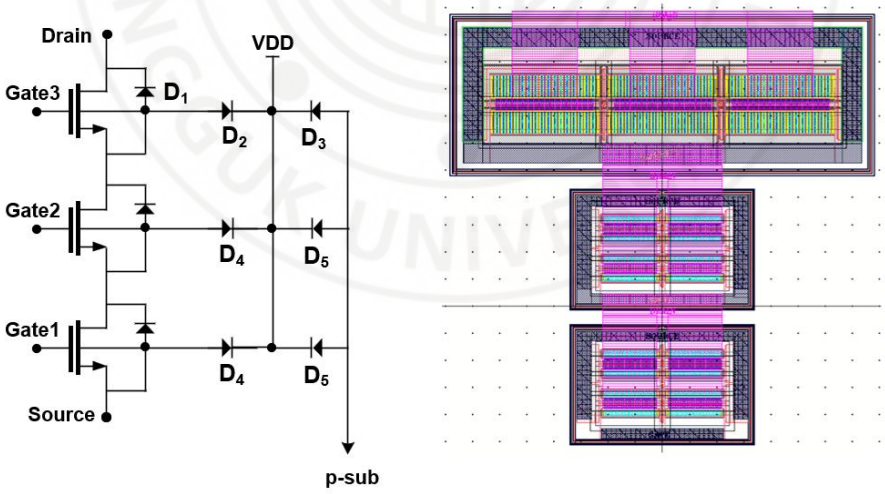


Figure 4.2-2 Schematic of proposed three-stacked power amplifier with deep n-well and its layout implementation

4.2.2 Over-neutralization capacitor

It is explained that hybrid structure has 0.5dB gain trade-off than conventional structure. To address the gain reduction caused by the thick-oxide device at the top stage, an over-neutralized cross-coupled capacitor is incorporated in M1. It should be noticed that utilizing a capacitor larger than C_{gd} can cause potential instability and output power degradation due to the undesirable positive feedback [15]. Fig. 4.2-3 shows the simulation results for the maximum available gain as a function of the neutralization capacitor C_n. In this work, an overcompensated cross-coupled capacitor with C_n =106fF is used to balance the gain reduction and instability issue.

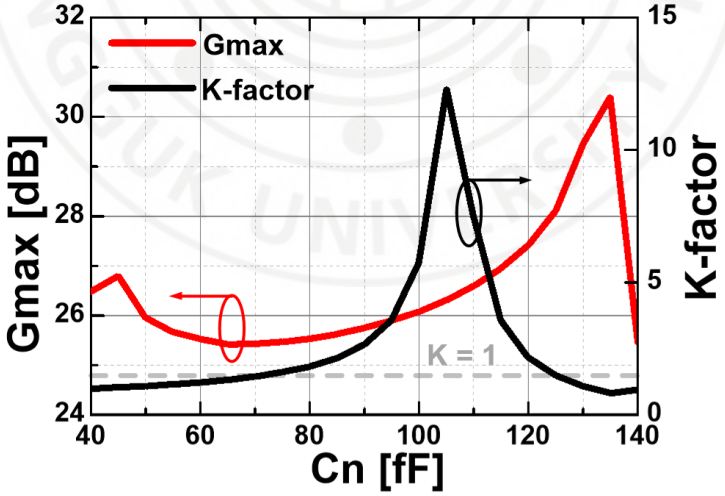


Figure 4.2-3 Simulation result of G-max and stability factor versus C_n.

4.2.3 Passive element design

4.2.3.1 TF-based balun design

Accurate modeling of parasitic in radio frequency range is important to get precise measurement result. For the accurate modeling, the parasitic of the active devices were extracted at the transistor level using the Calibre tool under a 50℃ operating condition, while the passive components, including transmission lines and transformers, were modeled through full-wave electromagnetic simulations using HFSS.

Using dielectric and metal information from foundry provided PDK, BEOL can be modeled accurately. Top metal is used for the primary side considering current flows in drain side and metal below top metal is utilized for the secondary side.

4.2.3.2 CPW transmission line power combining

To implement four-way power amplifier each differential PA is current-combined with CPW line. 100Ω CPW line is utilized to combine each differential PA whose output impedance is 100Ω, which results in 50Ω matching. Fig. 4.2-4 illustrates the layout of current mode power combining structure, the simulated insertion loss is presented in Fig. 4.2-5.

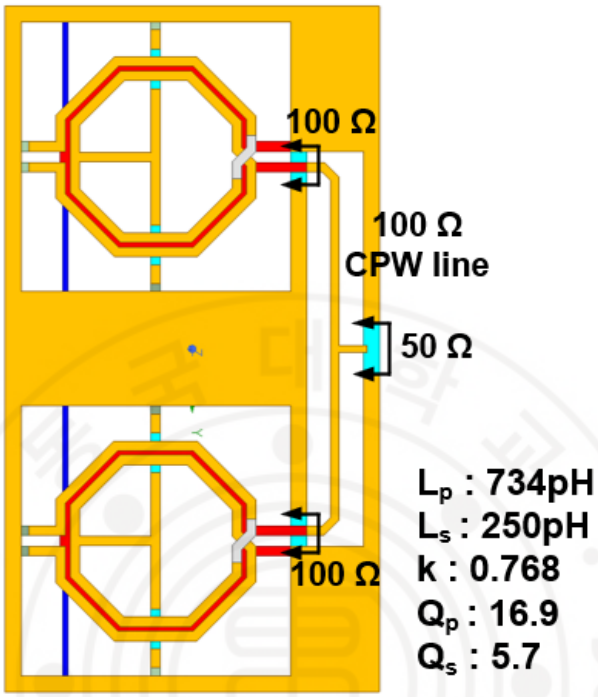


Figure 4.2-4 Layout of current mode power combining structure.

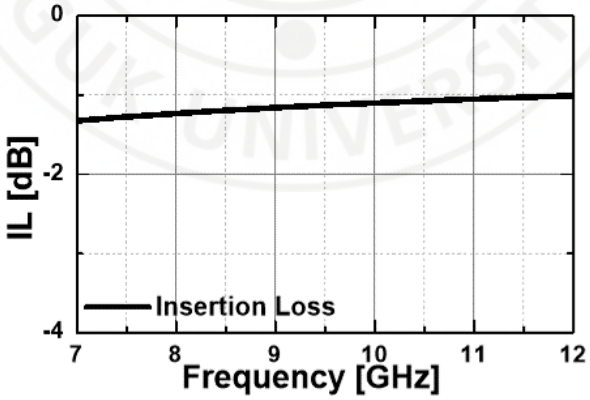
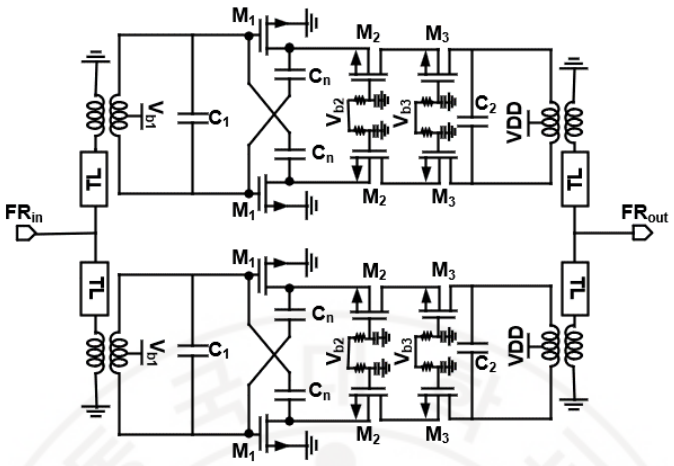


Figure 4.2-5 Simulated Insertion loss of transformer-based balun.

4.2.4 Schematic and chip photograph

The hybrid three-stacked, four-way X-band power amplifier is proposed and designed, as illustrated in Fig. 4.2-6. The amplifier's stability was also confirmed through the Mu and Mu_prime factors shown in Fig. 4.2-7, both exceeding unity across the operating band, indicating unconditional stability. The output power contour of the three-stacked structure, under the bias conditions illustrated in the schematic and with an input power of -5 dBm, is presented in Fig. 4.2-8. Fig. 4.2-9 shows the simulated impedance trajectory of the output matching network over the 8GHz to 12GHz frequency range. Fig. 4.2-10 presents the transient simulation results, demonstrating stable large-signal behavior. Fig. 4.2-11 the chip photo of the fabricated PA. The chip occupies a total area of 0.577 mm^2, with the core (excluding pads) measuring only 0.22 mm^2.



Device parameters

M_1, M_2	M_3	V_{b1}, V_{b2}, V_{b3}
256 μm(W) / 60 nm(L)	768 μm(W) / 280 nm(L)	0.45V/ 1.6V/ 3V

C_1	C2	C_n	VDD
150 fF	195 fF	106 fF	3.3 V

Figure 4.2-6 Schematic of the proposed hybrid 3-stack 4-way PA.

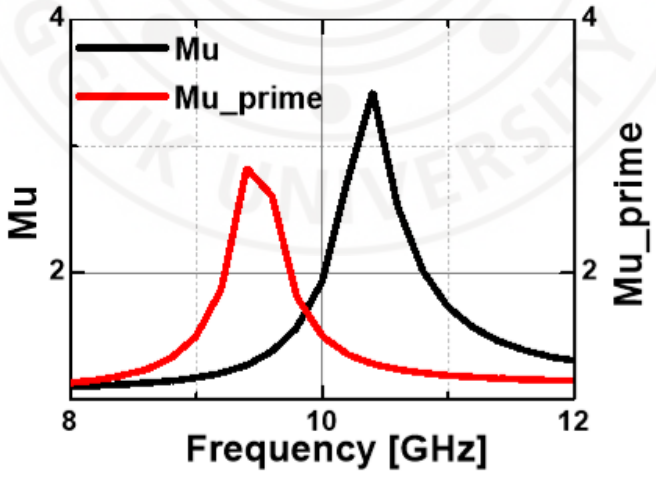


Figure 4.2-7 Simulated Mu and Mu_prime factor

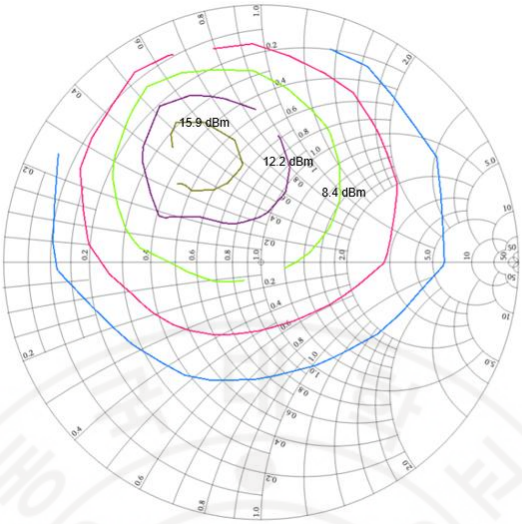


Figure 4.2-8 Power contour of three-stacked structure under the bias condition illustrated in Fig. 4.2-6, with the input power set to the 1-dB compression point.

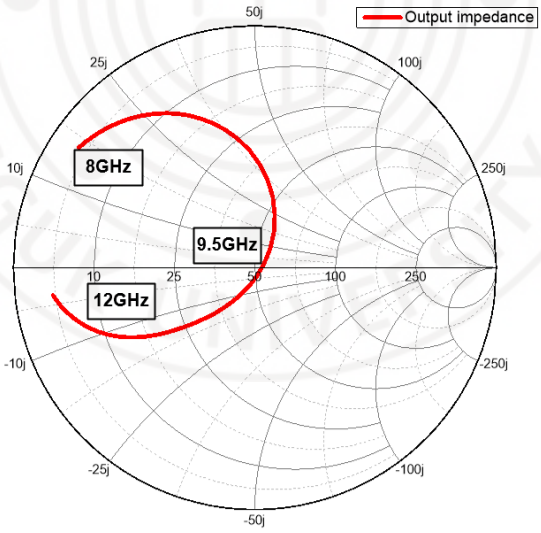


Figure 4.2-9 Simulated output network impedance versus frequency

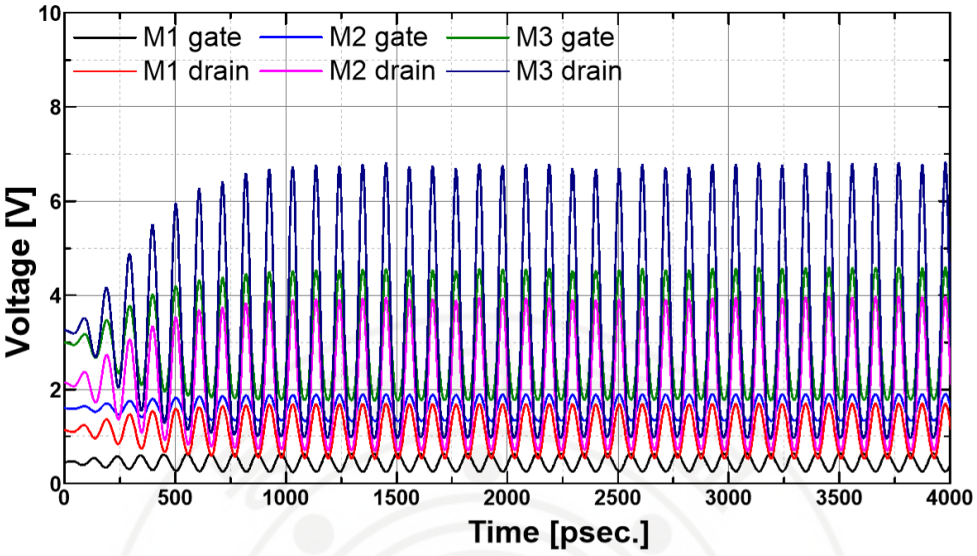


Figure 4.2-10 Simulated transient result of all gate and drain node with the input power set to the 1-dB compression point.

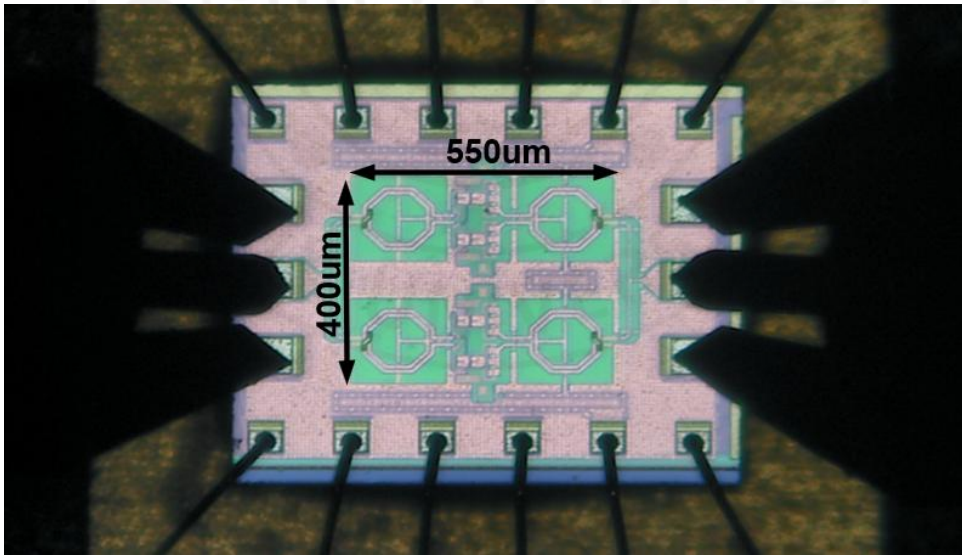


Figure 4.2-11 Die photo of the fabricated PA (core size: 0.22 mm²)

4.3 Measurement

4.3.1 small-signal

4.3.1.1 small-signal measurement setup

The proposed X-band PA was implemented in 65nm bulk CMOS technology. The implemented PA was evaluated through on-wafer probing of a chip-on-board (CoB) for DC biasing. S-parameter measurements were performed with Keysight N5224A network analyzer after on-wafer calibration using GGB CS-105 as illustrated in Fig. 4.3-1.

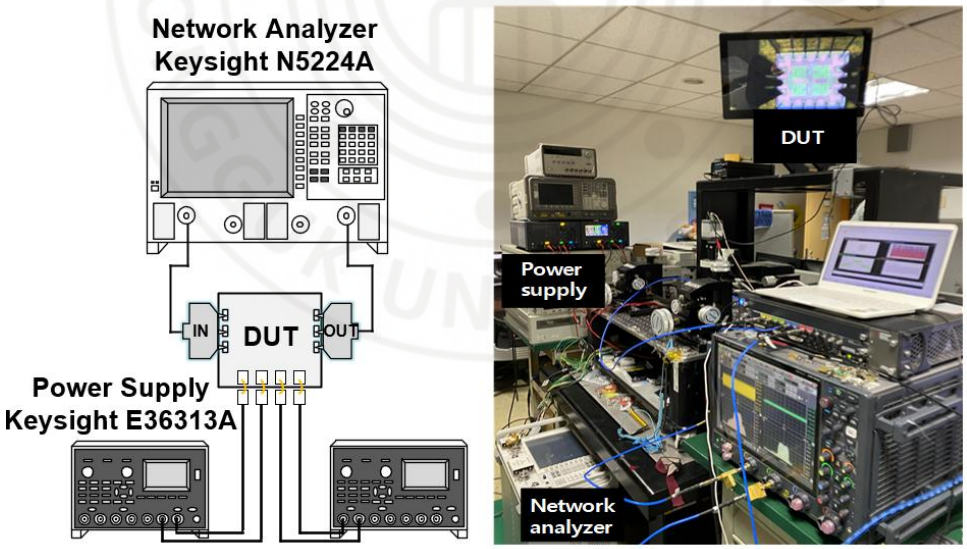


Figure 4.3-1 Small signal measurement setup

4.3.1.2 small-signal measurement result

The measured S-parameters are presented in Fig. 4.3-2. The implemented PA achieves an S21 of 23.2dB at 9.5GHz, an input and output return loss of better than 10dB, and a 3dB bandwidth of around 1GHz. S12 was less than -43dB at all frequency range. Unconditional stability was confirmed across the entire frequency band, as demonstrated by the K-Δ stability test in Fig. 4.3-3.

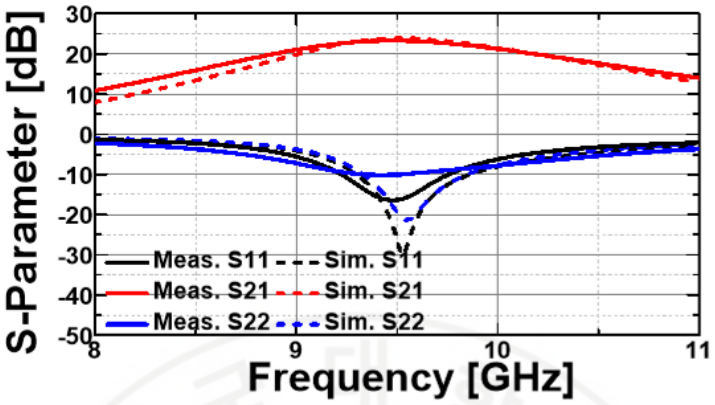


Figure 4.3-2 Simulated and Measured S-parameters

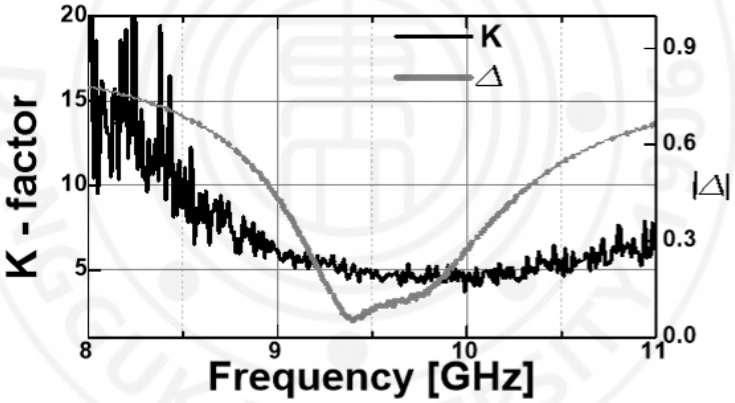


Figure 4.3-3 Measured Stability factor

4.3.2 Large-signal

4.3.2.1 Large-signal measurement setup

The large-signal measurements, Agilent 83623B signal generator and Agilent E4407B spectrum analyzer were used after meticulous compensation for cable and probe tip losses, as depicted in Fig. 4.3-4.

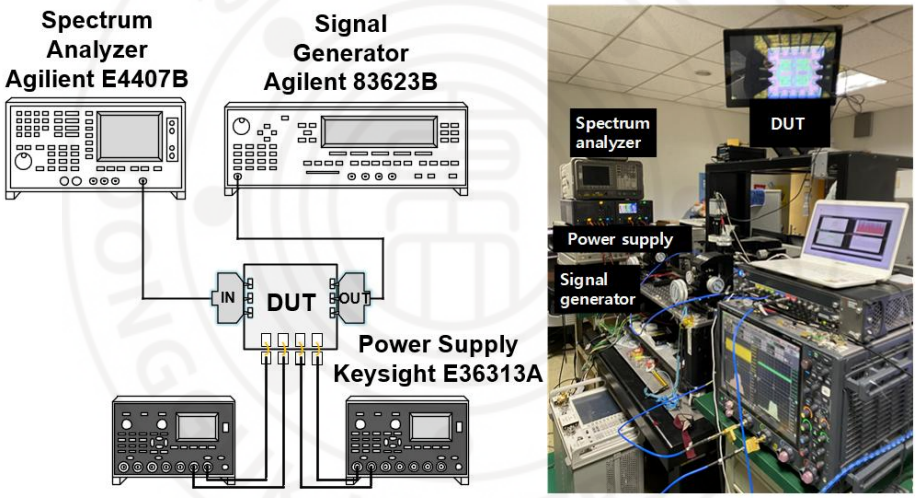


Figure 4.3-4 Large signal measurement setup

4.3.2.2 Large-signal measurement result

The measured saturated power (Psat) is 20.9dBm at 9.5GHz, output 1dB compression point (OP1dB) is 16.4dBm and peak PAE is 24% as shown in Fig. 4.3-5. Fig. 4.3-6 shows the Pout, OP1dB and PAE across the operating frequency range.

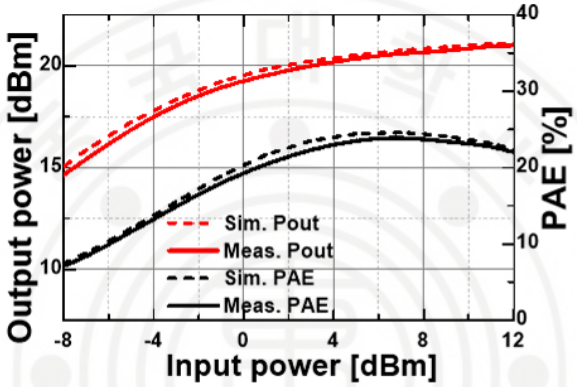


Figure 4.3-5 Simulated and Measured Pout and PAE versus Pin at 9.5GHz

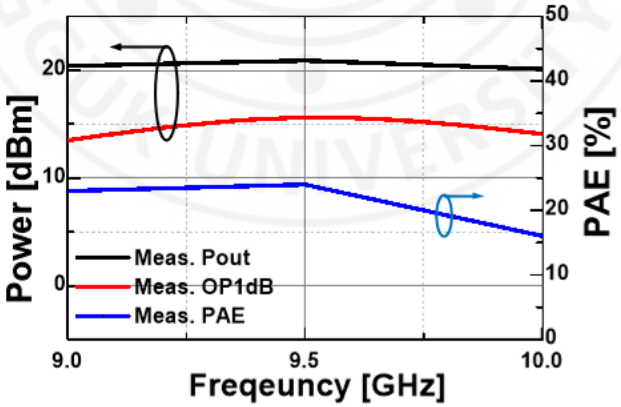


Figure 4.3-6 Pout, OP1dB and PAE across the operating frequency range

4.3.3 Modulation test

4.3.3.1 Modulation test setup

The modulation tests were conducted with Keysight M8195A arbitrary waveform generator to input a modulated signal and Keysight UXR0104A digital oscilloscope to characterize the output as shown in Fig. 4.3-7. Digital predistortion was applied to compensate for the PA's inherent nonlinearity, ensuring improved linearity and meeting stricter EVM/ACPR requirements during the modulation test.

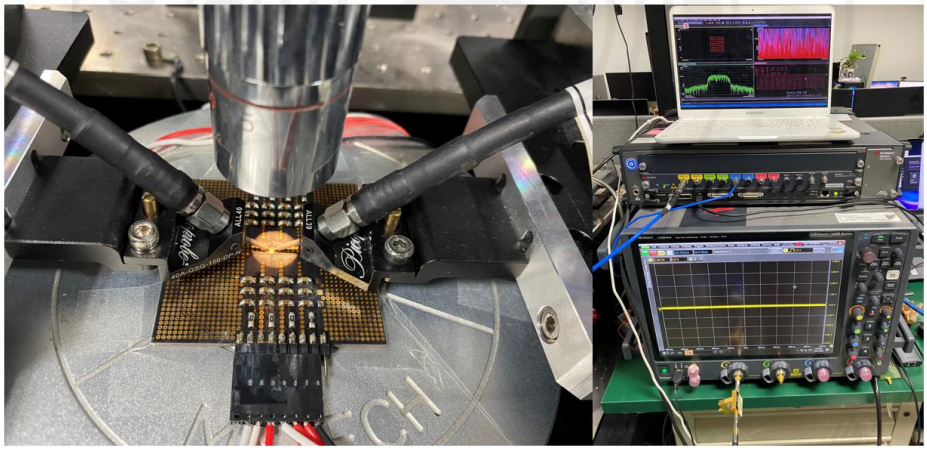


Figure 4.3-7 Modulation test setup

4.3.3.2 Modulation test result

The 500MHz Baud 64−QAM measurement achieved an EVM of −25 dB and ACPR below −34 dBc without digital predistortion (DPD) as shown in Fig. 4.3−8. When DPD is applied, the ACPR performance is further enhanced, as illustrated in Fig. 4.3−9. To investigate feasibility of higher−order modulation schemes such as 256−QAM, digital predistortion is applied during measurement. The measurement shows −35 dB of error vector magnitude (EVM) and −33.5dBc of the adjacent channel power ratio (ACPR) with 256−QAM, measured with a 600 MHz reference and adjacent channel bandwidth, as presented in Fig. 4.3−10. At 9.5GHz, the PA achieves a 4.8Gbps data rate with average power of 12.7dBm, average PAE of 4.58%.

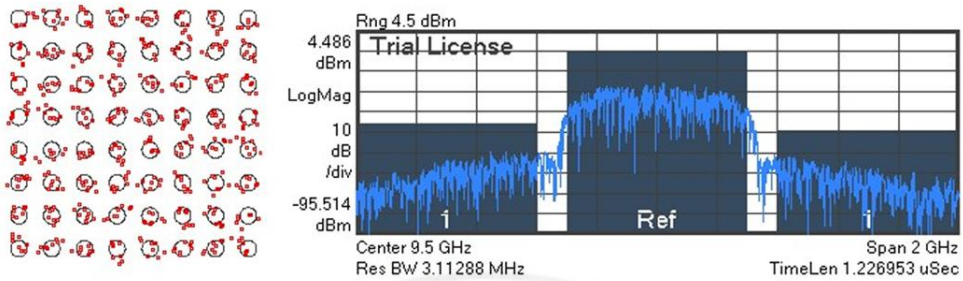


Figure 4.3-8 Measured constellation diagram and Spectrum Analysis at 9.5 GHz with 500 MHz baud rate 64-QAM signal

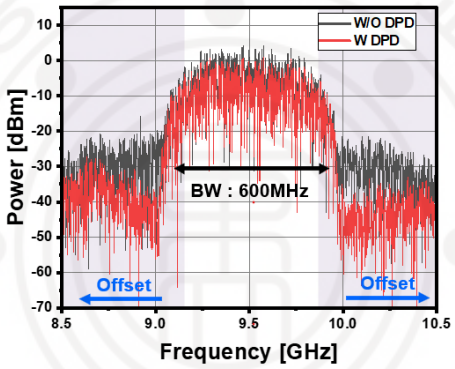


Figure 4.3-9 Measured spectrum with and without Digital predistortion.

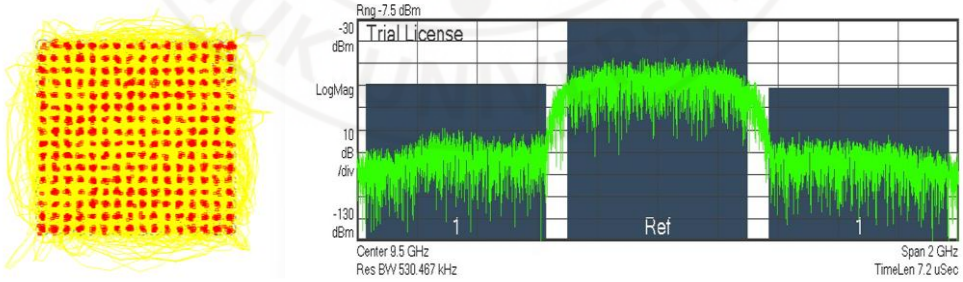


Figure 4.3-10 Measured constellation diagram and Spectrum Analysis at 9.5 GHz with 600 MHz baud rate 256-QAM signal with digital predistortion (DPD)

4.3.4 Reliability test

4.3.4.1 Reliability test based on JEDEC standard

To guarantee robustness and long-term reliability, a High Temperature Operating Life (HTOL) and Highly Accelerated Stress Test (HAST) were conducted. The HTOL test was carried out in our laboratory using a temperature chamber, as shown in Fig. 4.3-11, while HAST was performed by a third-party laboratory specializing in the reliability testing, as shown in Fig. 4.3-12. HTOL was conducted at 145 °C for 380 hours on two samples, which is equivalent to the JEDEC standard condition of 125 °C for 1000 hours [16], using an activation energy of 0.7 eV. For HAST, following the JESD22-A110E.01 [17], three samples were tested at 130 °C and 85% relative humidity for 96 hours. It is noteworthy that if the measured output power or current decreased by more than 10% from the initial value, the PA was considered to have failed according to our failure criteria. Fig. 4.3-13 and Fig. 4.3-14 show the output fluctuation for HTOL and HAST, respectively. No failures were observed for either HTOL or HAST. Based on the HTOL data and the zero-failure χ^2 method with a 60% confidence level, the MTTF at 50 °C was estimated to be 2.5×10^5 hours [18].

Figure 4.3-11 HTOL test setup

1 Qualification Plan and Results

The purpose of these tests is evalution (or monitoring) of CMOS 전력증폭기.
Test conditions are specified in customers in - house test plan all test procedures comply with JEDEC standards.
Obligation to perform exact procedure to reference documents is QRT Inc. responsibility only, but establishing failure criteria and judgment of pass/fail is customer's responsibility.

Test Items	Test Condition	Duration	Sample Size	Failed Unit [1]	Test Method [2]
Highly Accelerated Stress Test	130 °C ± 2 °C, 85 % ± 5 % R.H. / 230 kPa VDD = 0.45 V, VBB = 1.6 V, VCC = 3 V, VREF = 3.3 V	96 hrs	3 ea	0	JESD22-A110E.01:2021 (HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST(HAST))

Additional Requirement : N/A

Note :

1) Test results are based on the "Final Test Result" provided by customer.
2) Although the name of test item is same, reference documents can be JEDEC
3) "This laboratory is not accredited for the test results " * " marked."

Figure 4.3-12 HAST test report

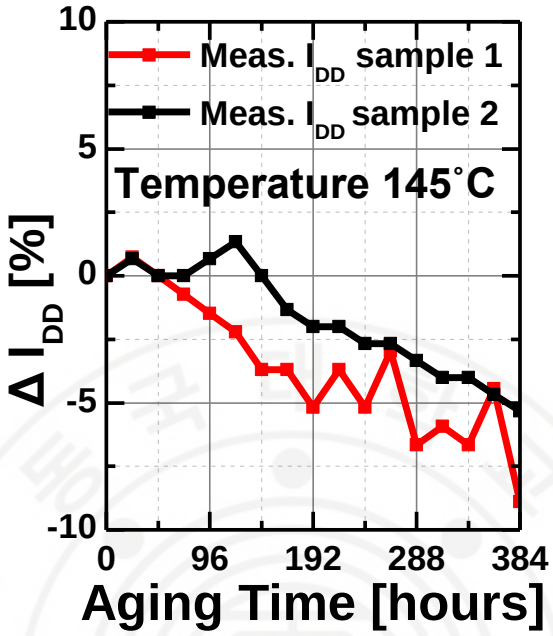


Figure 4.3-13 Measured I_{DD} fluctuation during HTOL test

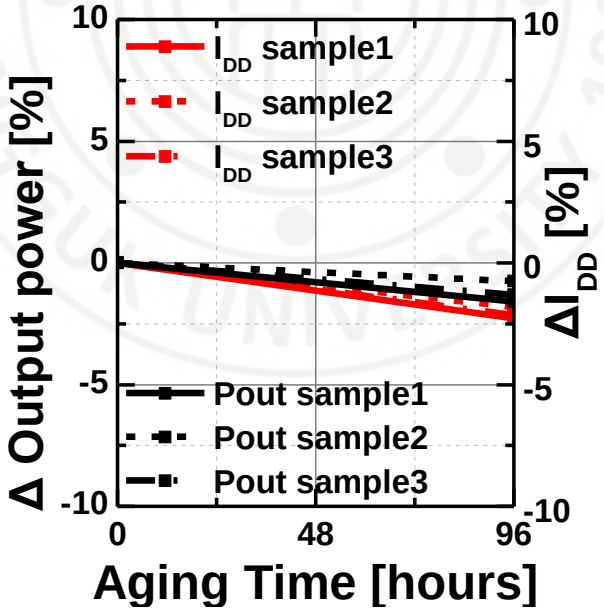


Figure 4.3-14 Measured I_{DD} and Pout fluctuation during HAST

4.3.4.2 RF overdrive Test

To validate the robust operation of the proposed PA utilizing the hybrid three-stack structure, a series of aging tests were also conducted. The PCB with JIG used for the reliability test is shown in Fig. 4.3-15.

The return loss aging test was performed with an input power level of 10 dBm, corresponding to the saturation point, over a 100-hour operational period. As illustrated in Fig. 4.3-16, the S11 and S22 measurements at the beginning and end of the test show negligible variation, confirming stable impedance matching throughout.

Also, an output power aging test was carried out by operating the PA under a 10 dBm input power level for 100 consecutive hours. The results, depicted in Fig. 4.3-17, indicate no breakdown occurred, with very marginal degradation observed in the saturated output power. In contrast, conventional power amplifier structures demonstrated significant performance degradation under shorter aging test durations, as reported in [19]. These observations demonstrate the enhanced robustness and reliability of the proposed hybrid stacking approach, which effectively mitigates the impact of hot carrier injection. The advancement ensures the suitability of the

proposed CMOS PA with hybrid stacks for long-term operation in high-performance applications operating under relatively high supply voltage conditions.

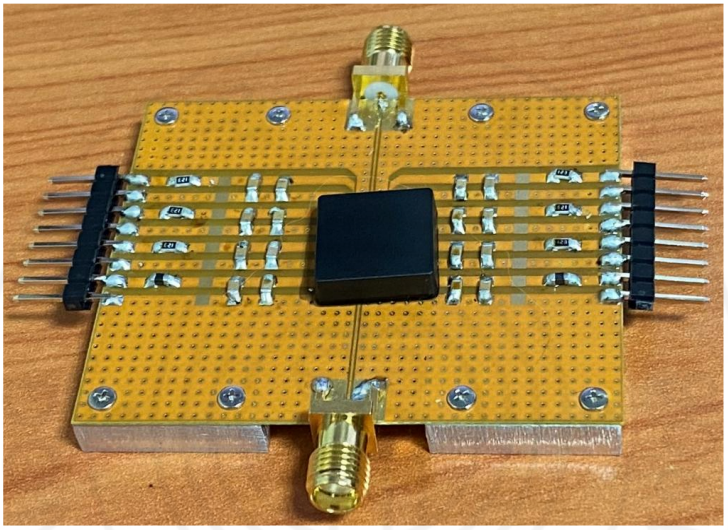


Figure 4.3-15 PCB with JIG for the reliability test

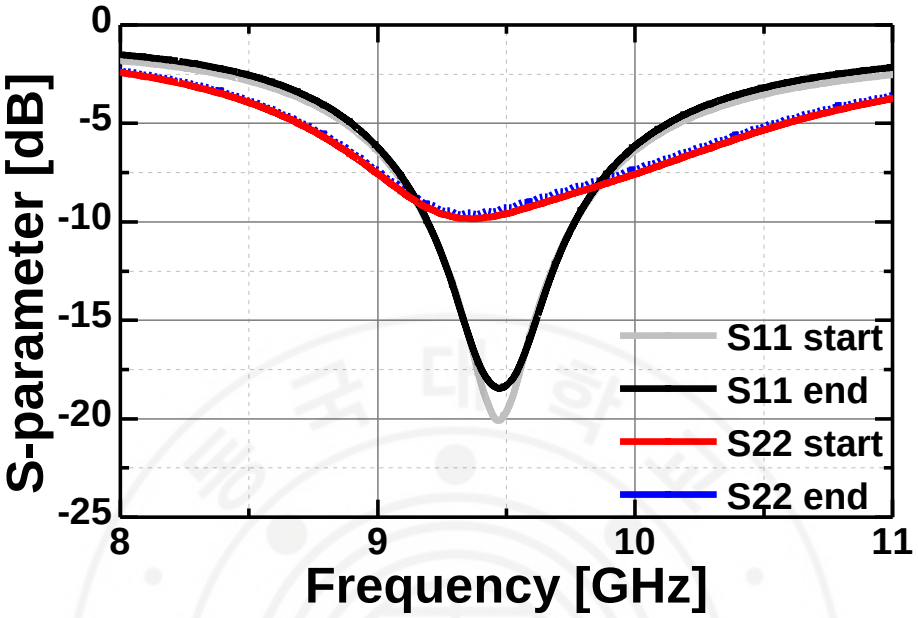


Figure 4.3-16 Comparison of S_{11} and S_{22} before and after 100 hours of return-loss aging test with 10dBm input power under 3.3V supply.

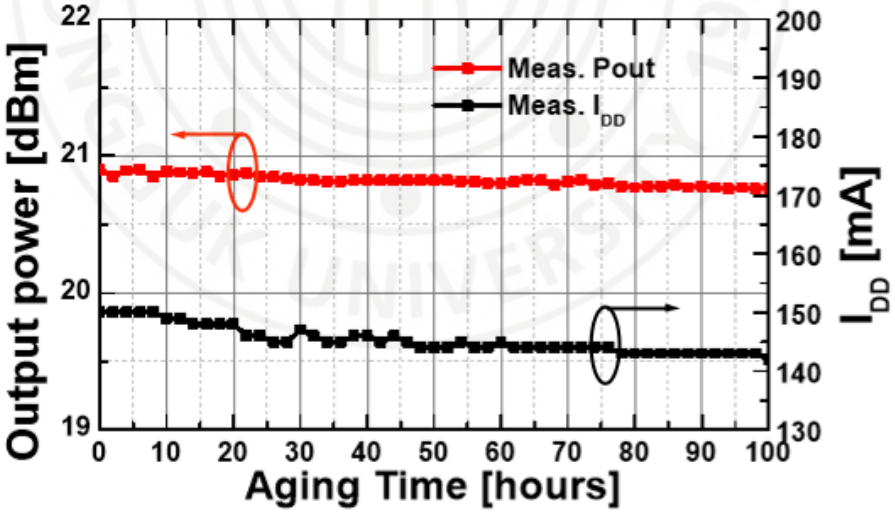


Figure 4.3-17 Measured Output power and drain current during 100 hours of the consecutive aging test with 10dBm input power under 3.3V supply.

Chapter 5. D-band Power Amplifier Design

5.1 Concept of Dual-peaking G_{max} structure

Designing amplifiers for sub-THz frequencies in CMOS technology presents several challenges. As operating frequencies approach the half of the maximum oscillation frequency (fmax) of active devices, the intrinsic gain of transistors decreases significantly, making it difficult to achieve sufficient power gain. This issue is further compounded by the high losses associated with input and output matching networks, often resulting in a total power gain close to or even below unity.

To address these challenges, various techniques have been proposed, including maximum achievable gain (G_{max}) boosting through linear, lossless, and reciprocal (LLR) embedding networks. However, this G_{max}-based amplifier typically exhibit gain enhancement sharply at specific target frequency, resulting in narrow bandwidth limitations. To cover a wider frequency range, wideband amplifiers such as distributed or stagger-tuned structures have been explored, but these designs often suffer from lower gain, larger chip area, and higher power consumption due to their design complexity.

Therefore, the dual-peaking G_{max} technique has been investigated as a promising solution to these challenges [10], as illustrated in Fig. 5.1-1. This approach simultaneously generates peaks at two distinct frequencies, enabling the maintenance of wide bandwidth and high gain, thereby greatly enhancing its suitability for high-performance RF systems such as transmitters. While [10] realizes the dual-peaking effect using a long transmission line in a single-ended amplifier configuration, the approach presented in this thesis employs a negative capacitance-based implementation compatible with differential architectures. This method enables the implementation of dual-peaking G_{max} technique in a more compact and integrable layout by eliminating the need for physically long structures.

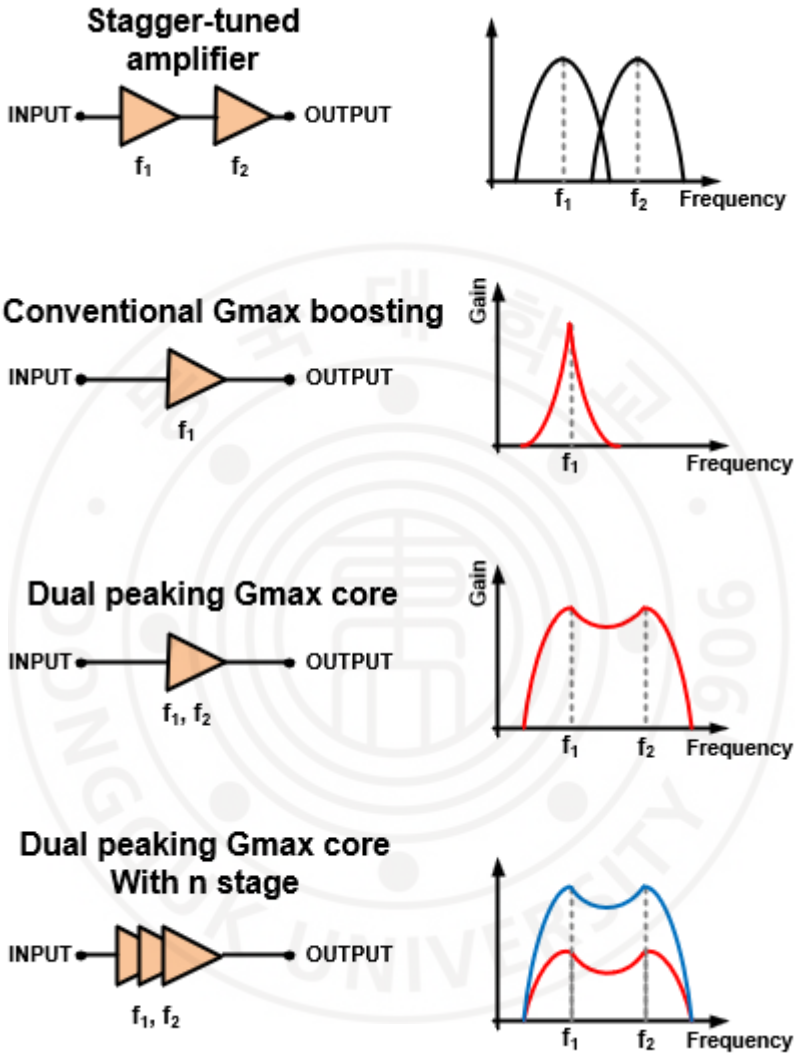


Figure 5.1-1 Circuit schematic and gain performance of various structures

5.2 Design approach of Dual-peaking Gmax structure

With a properly designed feedback network represented by the LLR embedding network, the maximum achievable gain can be expressed as:

$$G_{\max} = 2U - 1 + 2\sqrt{U(U-1)} \qquad \textbf{(5.2.1)}$$

When $K = 1$, $phase\left(\frac{Y_{21}}{Y_{12}}\right) = \pi$, G_{max} becomes 4U, with K representing Rollett's stability factor and U representing unilateral gain. This G_{max} boosting technique can be achieved at two frequencies simultaneously by utilizing an appropriate embedding network.

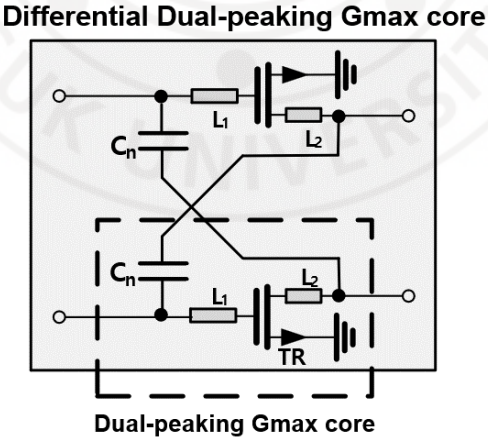


Figure 5.2-1 Schematic of proposed Dual-peaking G-max boosting structure

However, achieving both conditions simultaneously is often not feasible, as analysis in [20] shows that G_{max} is more dependent on the K-factor than on the phase of the LLR structure. To achieve wideband performance, focusing on making stability factor unity, G-max boosting was targeted at 130 GHz and 150 GHz, with a center frequency of 140 GHz. The proposed dual-peaking G-max boosting core is illustrated in Fig. 5.2-1. Using transmission line at gate, drain node with length of L_1 and L_2, phase condition can be achieved and over-neutralization capacitor between gate and opposite drain makes K=1. Y-parameter of transmission and transistor can be modeled as following equation:

$$Y_{L_i} = \frac{1}{Z_0}\begin{pmatrix} \frac{1}{\tanh(\gamma L_i)} & -\frac{1}{\sinh(\gamma L_i)} \\ -\frac{1}{\sinh(\gamma L_i)} & \frac{1}{\tanh(\gamma L_i)} \end{pmatrix} \quad \textbf{(5.2.2)}$$

$$Y_{TR} = \begin{pmatrix} Y_{11TR} & Y_{12TR} \\ Y_{21TR} & Y_{22TR} \end{pmatrix} \quad \textbf{(5.2.3)}$$

Where Z_0 is the characteristic impedance of transmission line and Y_{TR} is transistor's intrinsic Y-parameter. Using this Y-parameter and considering over-neutralization capacitor value, the equivalent

Y-parameter of the Dual-peaking G_{max} structure are derived as follows, which allows for the calculation of G_{max} and the K-factor [21][22].

$$Y_{11} = -\frac{(Y_{22TR} + Y_{11L2}) \cdot Y_{12L1} \cdot Y_{21L1}}{(Y_{22L1} + Y_{11TR})(Y_{22TR} + Y_{11L2}) - Y_{12TR} \cdot Y_{21TR}} + Y_{11L1} - j\omega C_n \quad \textbf{(5.2.4)}$$

$$Y_{12} = -\frac{Y_{12TR} \cdot Y_{12L1} \cdot Y_{12L2}}{(Y_{22L1} + Y_{11TR})(Y_{22TR} + Y_{11L2}) - Y_{12TR} \cdot Y_{21TR}} + j\omega C_n \quad \textbf{(5.2.5)}$$

$$Y_{21} = -\frac{Y_{21TR} \cdot Y_{21L1} \cdot Y_{21L2}}{(Y_{22L1} + Y_{11TR})(Y_{22TR} + Y_{11L2}) - Y_{12TR} \cdot Y_{21TR}} + j\omega C_n \quad \textbf{(5.2.6)}$$

$$Y_{22} = -\frac{(Y_{11TR} + Y_{22L1}) \cdot Y_{12L2} \cdot Y_{21L2}}{(Y_{22L1} + Y_{11TR})(Y_{22TR} + Y_{11L2}) - Y_{12TR} \cdot Y_{21TR}} + Y_{22L2} - j\omega C_n \quad \textbf{(5.2.7)}$$

Theoretically, dual-peaking can be achieved with various combinations of L_1, L_2, and C_n. However, L_2 was fixed in this design due to its placement on the drain side, where extending its length could lead to significant voltage drop and increased power loss, degrading PA performance. Keeping L_2 short minimizes these adverse effects, ensuring efficient power delivery to the output stage. In contrast, C_n directly affects G_{max} and the K-factor, requiring dynamic adjustments to achieve optimal gain and stability, rather than setting it to a fixed value. Therefore, fixing L_2 is the optimal choice as it simplifies the design and optimizes power delivery efficiency

compared to fixing L_1 or C_n. The intersection of the two graphs in Fig. 5.2-2 indicates the theoretical feasibility of dual-peaking boosting. However, practical implementation is not feasible because when K equals unity, the real part of the source and load admittances in the embedding network becomes zero, as shown in the equations [23] as below.

$$y_s = \frac{|y_{12}y_{21}|\sqrt{K^2-1}}{2|G_{22}|} + \frac{j\left[\mathrm{Im}(y_{12}y_{21}) - 2G_{22}B_{11}\right]}{2G_{22}} \quad \textbf{(5.2.8)}$$

$$y_L = \frac{|y_{12}y_{21}|\sqrt{K^2-1}}{2|G_{11}|} + \frac{j\left[\mathrm{Im}(y_{12}y_{21}) - 2G_{11}B_{22}\right]}{2G_{11}} \quad \textbf{(5.2.9)}$$

To enhance stability and feasibility, the design points of 130 GHz and 150 GHz were adjusted to 120 GHz and 160 GHz, providing additional margin to the K-factor. The L_1 and C_n values were selected to maximize the G_{max} value, as shown in Fig. 5.2-3. The implemented Dual-peaking G_{max} core achieved high gain and wide bandwidth than conventional common-source amplifier as illustrated in Fig. 5.2-4.

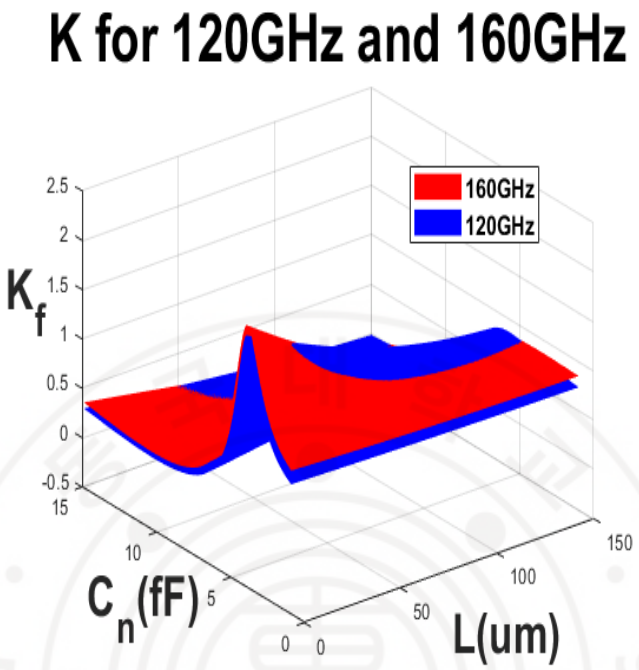


Figure 5.2-2 K value related to C_n and L_1

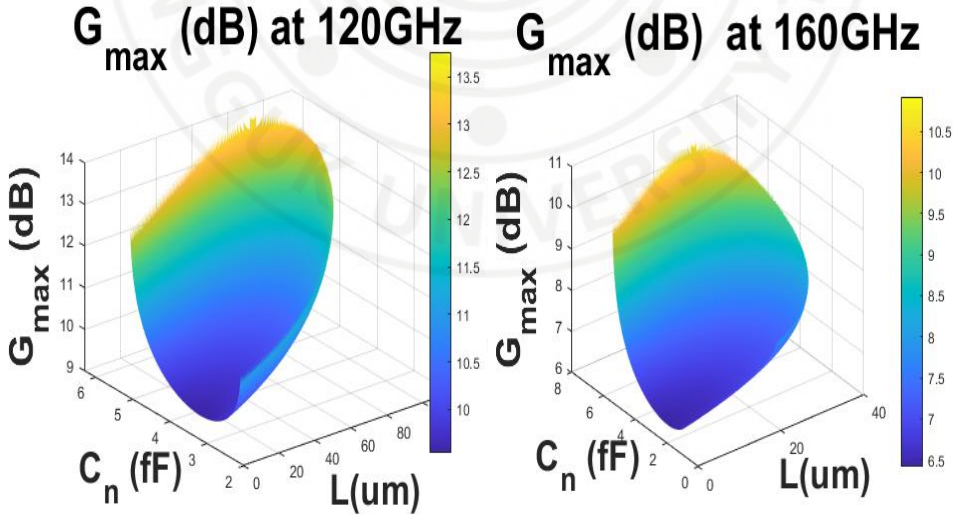


Figure 5.2-3 G_{max} value related to C_n and L_1

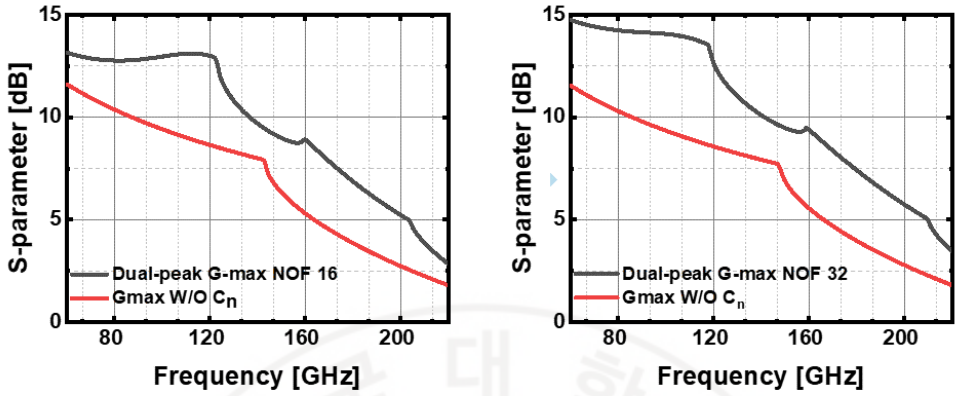


Figure 5.2-4 Simulated Gma of the proposed dual-peak Gmax core

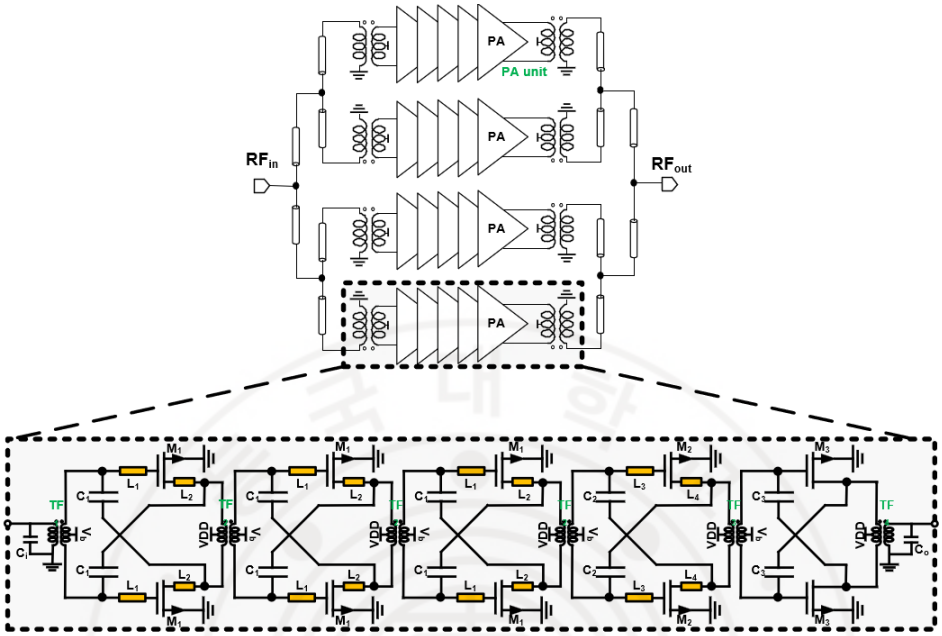
5.3 Circuit Implementation in 40nm bulk CMOS

5.3.1 Circuit design

The subsequent steps in the design process are is illustrated in Fig. 5.3-1: the 5-stage 8-way power amplifier are designed to achieve high gain and high output power. From the first to fourth stage, dual-peaking G-max boosting technique was applied to achieve high gain and wide bandwidth. However, it was not used in the output stage because the increased neutralization capacitance could degrade large-signal performance, leading to reduced output power and efficiency [15].

Instead, a cascaded balun with flat intrinsic loss characteristics was employed at the output stage to achieve wideband output performance, overcoming the narrowband limitations caused by the self-resonant frequency of conventional baluns in 40nm CMOS [24]. An active device size of 64 μm was utilized at the output stage, while the transistor sizes in the preceding stages were set to half of those in the subsequent stages, optimizing power delivery and current consumption. Fig. 5.3-2 presents the output power contour of the output device under the conditions of VDD=1.2V, Vbias = 0.6V and an input power of 0dBm.

The PA consumes 455 mA with V_{DD} = 1.2V and its gate bias at 0.6V, balancing power-added efficiency and output power trade-offs. The four PA units were combined using an MSTL-based current mode power combiner. Fig. 5.3-3 shows the output network impedance as a function of frequency from 100 GHz to 200 GHz. At 140 GHz, the output matching network achieves a near-50 Ω impedance, indicating proper matching to a 50 Ω system.



M$_1$	C$_1$	L$_1$	C$_i$	TF$_1$	TF$_2$	TF$_3$	TF$_4$
16 µm(W) / 40 nm(L)	7.5 fF	121 um	14.5 fF	L$_P$:74.05pH L$_S$:84.69pH k:0.777 Q$_p$:13.99 Q$_s$:10.93	L$_P$:82.44pH L$_S$:29.12pH k:0.462 Q$_p$: 12.98 Q$_s$:11.06	L$_P$:40.19pH L$_S$:33.12pH k:0.394 Q$_p$: 15.26 Q$_s$:11.37	L$_P$:59.3pH L$_S$:86.3pH k:0.54 Q$_p$: 11.9 Q$_s$: 6.76
M$_2$	C$_2$	L$_2$, L$_4$	C$_o$				
32 µm(W) / 40 nm(L)	13.6 fF	3um	23 fF				
M$_3$	C$_3$	L$_3$	VDD/V$_b$				
64 µm(W) / 40 nm(L)	18fF	88um	1.2V/0.6V				

Figure 5.3-1 Schematic and design parameter of proposed 5-stage 8-way power amplifier in 40nm bulk CMOS

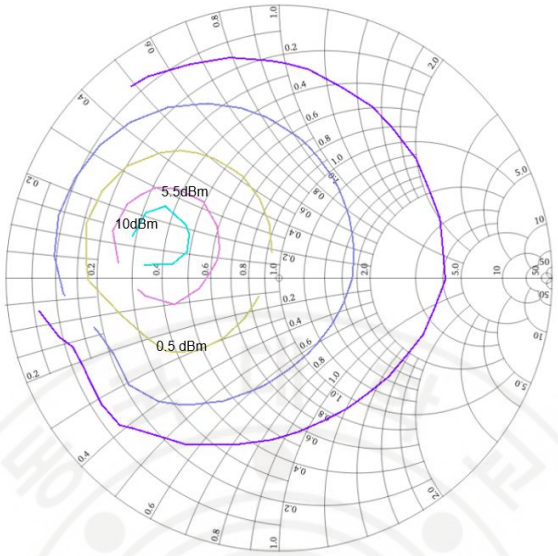


Figure 5.3-2 Power contour of output device (device width: 64um) under V_{DD}=1.2V, Vbias = 0.6V and input power is 0dBm. (output power step: 5dBm)

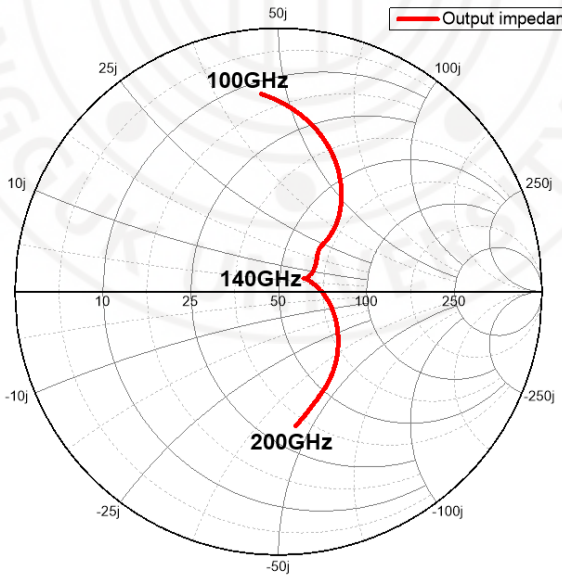


Figure 5.3-3 Simulated output network impedance versus frequency

5.3.2 Layout implementation

In D-band design, accurate simulation considering its layout structure is essential due to considering frequency shift which can affected by parasitic during layout level. For accurate simulation, the dual-peaking structure is simulated using HFSS simulation, as illustrated in Fig. 5.3-4 and Fig. 5.3-5. The M2 metal is used as ground plane for the L_1 and L_2.

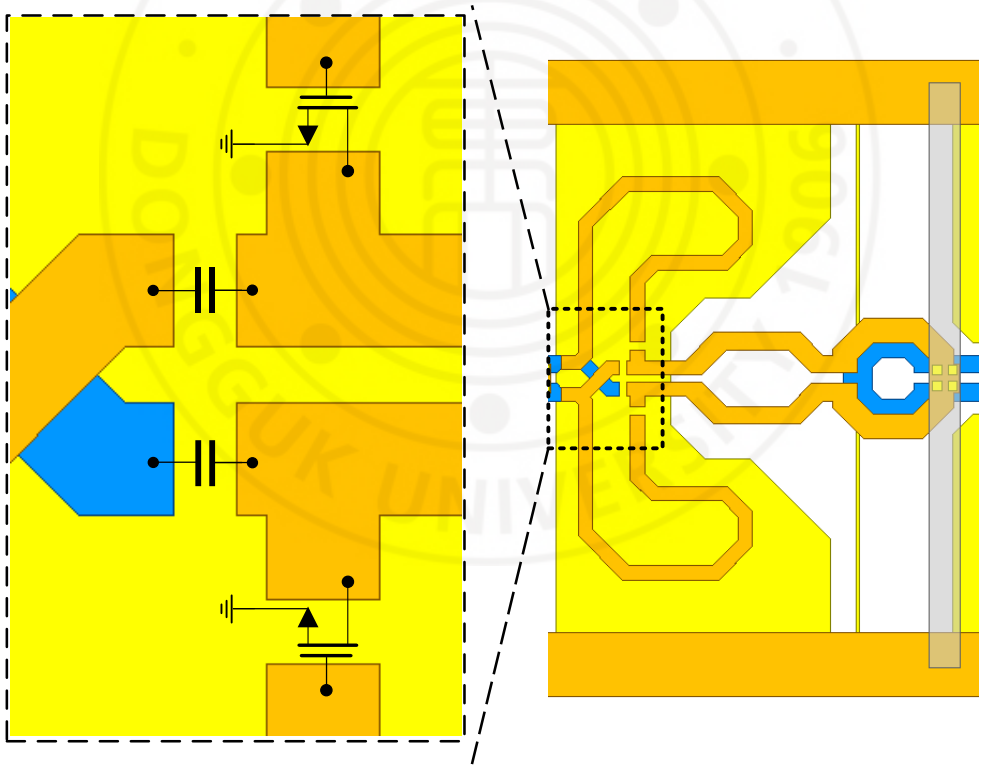


Figure 5.3-4 Implementation of Dual-peaking structure

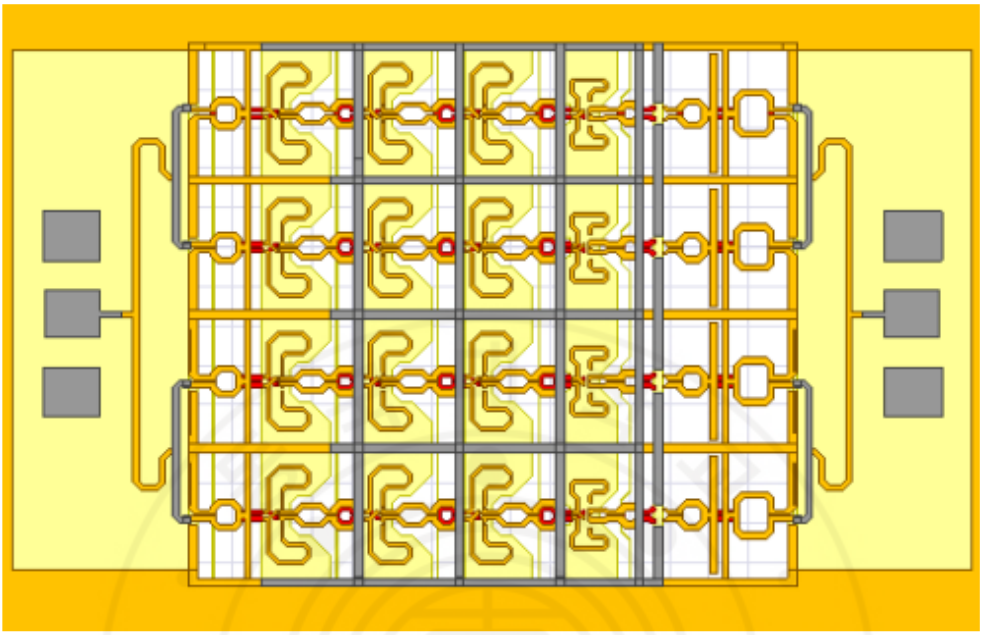


Figure 5.3-5 HFSS simulation setup

5.3.3 Chip photograph

The five-stage eight-way D-band power amplifier is proposed. Fig. 5.3-6 shows the chip photo of the fabricated PA. The total chip area of the PA is 0.915 mm², and the core area, excluding pads, is 0.524 mm².

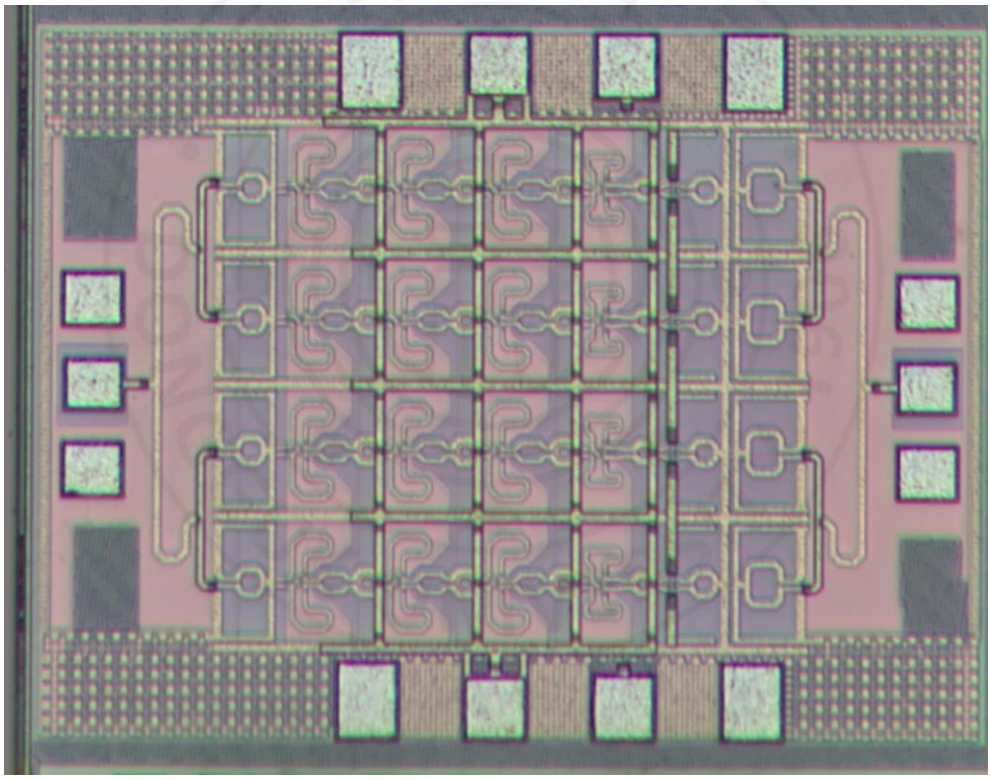


Figure 5.3-6 Chip photograph of D-band PA

5.4 Measurement

5.4.1 Small signal

5.4.1.1 Small signal measurement set up

The proposed PA was fabricated in 40nm Bulk CMOS technology. Fig. 5.4-1 shows the measurement setup. For the S-parameter measurement, Keysight PNA N5244B connected with WR6.5 VDI network analyzer extension modules were utilized. The calibration was done using the GGB CS-5 calibration substrate.

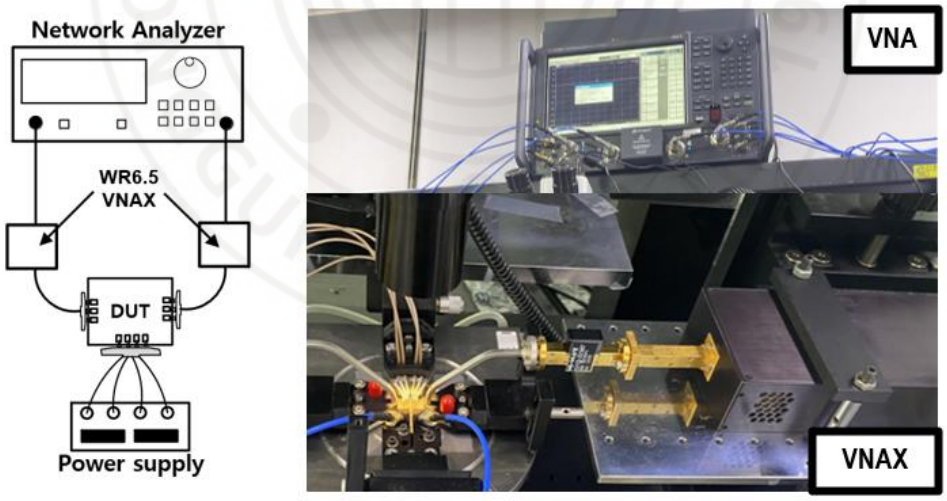


Figure 5.4-1 Small signal measurement setup

5.4.1.2 Small signal measurement result

In Fig. 5.4-2, S21 achieve dual peaking at 128GHz and 152GHz and 3-dB bandwidth based on 140 GHz is over 35 GHz. The measured input and output return losses were better than 10 dB from 110 GHz to 170 GHz, and 130 GHz to 170 GHz, respectively. For stability check, Fig. 5.4-3 shows K-delta result which guarantees unconditionally stable across the whole frequency band.

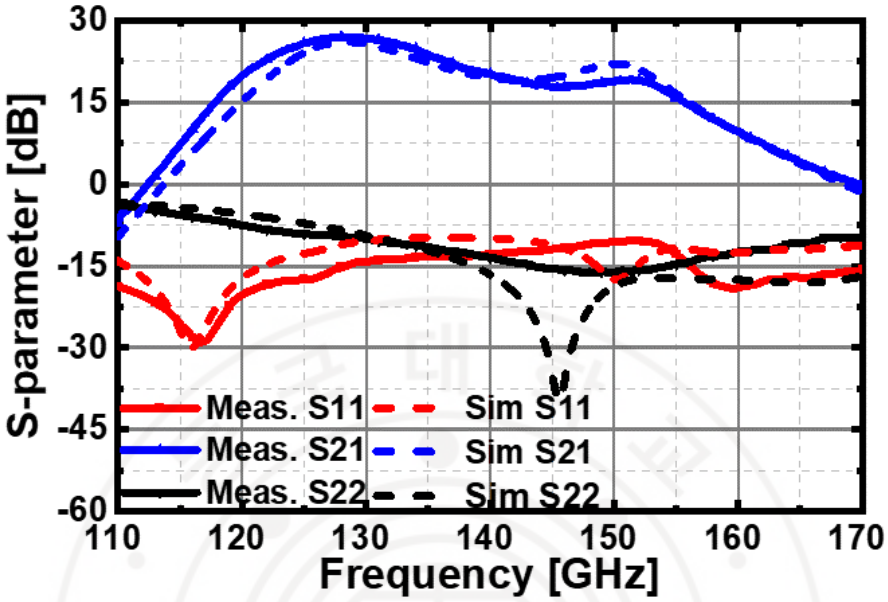


Figure 5.4-2 Simulated and measured results of S-parameters

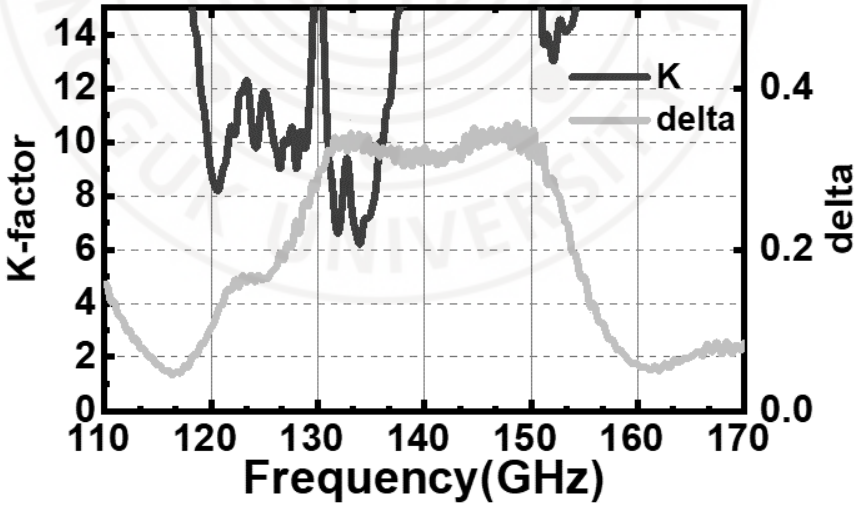


Figure 5.4-3 Measured results of K&delta

5.4.2 Large signal

5.4.2.1 Large signal measurement set up

Fig. 5.4-4 shows the measurement setup. For large-signal measurement, PNA combined with the D-band extender was employed to generate a continuous wave signal in D-band, which is injected into the PA via a tunable attenuator for input power control. Output power was measured using the power sensor and Erickson Power Meter (PM5).

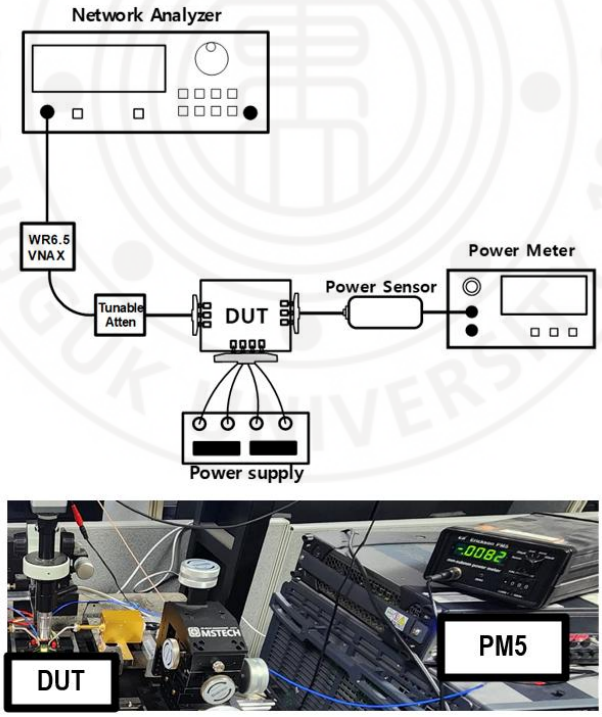


Figure 5.4-4 Large signal measurement setup

5.4.2.2 Large signal measurement result

Fig. 5.4-5 and Fig. 5.4-6 show large-signal measurement data. The measured saturation power is 14.6 dBm at 128 GHz, 13 dBm at 152 GHz, with peak PAE of 4.74% and 3%, respectively.

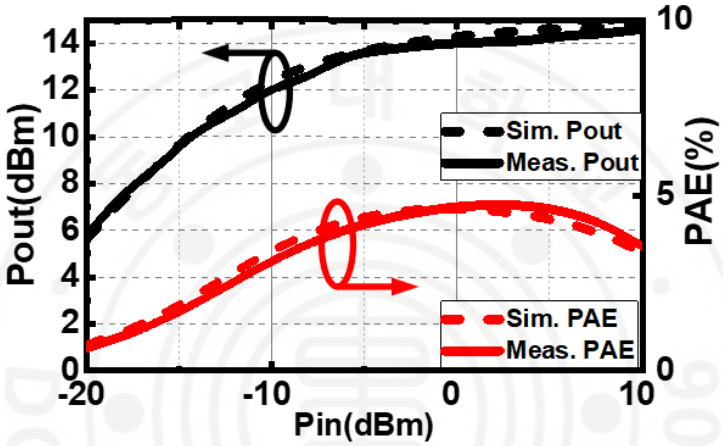


Figure 5.4-5 Simulated and measured results of output power and power added efficiency

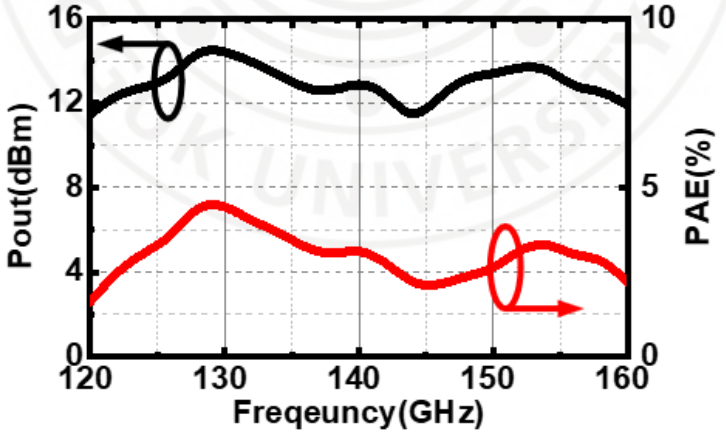


Figure 5.4-6 Measured Psat and PAE versus frequency

5.4.3 Comparison with other work in D-band

This PA achieves the highest Figure of Merit (FOM) compared with other state-of-art BULK CMOS PAs, which is 90.28.

Table 5.4-1 State-of-Art PAs in D-band

	Topology	Tech	VDD (V)	Freq (GHz) BW (GHz)	Gain (dB)	OP1dB (dBm)	P_{sat} (dBm)	PAE (%)	Area (mm^2)	FOM**
This	5S-8W	40nm CMOS	1.2V	128	27	10.1	14.6	4.74	0.915	90.28
				140 :35	20.2	8.1	13.1	3.2		81.3
				152	19.1	7.8	13.7	3.3		81.6
[24] MWTL 24	3S-8W	40nm CMOS	1.2	132: 18	14.5	12.3	16.4	7.2	0.72	81.8
[25] TCAS II 19	3S-4W	40nm CMOS	1.2	120 :38.5	16	9.3	14.6	9.4	0.33	81.9
[26] TMTT 23	3S-4W	28nm CMOS	1	138 :27.5***	19.2	11.2	15.4	14.25	0.091*	88.9
[27] RFIC 18	3S-4W	40nm CMOS	1	140 :17	20.3	10.7	14.8	8.9	0.34	87.5
[28] ACCESS 21	3S-2W	28nm CMOS	1	135 :20	21.9	N/A	11.8	10.7	0.24*	86.6
[29] TCAS I 20	4S-2W	28nm CMOS	0.9	132: 22	22.5	5.2	8	6.6	0.026*	81.1
[30] JSSC 22	4S-8W	45nm RF SOI	1.2	140: 21	24	14.2	17.5	13.4	0.43	95.7
[31] MWTL 24	4S-2W	28nm CMOS	0.9	160	21.9	4.6	9.5	7.6	0.26	84.3
[32] TCAS I 24	4S-2W	40nm CMOS	1	130 :22	23.5	8.2	13.2	9.1	0.34	88.5

*Core only **FOM =Psat[dBm]+Gain[dB]+20log(freq[GHz])+10log(PAEmax[%]) ***Estimated value

Chapter 6. Conclusion

This thesis demonstrates two PA designs that employ different techniques to overcome the inherent limitations of CMOS in the X-band and D-band. In the X-band design, a stacked structure achieves a power gain of 23.2 dB, a 3 dB bandwidth of 1 GHz, a peak PAE of 24%, and a saturated output power of 20.9 dBm. Under 256-QAM modulation, it maintains an EVM below −35 dB and an ACPR of −33.5 dBc. Reliability evaluation following JEDEC standards predicts an MTTF over 28 years at a 3.3 V supply, and continuous 100 hours RF overdrive test shows stable operation for high input power.

For the D-band, the dual-peaking G_{max} boosting technique is applied to achieve 27 dB of gain, a 3 dB bandwidth exceeding 35 GHz, and a saturated output power of 14.6 dBm. This represents the highest figure of merit among recently reported bulk CMOS PAs in this frequency range.

These measurement results illustrate how the proposed approaches effectively mitigate CMOS limitations and enhance overall performance, making the presented PAs well-suited for future high-speed communication systems, including next-generation 6G applications.

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국문 초록

전력증폭기 설계에서는 충분한 출력전력을 보장하는 것은 물론, 소형화, 저전력 소비, 저비용 등의 다양한 요구사항을 동시에 만족시켜야 한다. 특히, CMOS 공정을 이용한 전력증폭기 설계에서는 출력전력의 한계와 낮은 임피던스로 인한 매칭의 어려움이 주요한 설계 과제로 꼽힌다. 본 연구에서는 실리콘 기반의 65nm 및 40nm CMOS 기술을 활용하여 다양한 기법을 적용한 전력증폭기 설계를 제안한다. 40nm CMOS 공정에서는 전력증폭기의 이득을 극대화하기 위해, 피드백 구조를 기반으로 한 Dual-Peaking Gmax 기법을 적용하였다. 이를 통해 높은 주파수 대역에서 넓은 대역폭과 높은 이득 특성을 확보할 수 있도록 설계되었다. 한편, 65nm CMOS 공정에서는 출력전력을 향상시키고 전력 부가 효율을 극대화하기 위해 3개의 MOSFET을 직렬(Stacked)로 연결한 전력증폭기 구조를 채택하였다. 이 설계는 트랜지스터 간 전압 분배를 통해 높은 전압 구동이 가능하도록 하여, 기존의 CMOS 전력증폭기 대비 우수한 성능을 보일 수 있도록 하였다. 본 연구를 통해 제안된 전력증폭기 설계 기법은 고주파 대역에서 높은 출력전력과 전력 효율을 동시에 확보할 수 있는 효과적인 솔루션을 제공할 것으로 기대된다. 또한, CMOS 기반 무선 통신 시스템에서의 실용적인 적용 가능성을 높이는 데 기여할 수 있을 것이다.