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Master' Thesis

Design of a 250nm GaN Monolithic
Transceiver and Study on the
Applicability of a Radar/Communication
Dual-Use System with DPD and Code
Optimization

Advisor: Professor Jung-Dong Park

Graduate School, Dongguk University
Department of Electronics and Electrical
Engineering

Tae-Hoon Kim

2025

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Abstract

This thesis presents the design of an integrated X-band transceiver in a 250 nm GaN HEMT process utilizing the memory polynomial digital predistortion (DPD) and Simulation Annealing (SA)-based code optimization to improve the Peak Sidelobe Ratio (PSLR) in dual function radar and communication (DFRC) systems. The proposed transceiver integrates a power amplifier (PA), low-noise amplifier (LNA), and SPDT T/R switch to suppress nonlinear distortion and harmonic content inherent to GaN devices, second- and third-order harmonic filters are implemented using $\lambda/4$ transmission lines and LC resonators.

To further mitigate PSLR degradation caused by modulation complexity and PA nonlinearity, we applied simulation annealing (SA) optimization algorithm. This algorithm enables efficient code sequence optimization.

Additionally, memory polynomial-based digital predistortion (DPD) is applied to improve linearity under high-PAPR signals, especially for 16QAM.

In measurement, the fabricated transceiver achieved excellent measurement result with 41.5dBm of output power and 31.8% of PAE and 2.04dB of noise figure

In PSLR measurement results, it shows that the proposed code optimization and DPD techniques successfully reduced PSLR. These findings confirm that the proposed method effectively suppresses sidelobes, providing a viable solution for future dual function radar and communication (DFRC) system.

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Chapter I. Introduction

1.1 Research Background

In next-generation wireless platforms, dual function radar and communication (DFRC) systems have emerged as a key enabler for achieving both high-speed data transmission and high-resolution target detection within a unified hardware architecture [1–2]. These systems are increasingly important in applications such as autonomous vehicles, 6G mobile networks, aerospace, and defense [3–4]. By sharing the same RF front-end for both radar and communication functions, such systems significantly improve size, weight, and power efficiency. However, they must ensure simultaneously the signal quality requirements of both modes. In particular, time-domain autocorrelation performance, especially the suppression of sidelobes as quantified by the Peak Sidelobe Ratio (PSLR), is critical for ensuring accurate radar ranging and robust communication reliability [5–6]. Bad PSLR can lead to false alarms in radar detection and increased adjacent channel interference in communication, making its minimization essential in integrated systems [7].

To meet the stringent performance requirements of

radar/communication co-design, Gallium Nitride (GaN) technology have become the preferred choice due to their high-power density and efficiency [8]. However, GaN devices exhibit strong nonlinear behavior caused by trapping effects and self-biasing phenomena, which degrade linearity, especially under high Peak-to-Average Power Ratio (PAPR) signals such as 16QAM [9]. These modulation schemes are used in radar and communications integrated systems for their spectral efficiency and throughput advantages [10]. Nonetheless, their use in conjunction with nonlinear amplifiers leads to AM-AM and AM-PM distortion, which deteriorates PSLR. This nonlinear distortion not only undermines radar detection accuracy but also reduces communication quality by increasing Error Vector Magnitude (EVM) and adjacent channel leakage [11].

This thesis proposes an integrated approach that combines signal processing and hardware techniques to improve the PSLR in radar/communication integrated systems. First, the design and implementation of an X-band GaN transceiver are presented. In the transceiver, the power amplifier (PA), low-noise amplifier (LNA), and T/R switch are integrated into a single chip. To suppress radiation of the harmonics at the output of the transmitter, hardware-based filtering techniques using quarter-wavelength transmission

lines and LC resonators are employed for second and third harmonic rejection. In addition, modulation-specific code sequence optimization for QPSK and 16QAM is conducted using the Simulated Annealing algorithm. Finally, digital predistortion (DPD) is applied to compensate for the nonlinear characteristics of the GaN amplifier, thereby restoring linearity and improving overall system performance. Through frequency- and time-domain measurements, this thesis demonstrates that the proposed methodology effectively enhances PSLR and provides a practical solution for future integrated transceiver designs for DFRC systems.

1.2 Gallium Nitride (GaN) technology

The Gallium Nitride (GaN) technology has emerged as a cornerstone for modern radar and communication systems, particularly in applications requiring high output power, wide bandwidth, and compact integration [12]. Compared to traditional GaAs and Si-based technologies, As can be seen in Table 1, GaN offers several distinct advantages most notably, its wide bandgap, high breakdown voltage, high saturation velocity, and excellent thermal conductivity. These properties enable GaN devices to operate reliably under high voltage and high-power conditions, making them ideal for PAs and switches in X-band [13]. In DFRC transceivers, GaN HEMTs provide the necessary power density and efficiency to meet stringent performance requirements without relying on bulky limiters or circulators.

One of the most critical strengths of GaN lies in its robustness against high voltage operation. The AlGaN/GaN heterostructure forms a high mobility two-dimensional electron gas (2DEG) channel, enabling both high current handling and low on resistance [14]. This allows RF front-end modules, such as PAs and SPDT T/R switches, to withstand peak powers exceeding 40 dBm while maintaining

insertion losses below 1 dB. Moreover, GaN technology's compatibility with silicon carbide (SiC) substrates offers superior thermal conductivity, helping to efficiently dissipate heat generated during high-power operation. This thermal advantage is particularly important for ensuring device reliability in compact monolithic microwave integrated circuit (MMIC) designs where power density is high [15].

Despite these advantages, GaN HEMTs inherently suffer from nonlinear behaviors such as trapping effects, which can lead to gain compression, phase distortion, and memory effects particularly under high PAPR signals like QAM [16]. These nonlinearities originate from electron trapping at surface and bulk defect sites, which cause gate-lag and drain-lag effects, shifting the device's quiescent point during operation [17].

Property	Si	SiC	GaAs	GaN
Energy bandgap [eV]	1.12	3.2	1.43	3.5
Breakdown field [10^6 V/cm]	0.3	3.2	0.4	3
Electron mobility [$\text{cm}^2/\text{V} \cdot \text{S}$]	1450	700	8500	1250
Saturation velocity [10^5 m/s]	1	2.0	1.2	2.5
Thermal Conductivity [W/cm · K]	1.31	4.9	0.46	1.5

<Table 1.2–1> Properties comparison of various semiconductor materials.

1.3 Pulse Compression Technique

A Pulse–Doppler radar system needs to minimize the PSLR in the time domain autocorrelation to accurately detect high–speed targets and precisely measure range [18]. If the PSLR is high, strong side lobes form around the main lobe, which increases false alarms and degrades target resolution [18]. To address these issues, pulse compression has been introduced as a key technique. By applying phase or frequency modulation, pulse compression effectively suppresses side lobes in the whole system, thereby ultimately reducing the PSLR [19].

Among the various phase modulation techniques available for pulse compression, BPSK is the most straightforward to implement. To achieve uniform sidelobe suppression, the Barker code was introduced [20]. One of its main benefits is its ability to reduce sidelobe levels without altering the signal amplitude. Nevertheless, a major drawback is its limited length, as the maximum achievable pulse compression ratio is capped at 13 [20]. In addition to Barker codes, other sequences such as polyphase codes and Zadoff–Chu sequences have been proposed. Yet, as the sequence length increases, these codes often contain phase values incompatible with

higher-order modulation formats, rendering them unsuitable for such use cases [21–23].

To address the inherent limitations of traditional code types, advanced modulation schemes with higher orders can be employed. QPSK, for instance, offers twice the spectral efficiency of BPSK by allowing independent modulation of both the in-phase (I) and quadrature (Q) components [24]. This parallel encoding approach enables the transmission of double the amount of information over the same bandwidth, thereby greatly enhancing spectral utilization [25]. Furthermore, QPSK supports arbitrary code lengths without constraint and maintains a PAPR as low as 0 dB.

QAM integrates both phase and amplitude modulation, allowing it to achieve higher spectral efficiency than schemes like QPSK, without being restricted by code length L [26]. As a result, it produces a narrower main lobe and demonstrates improved adjacent channel power characteristics. Specifically, 16QAM tends to yield a lower PSLR. Moreover, in radar-communication co-design systems, 16QAM enables greater data throughput than BPSK or QPSK due to its increased modulation order and information density.

Accordingly, there is a need to design tailored code sequences capable of minimizing the PSLR when employing higher-order modulation formats like QPSK and 16QAM.

In QAM-based systems, the inclusion of amplitude modulation results in a non-zero PAPR, which leads to power inefficiencies during the pulse duration and may cause the PA to operate in its nonlinear region [27]. Additionally, QAM is susceptible to both AM-AM and AM-PM distortions.

To address these challenges, second- and third-order harmonic filters were integrated into the transceiver design. These filters effectively suppress radiation of the unwanted harmonic components at the transmitting antenna, thereby improving the PSLR of the radar system. Furthermore, DPD techniques were employed to enhance the linearity of the overall system. The combination of these approaches reduces signal distortion and boosts system performance when operating under QAM modulation.

1.4 Thesis Organization

In Chapter II, we present the design of an X-Band Transceiver utilizing a 250nm GaN process, optimized for DFRC systems with harmonic reduction filter.

Chapter III introduces simulation annealing optimization algorithm for code sequence optimizing. Subsequently, we applied this SA algorithms for code sequence optimization in QPSK and 16QAM systems, demonstrating their superiority through comparisons with existing methods and examples.

Chapter IV introduces memory polynomial DPD and it was applied to effectively compensate for the PSLR degradation caused by the nonlinearity of GaN HEMT and the amplitude modulation in 16QAM, and its effectiveness was verified through simulation.

In Chapter V, we present the measurement results of our designed Transceiver and experimentally validate the method proposed in Chapter III. The results confirm that the proposed approach significantly improves PSLR for each modulation scheme. Through this study, we demonstrate that our approach prevents PSLR degradation caused by hardware nonlinearities, thereby maximizing

radar detection range and reducing false alarm rates. In particular, the optimized code sequence for 16QAM provides an excellent foundational research resource for future integrated radar and communication systems.



Chapter II. X–Band GaN Transceiver Design

Figure 2(b) illustrates the architecture of the transceiver designed for DFRC systems. The receive chain integrates a T/R switch followed by a 4 stage LNA, while the transmit chain consists of a T/R switch and a 4–way power amplifier (PA). All components were implemented within a single MMIC using a commercial 0.25 μm GaN HEMT process.

In this technology, the GaN heterostructure is grown on a 100 μm silicon carbide (SiC) substrate using plasma–enhanced chemical vapor deposition (PECVD). The process offers two metal layers in the layout: Metal 1 (M1) with a thickness of 1.1 μm and Metal 2 (M2) with a thickness of 4 μm . The GaN HEMT devices used in this design exhibit a maximum oscillation frequency (f_{MAX}) of 76.7 GHz and a cut–off frequency (f_{T}) of 25 GHz. The peak transconductance reaches 370 mS/mm, and the device supports a power density of 5 W/mm. It delivers a current density of 100 mA/mm and sustains a breakdown voltage of 120 V. Additionally, the minimum noise figure (NF) is measured to be 0.5 dB at 9 GHz.

2.1 X-Band GaN Transmit/Receive Switch design

The transmit/receive (T/R) switch controls the routing of the RF signal according to the T/R control signal, directly impacting the overall transceiver's output power and noise figure (NF). When a Tx control signal is applied, the T/R switch routes the incoming RF signal to the power amplifier (PA) located before the switch. Conversely, it routes the signal to the receive path when the Rx control is active. Therefore, minimizing insertion loss between the Tx and Rx ports is essential for improving the signal to noise ratio (SNR) of the TRM. High isolation is also critical to suppress leakage between the Tx and Rx paths, which can otherwise damage the HEMT gate of the LNA depending on the application [28].

Because the T/R switch handles high power from the PA, high linearity is also required. To prevent performance degradation caused by the large output power of the PA, $\lambda/4$ TLs were inserted. The switch devices on the Tx and Rx paths operate in opposite states according to the control gate voltage. To maximize the voltage swing, the control voltage can be chosen between the pinch-off voltage (V_P) and the breakdown voltage (V_{BD}), which are -2.6 V and 120 V, respectively [29].

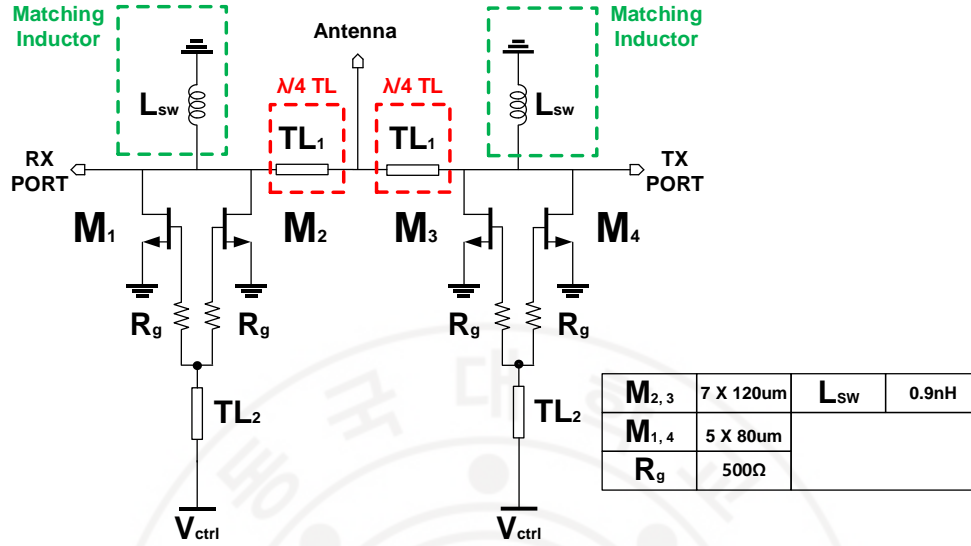


Figure 2.1–1 Schematic of X–band T/R switch in the single chip transceiver.

Figure 2.1–1 shows the schematic of the designed T/R switch. A Single–Pole–Double–Throw (SPDT) design was adopted to achieve both low insertion loss and high isolation. The structure is fully symmetric, and each signal path includes two parallel HEMTs to improve isolation. When the Tx path is active, devices M1 and M2 are turned on to create a short circuit, appearing as an open termination on the other side. A quarter–wave transformer ($\lambda/4$ T–line) is used to implement this function. To achieve impedance matching in the off–state, parallel inductors are included to resonate with the parasitic capacitance of the transistors. A 500Ω resistor is inserted into the gate control path to isolate the switch from the

common gate ground. All passive components were verified using Momentum EM simulation in ADS. The HEMT sizes were optimized to minimize insertion loss while maintaining sufficient isolation. Specifically, M2 was sized to $7 \times 120 \mu\text{m}$, and M1 and M4 were $5 \times 80 \mu\text{m}$. The transmission lines were designed to be wide enough to handle the output power from the PA reliably.

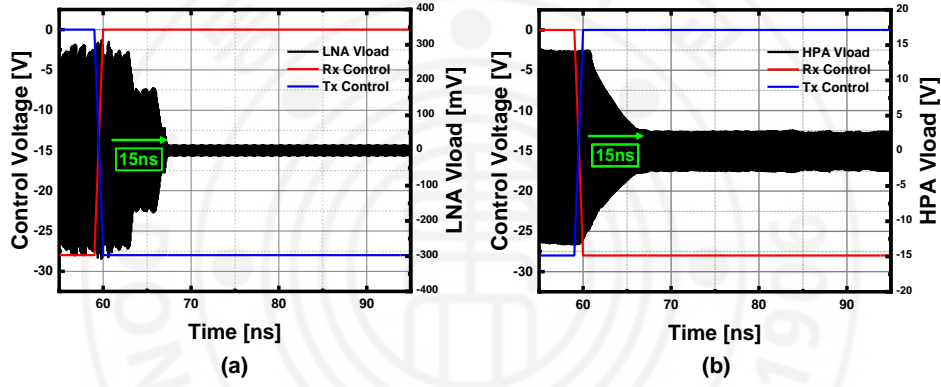


Figure 2.1-2 SPDT switching delay when the input power of SPDT switch antenna port is (a) -30dBm at 9GHz (b) 10dBm at 9GHz .

In DFRC systems, fast switching is crucial for accurate radar detection, Doppler estimation, high communication throughput, and effective self-interference cancellation. Figures 2.1-2 (a) and (b) show the transient response of the SPDT T/R switch when the input power is -30dBm and 10dBm , respectively. To achieve faster switching, $\lambda/4$ transmission lines were used in series instead of

series-connected HEMTs, enabling faster transitions than conventional SPDT designs. For high-speed validation, an RF signal was applied to the common port, and the time delay between the control signal transition and the signal drop at the load was measured. As shown in Figures 2.1–2 (a) and (b), the measured delay is 15 ns, confirming that the switch can rapidly transition between Rx and Tx modes, which is essential for DFRC system.

2.2 X-Band GaN Power Amplifier Design

The Power Amplifier (PA) is a key component in the DFRC single-chip transceiver, as it determines the overall system efficiency by amplifying the transmit signal to the required output power level. Given the high-power demands of DFRC systems for both sensing and communication functions, the PA must deliver sufficient output power while maintaining high efficiency.

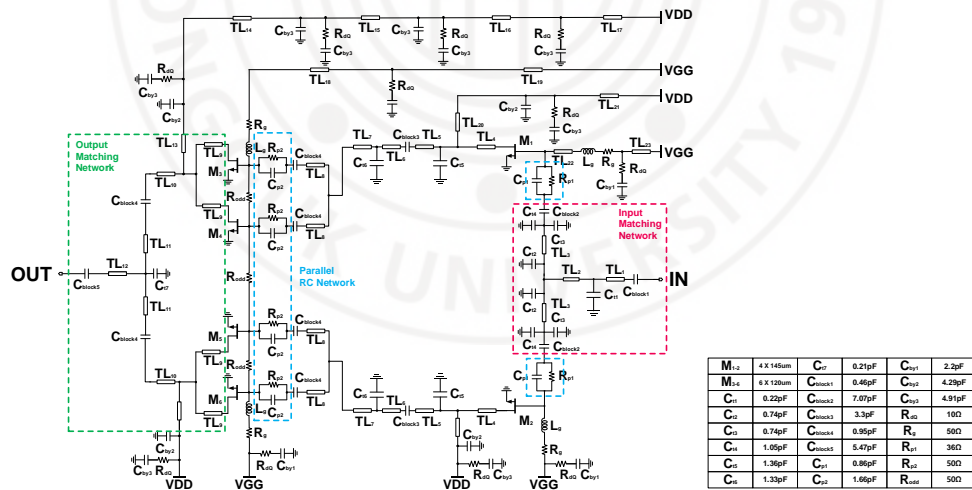


Figure 2.2–1 Schematic of designed X-band PA in the single chip transceiver.

Figure 2.2–1 presents the schematic of the designed PA, which adopts a four–way combining architecture with a two–stage configuration. At the input stage, two HEMTs with dimensions of $4 \times 145 \mu\text{m}$ serve as driver amplifiers, while the output stage employs four HEMTs sized at $6 \times 120 \mu\text{m}$ to realize a four–way power combining structure.

To ensure robust and stable operation, several circuit techniques were applied, as illustrated in Figure 2.2–2.

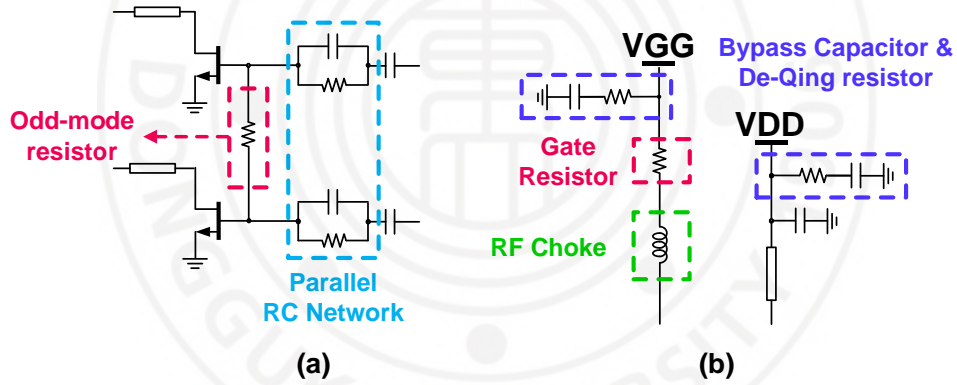


Figure 2.2–2 (a) Odd–mode resistor and parallel RC network at the gate and (b) Bypass capacitors and de–Qing resistor network for the bias routing lines of the integrated PA for the improved Stability.

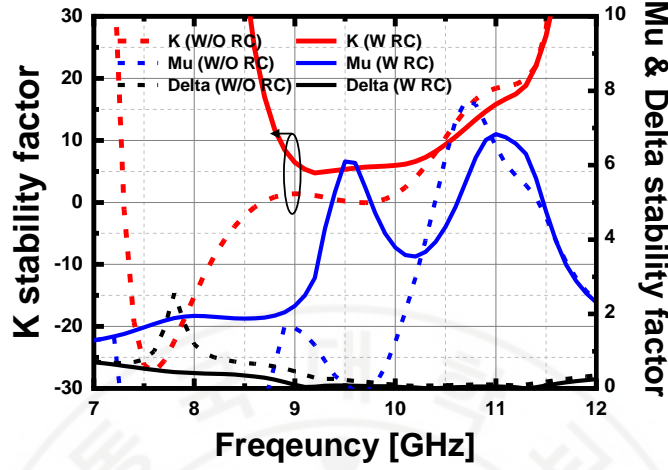


Figure 2.2-3 K, Mu and Delta stability factor with and without RC network

First, to enhance low-frequency stability, a parallel RC network was added at the gate of each HEMT. For the driver stage ($4 \times 145 \mu\text{m}$), a 36Ω resistor (R_{P1}) and 0.86 pF capacitor (C_{P1}) were used, while the output stage ($6 \times 120 \mu\text{m}$) included a 50Ω resistor (R_{P2}) and a 1.66 pF capacitor (C_{P2}). Stability analysis results, shown in Figure 2.2-3 using K-factor and μ -factor plots, indicate that the absence of the RC network results in significant degradation in low-frequency stability.

Second, to prevent odd-mode oscillations arising from power imbalance or mismatches across the parallel output branches, a transient simulation was performed with small perturbations on the supply and bias nodes. Because such odd-mode oscillations are not

detectable through standard two port stability metrics (K or μ), practical verification is necessary. To suppress these oscillations, a $50\ \Omega$ shunt resistor (R_o) was inserted between each of the output-stage transistors [30].

Third, to mitigate VDD line ringing and associated bias instability, bypass capacitors in conjunction with damping resistors were employed. These components provide instantaneous current during switching events, thereby reducing impedance in the bias path and suppressing coupled noise. Specifically, a $10\ \Omega$ de-Qing resistor (R_{dQ}) was connected in series with each bypass capacitor to suppress oscillations originating from the bias line.

Since the T/R switch, PA, and LNA are monolithically integrated, the gate and drain bias lines of some HEMTs are relatively long. This increases the risk of parasitic inductance-induced ringing. To address this, multiple bypass capacitors were distributed along the bias lines. The series de-Qing resistor (R_{dQ}) in the gate bias line lowers the Q-factor of the equivalent RLC network formed by the bypass capacitor (C_{byp}) and parasitic inductance (L_{para}). To prevent unwanted low-frequency oscillation, this RLC network must remain overdamped, which is ensured by carefully selecting an appropriate value for R_{dQ} . Which is given by

$$R_{dQ} = 2 \sqrt{\frac{L_{para}}{C_{byp}}} \quad (2.2-1)$$

From equation (2.2-1), it is evident that minimizing the parasitic inductance L_{para} is essential to keeping the de-Qing resistor R_{dQ} sufficiently low, thereby preventing degradation in filtering performance. The parasitic inductance L_{para} was estimated through Momentum EM simulations, while the bypass capacitor C_{byp} was selected to be large enough to effectively suppress interference propagating through the bias line.

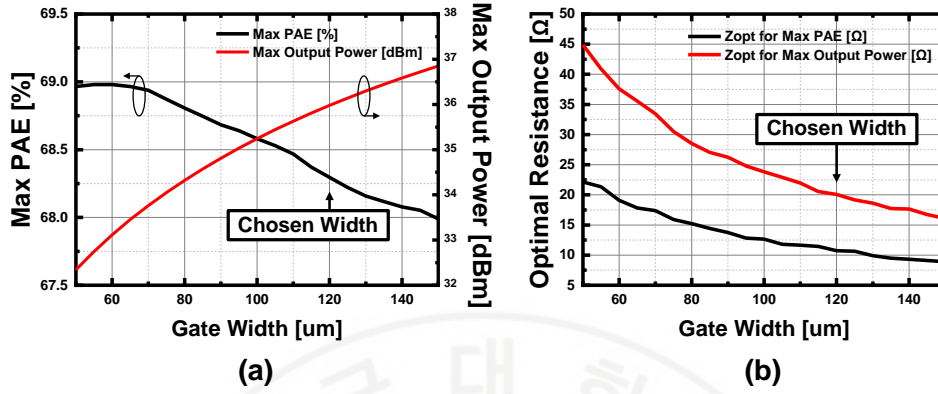


Figure 2.2-4 (a) Maximum output power and PAE of the GaN HEMT (b) Optimal resistance for maximum output power and PAE as a function of gate width.

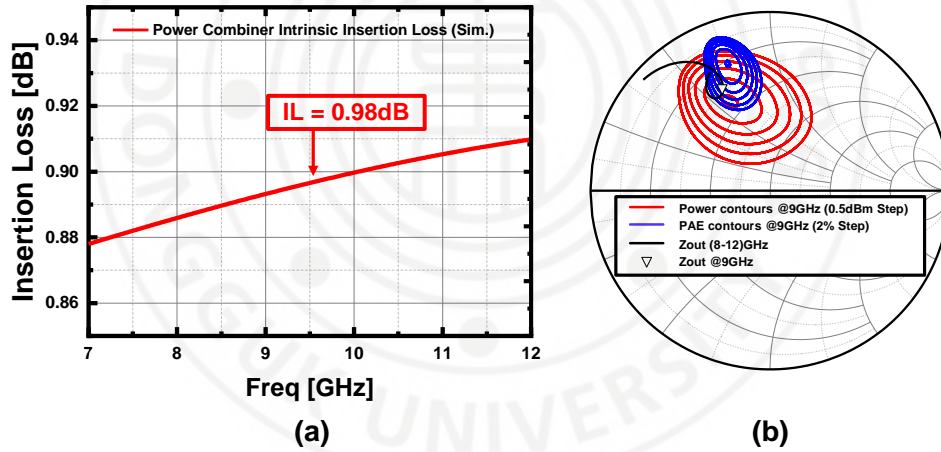


Figure 2.2-5 (a) Intrinsic Insertion loss of the power combiner (b) Output power and PAE contour of 6x120 μm HEMT device.

To maximize power-added efficiency (PAE) and output power, a parametric sweep of the HEMT gate width was performed, as shown in Fig. 2.2-4(a). To meet the target output power of 40 dBm using a 4-way power combining network and SPDT switch, a single device capable of delivering at least 36 dBm was required. A $6 \times 120 \mu\text{m}$ GaN HEMT was selected, as it provides the desired 36 dBm output power while also optimizing PAE. This choice also ensures a practical impedance transformation ratio, considering both insertion loss and bandwidth constraints.

Figure 2.2-4(b) illustrates the variation of the real part of the optimal impedance for maximum PAE and maximum output power as a function of device size. As the transistor gate width increases, the DC current increases linearly, while the optimal load impedance decreases inversely. To achieve saturated output power beyond 40 dBm, a 4-way power combining structure was adopted. The measured insertion loss of the designed combiner is 0.98 dB at 9 GHz, as presented in Fig. 2.2-5(a).

Subsequently, load-pull simulations were performed for the $6 \times 120 \mu\text{m}$ HEMT to determine the optimal load impedances for output power and PAE, as shown in Fig. 2.2-5(b). The device exhibited a

peak output power of 36.0 dBm at the optimal impedance $Z_{\text{opt,Pout}} = 20.7 + j28.0 \Omega$, and a maximum PAE of 68.3% at $Z_{\text{opt,PAE}} = 11.0 + j34.8 \Omega$. For the output matching network, the chosen load impedance was $Z_{\text{out}} = 16.8 + j27.6 \Omega$, positioned closer to $Z_{\text{opt,Pout}}$ to prioritize achieving the required output power level for the DFRC application.



2.3 X-Band GaN Low Noise Amplifier (LNA) Design

The Low Noise Amplifier (LNA), located at the front end of the receiver chain, amplifies the incoming RF signal with a minimized noise figure. Unlike GaAs-based LNAs, which require external limiters to protect them from high input power, GaN LNAs benefit from a high breakdown voltage, eliminating the need for such bulky protection components. This allows the implementation of the receiver chain without external limiters, while still maintaining performance comparable to GaAs LNAs with protection. However, since GaN HEMTs typically exhibit inferior RF performance compared to their GaAs counterparts, careful design is required to ensure low NF and high gain.

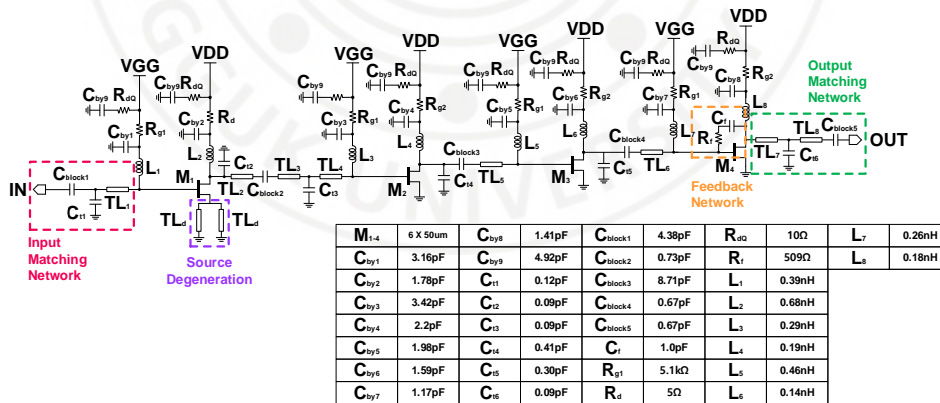


Figure 2.3–1 Schematic of designed X-band LNA in the single chip transceiver.

Figure 2.3–1 shows the schematic of the designed LNA. Because the overall noise performance of a cascaded system is predominantly determined by the first stage [31], careful input matching for optimal noise performance is essential. To achieve both impedance and noise matching, inductive source degeneration was applied to the first stage. A $6 \times 50 \mu\text{m}$ HEMT configured as a common – source amplifier with inductive degeneration was used. The values for the device size and source inductance were determined using the small signal noise model provided in the PDK.

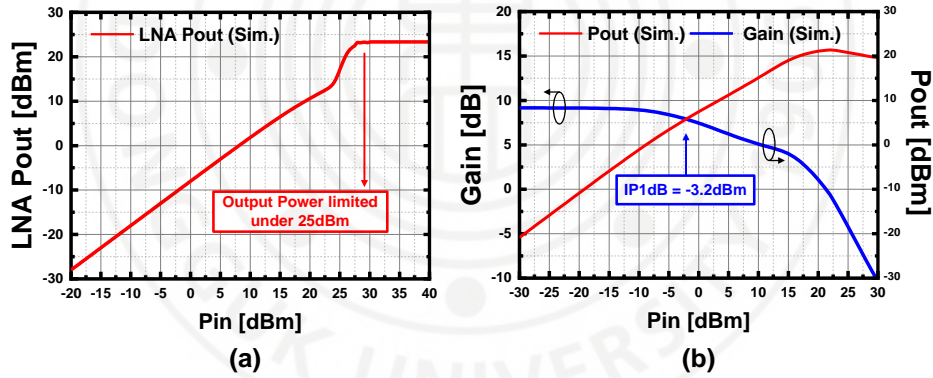


Figure 2.3–2 (a) Output power of the LNA at 9GHz depending on the input power from Tx port. (b) IP1dB of the single GaN CPW HEMT device at 9GHz

To achieve wideband performance and enhanced stability, an RC–RC feedback network was applied in the fourth stage. A four – stage LNA

structure was adopted to achieve high gain, which is important for reducing overall system cost and minimizing the need for an additional driver stage. A high-gain LNA also helps reduce the system footprint, as additional amplification is unnecessary. To avoid performance degradation in subsequent stages, the LNA output power was intentionally limited. The final stage device was sized at $6 \times 50 \mu\text{m}$ to ensure that the saturated output power (P_{sat}) remains below 25 dBm. As shown in Figure 2.3–2(a), even when the PA delivers high output power, the LNA output is limited to under 25 dBm, thereby protecting downstream components.

The input 1-dB compression point ($IP_{1\text{dB}}$) of a single-stage CS amplifier using a $6 \times 50 \mu\text{m}$ GaN HEMT is -3.2 dBm, as illustrated in Figure 2.3–2(b). This relatively soft compression is partly attributed to the nonlinear behavior of GaN HEMTs, such as the charge trapping effect [17].

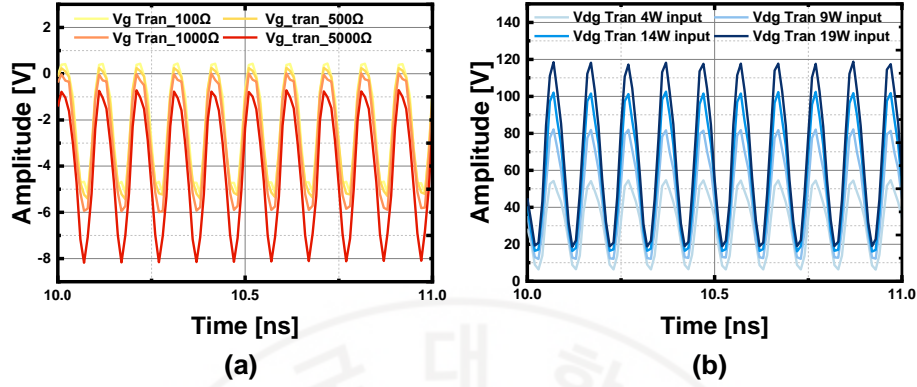


Figure 2.3–3 Transient simulation of (a) the gate voltage when $P_{in} = 20\text{dBm}$ of the first stage HEMT device in the LNA for various gate resistor value (R_g) (b) the drain–gate voltage for various input power level.

Figure 2.3–3(a) shows the transient simulation of the gate voltage of the first–stage HEMT in the LNA, integrated with a T/R switch, under a 20 dBm input power condition for various gate resistor (R_g) values. When R_g is too small, the gate voltage can exceed 0 V, causing large drain currents that destabilize the amplifier. Prior studies [32] have shown that using a sufficiently large gate resistor mitigates this issue by reducing gate DC current through feedback from the voltage drop across the resistor. In this design, R_g was set to $5\text{ k}\Omega$. Figure 2.3–3(b) presents the corresponding drain–gate voltage (V_{dg}) of the first–stage device at various input powers. The results show that V_{dg}

remains below the breakdown voltage ($V_{BD} = 120\text{ V}$) even under continuous-wave (CW) input signals of up to 19 W, confirming reliable operation under high-power conditions.

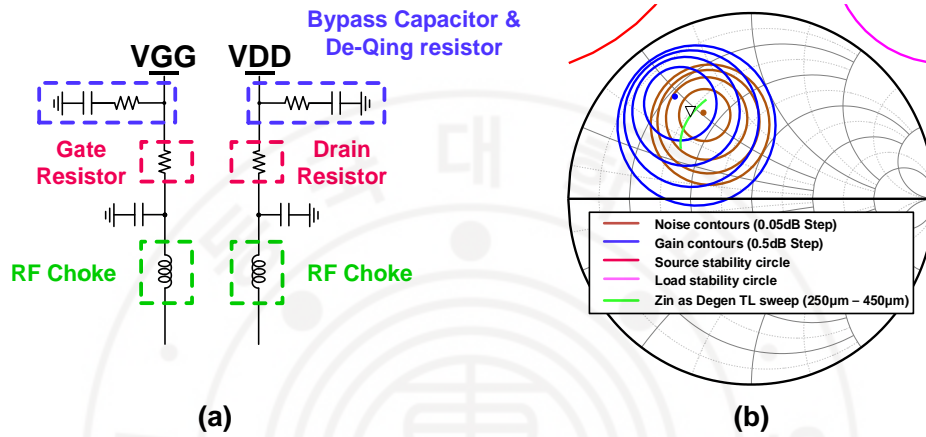


Figure 2.3-4 (a) Bypass capacitor and de-Qing resistor network (b) gain and noise contours, along with the source and load stability circles .

Figure 2.3-4(a) illustrates the bypass capacitor and de-Qing resistor network used for the LNA. A $5\ \Omega$ series resistor (R_d) was added to the drain bias line to enhance stability, even though it may slightly reduce the overall gain. Bypass capacitors (C_{by}) and de-Qing resistors (R_{dQ}) were included to suppress noise and bias line ringing, with component values selected based on earlier design principles. To further improve robustness without relying on external limiters—

as would be necessary for GaAs LNAs—a $5\text{ k}\Omega$ gate resistor (R_g) was inserted to limit gate leakage current by utilizing the self-biasing effect induced by high gate swing [32].

Figure 2.3–4(b) displays the gain and noise contours, along with the source and load stability circles for the $6 \times 50\text{ }\mu\text{m}$ HEMT, plotted on a Smith chart. A parametric sweep of the degeneration transmission line length (TLD) from $250\text{ }\mu\text{m}$ to $450\text{ }\mu\text{m}$ at 9 GHz was conducted to optimize the input impedance. The selected input impedance closely matches the optimal noise impedance. Noise contours were plotted with 0.05 dB steps and gain contours with 0.5 dB steps. The optimal noise impedance was found to be $19.8 + j25.6\Omega$, while the optimal gain impedance was $11.3 + j24.0\Omega$. Both source and load stability circles lie outside the Smith chart, indicating unconditional stability of the designed LNA.

Chapter III. Code Optimization Technique

3.1 Simulation Annealing

Simulated Annealing (SA) is a stochastic optimization method designed to efficiently explore global or near-global solutions of complex multivariate nonlinear functions. It was first introduced by Kirkpatrick et al [33] and is inspired by the physical annealing process, where a material is heated to a high temperature and then gradually cooled so that it crystallizes into a low-energy structure. Analogously, SA begins at a high temperature and progressively lowers this control parameter T , thereby transitioning from broad to more localized searches in the solution space.

Figure 3.1–1 illustrates the flowchart of the SA process. One of the key features of SA is that it accepts not only solutions that decrease the objective (or cost) function, but also, with a certain probability, those that increase it. This acceptance rule is governed by the Metropolis criterion, where a cost-increasing move with an energy difference ΔE is accepted with a probability $\exp(-\Delta E/T)$. At higher temperatures, the algorithm frequently accepts worse solutions, enabling an extensive exploration of the solution landscape. As the temperature is reduced, the acceptance of worse solutions becomes

less likely, thus refining the search in promising regions.

SA's performance is highly dependent on the chosen "cooling schedule." A common approach is geometric cooling, defined by $T_{k+1} = \alpha T_k$ with $0 < \alpha < 1$. As α approaches 1, the temperature decreases more slowly, allowing for more comprehensive exploration at the cost of increased computation time. Alternative schedules, such as logarithmic or linear cooling, may also be employed depending on the problem's characteristics, scale, and computational constraints. Tuning the cooling schedule and the number of iterations is crucial for balancing solution quality with execution time.

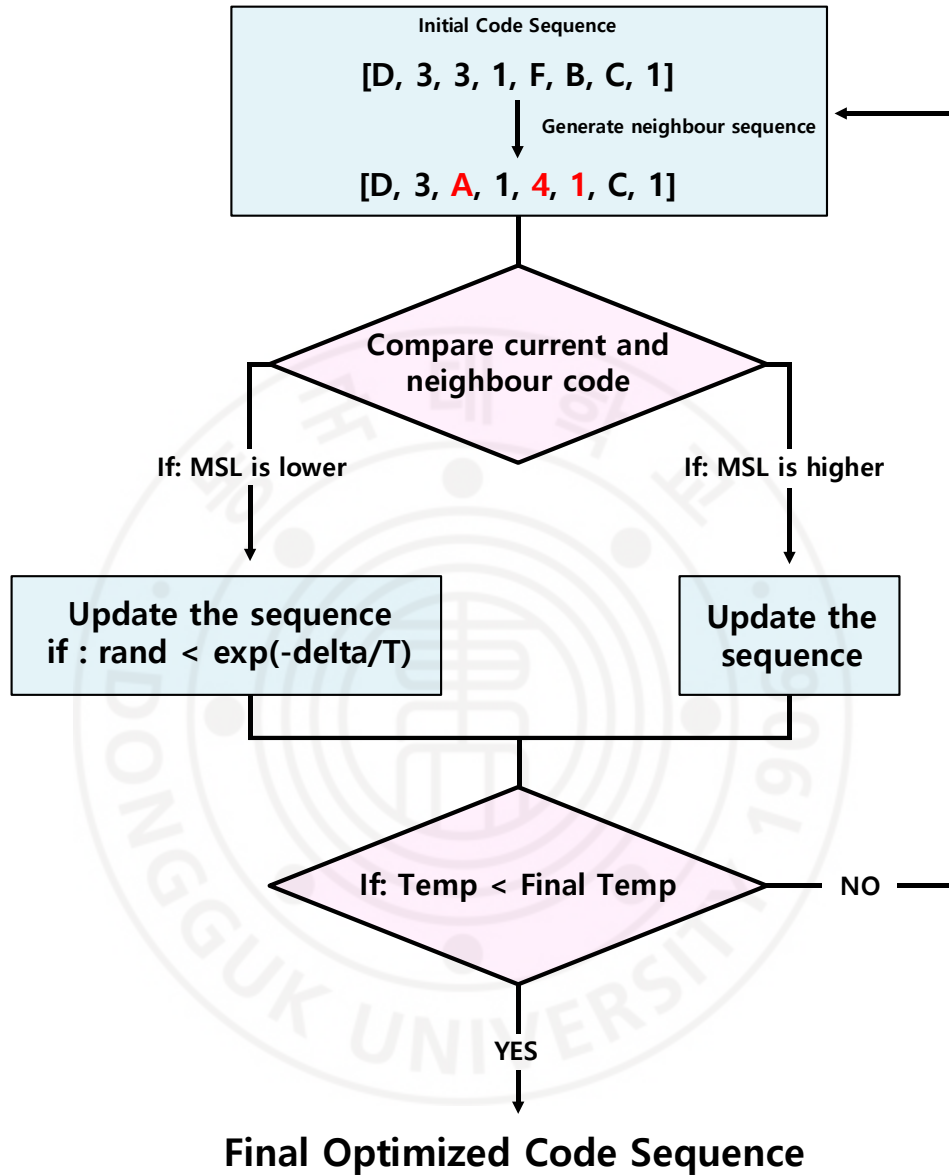


Figure 3.1–1 Flowchart of the Simulated Annealing Process.

In addition to SA, various other effective optimization algorithms have been proposed. For instance, Genetic Algorithm (GA) has been widely adopted in various optimization problems. GA is less likely to be trapped in local minima and has been used in many studies aimed at reducing the PSLR [34]. Nevertheless, GA suffers from high computational complexity and slow convergence speed.

Although SA is considered a relatively traditional method, several studies have demonstrated its effectiveness in SLL optimization by leveraging its rapid convergence and strong global search capability [35]. Thus, SA is evaluated as a promising algorithm that simultaneously satisfies the requirements for fast execution and global optimization performance.

In this study, we quantitatively evaluated the PSLR improvement and computation time for each optimization algorithm. To ensure statistical reliability, we performed 10,000 independent runs for each algorithm.

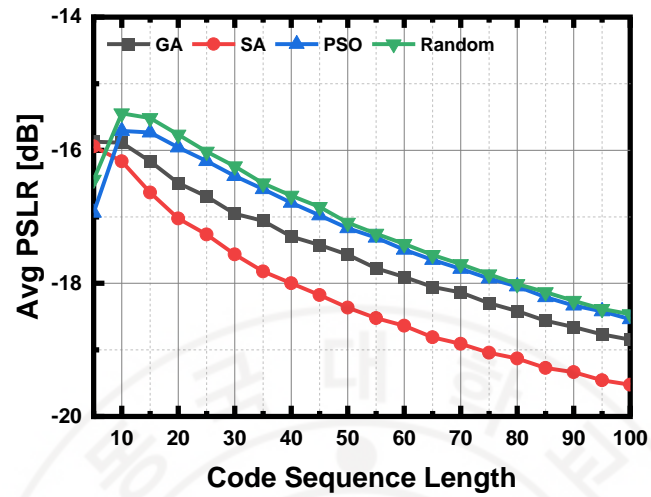


Figure 3.1–2 Average PSLR According to Code Sequence Length for Each Optimization Algorithm

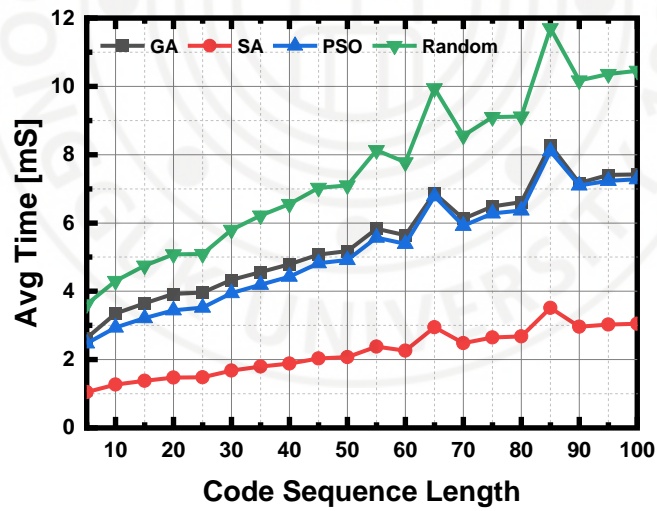


Figure 3.1–3 Average Execution Time According to Code Sequence Length for Each Optimization Algorithm

<Table 3.1–1> Comparison table of algorithms for code sequence optimization.

Algorithm	PSLR Mean [dB]	PSLR SD [dB]	Time Mean [mSec]	Time SD [mSec]
Simulation Annealing	–18.18	0.767	2.20	1.249
Genetic Algorithm	–17.54	0.610	5.46	3.237
PSO	–17.21	0.584	5.19	2.522
Random	–17.08	0.452	7.54	3.922

Figure 3.1–1 shows the average PSLR across different code sequence lengths for each algorithm after 10,000 optimization runs with 16QAM. As can be seen in the figure, starting from a sequence length of 10, the SA algorithm demonstrates better PSLR performance compared to the others.

Figure 3.1–2 shows the average execution time for each algorithm under the same conditions. As illustrated, SA consistently achieves the fastest execution time across all code sequence lengths.

In simulated annealing, 5,000 iterations are performed with the initial temperature set to 10 so that the algorithm can explore a broad range of solutions at the start. The temperature is gradually lowered to 10^{-6} through the cooling process, and with a cooling rate of 0.95,

it avoids dropping too quickly. As a result, it begins with a wide search scope and progressively narrows in on local areas to converge on a more refined solution. In the genetic algorithm, the number of generations is set to 100 with a population size of 50, striking a balance between search diversity and computational cost. The crossover probability is raised to 0.8 to broaden the combination of genetic information among different individuals, increasing the chance of finding better solutions, while the mutation probability is set at 0.2 to ensure that new solutions are continuously explored. Particle swarm optimization runs for 100 iterations with 30 particles, allowing the swarm to cooperate in refining the solution. An inertia weight of 0.8 is used so that each particle partially retains its previous velocity, preventing the search scope from shrinking too rapidly. With both the cognitive and social coefficients set to 1.5, individual and collective experiences are balanced. Random search, on the other hand, is set to 1,000 iterations, simply sampling the solution space at random to see if it can quickly find solutions that meet certain criteria, and providing a straightforward baseline against which to compare other metaheuristic methods.

The experimental results show that SA outperforms the other

algorithms in both PSLR reduction and computation time, and based on this, SA was selected as the final optimization algorithm in this study.



3.2 QPSK code optimization

We conducted code sequence optimization for QPSK using the SA algorithm, targeting PSLR minimization. Two code lengths 10 and 50 were evaluated in MATLAB.

The methodology followed a structured process:

First, we defined the objective function as follows. The normalized QPSK constellation S is typically represented as:

$$S = \left\{ \frac{1}{\sqrt{2}}(1+j), \frac{1}{\sqrt{2}}(1-j), -\frac{1}{\sqrt{2}}(1+j), -\frac{1}{\sqrt{2}}(1-j) \right\} \quad (3.2-1)$$

Each symbol is normalized to ensure that the average energy is equal to 1. For a given length N required by the system, the QPSK sequence s is:

$$s = (s_0, s_1, \dots, s_{N-1}) \quad (3.2-2)$$

Given a QPSK sequence of length N , its autocorrelation function $R(\tau)$ is defined as follows:

$$R(\tau) = \sum_{n=0}^{N-1-\tau} s_n s_{n+\tau}^* \quad \tau = 0, 1, \dots, N-1 \quad (3.2-3)$$

Where τ represents delay or shift index. The autocorrelation value at $\tau=0$ reflects the energy of the code and is considered the main

lobe.

The magnitude of the autocorrelation function, $|R(\tau)|$, for $\tau \neq 0$, is referred to as the side lobe. Various metrics are commonly used to quantitatively evaluate side lobes such as PSLR which is defined as:

$$PSLR = \frac{\max_{\tau=1, \dots, N-1} |R(\tau)|^2}{|R(0)|^2} \quad (3.2-4)$$

Then, we set PSLR as the objective function, performed optimization, and evaluated PSLR.

Secondly, we set the number of iterations to 5,000, the initial temperature to 10, the final temperature to $1/10^{-6}$, and the cooling rate to 0.95 and we initialize the code sequence by randomly generating a series of these complex symbols. This random sequence serves as the starting point for the optimization algorithm. The length of the code sequence is predetermined based on system requirements or desired performance characteristics.

Thirdly, the optimization process employs simulated annealing to minimize the objective function, thereby reducing the PSLR. Initially, a randomly generated code sequence is used as the starting point. During each iteration a symbol is randomly selected.

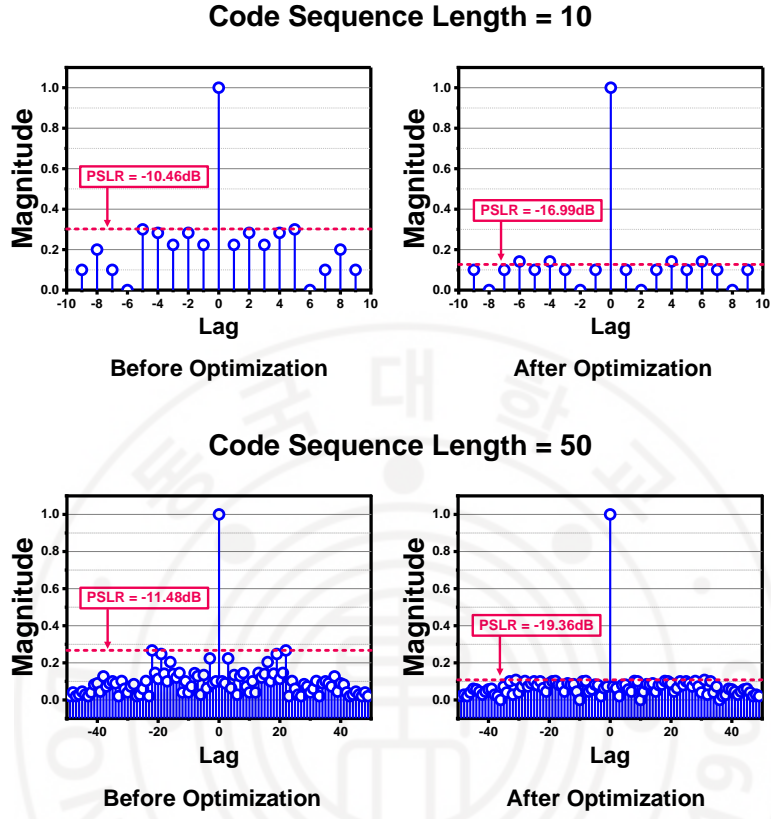


Figure 3.2-1 Autocorrelation result of before and after QPSK code optimization for code sequence length 10 and 50 ($L=10$ and 50).

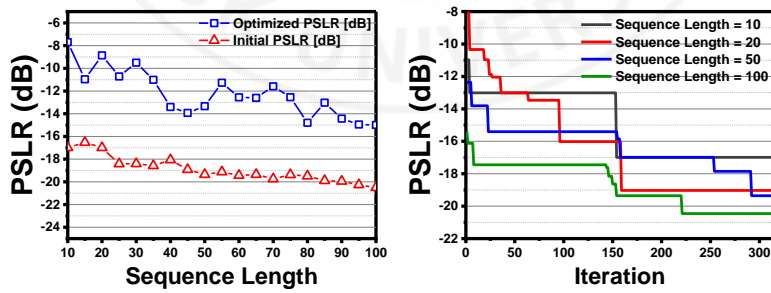


Figure 3.2-2 (a) PSLR according to code sequence length (b) PSLR according to optimization iteration

<Table 3.2–1> Comparison table of PSLR improvement in QPSK signal.

Ref	PSLR [dB]	Code Length
This work	– 16.99	10
	– 19.36	50
[36]	– 10.2	50
	– 7	10
[37]	– 16.51	12

Fig. 3.2–1 depicts the result of auto–correlation before optimization process and after optimization process when the code lengths are 10, 50 in QPSK. As can be seen in Fig. 3.2–1, when the code length is 10 ($L=10$), the PSLR before optimization was -10.46dB and after it was -16.99dB . When the code length is 50 ($L=50$), the PSLR before optimization was -10.46dB and after it was -16.99dB . As can be seen in this result, the optimization process through simulation annealing successfully lowered the PSLR of the code sequence. Figure 3.2–2(a) depicts the comparison of PSLR between before the optimization process and after the optimization process. We can see that the longer code sequence the better PSLR improvement. Figure 3.2–2(b) depicts the PSLR improvement against the iteration number. We can see that the trade–off between number of iterations which is

directly related to the computing power and the time and the PSLR improvement. Therefore, Selecting the optimal code length is crucial for rapid calculation time and the PSLR improvement performance.

Table 3.2-1 benchmarks three different PSLR-minimization strategies applied to QPSK codes. Our work employs simulated annealing (SA) with a finely tuned schedule (5000 iterations, $T_0 = 10$, $T_f = 10^{-6}$, cooling = 0.95) and achieves -16.99 dB for $L = 10$ and -19.36 dB for $L = 50$. In contrast, Singh & Rao [36] also relied on SA for poly-phase code design in netted-radar systems, but reported higher sidelobes (-7 dB at $L = 10$, -10.2 dB at $L = 50$). Tang et al. [37] adopted a joint sequence-mapping + recursive-least-squares (RLS) filter architecture; while effective for communication/radar co-design, it yielded -16.51 dB with only a 12-chip sequence and did not scale to longer codes.

The markedly deeper sidelobe suppression obtained here stems from the way SA was integrated. By exploring 10 000 random restarts and permitting occasional uphill moves, the algorithm consistently escaped local minima, converging on longer sequences whose phase combinations are rarely reached by deterministic mapping or single-pass RLS filtering. This exhaustive global search, backed by statistically reliable Monte-Carlo testing, tightened the

worst-case PSLR by roughly 9 dB at $L = 10$ and 9.1 dB at $L = 50$ relative to the best prior studies, validating SA' s superior balance of global exploration and fast convergence for radar-centric code optimization.



3.3 16QAM Code Optimization

To identify the optimal code sequence for 16QAM which minimize the PSLR, we undertook the same methodological steps as we performed in QPSK code sequence optimization.

Firstly, we defined objective function as below. The normalized 16QAM constellation S is generally defined as follows:

$$S = \left\{ \frac{a + jb}{\sqrt{10}} \middle| a, b \in \{-3, -1, +1, +3\} \right\} \quad (3.3-1)$$

The remaining steps are identical to those performed in the QPSK. Firstly, the autocorrelation is defined using equation (3.2-3), and the PSLR is defined using equation (3.2-4), which is then used to formulate the objective.

Secondly, we set the number of iterations to 5,000, the initial temperature to 10, the final temperature to $1/10^6$, and the cooling rate to 0.95. And we initialize the code sequence by randomly generating a series of these complex symbols.

Thirdly, the optimization process employs simulated annealing to minimize the autocorrelation of the code sequence like we did for the QPSK. But for the 16QAM, we limited the selected symbol's phase

and amplitude is altered to one of the 16 states which ensures the optimized sequence with in the phase and amplitude of the 16QAM.

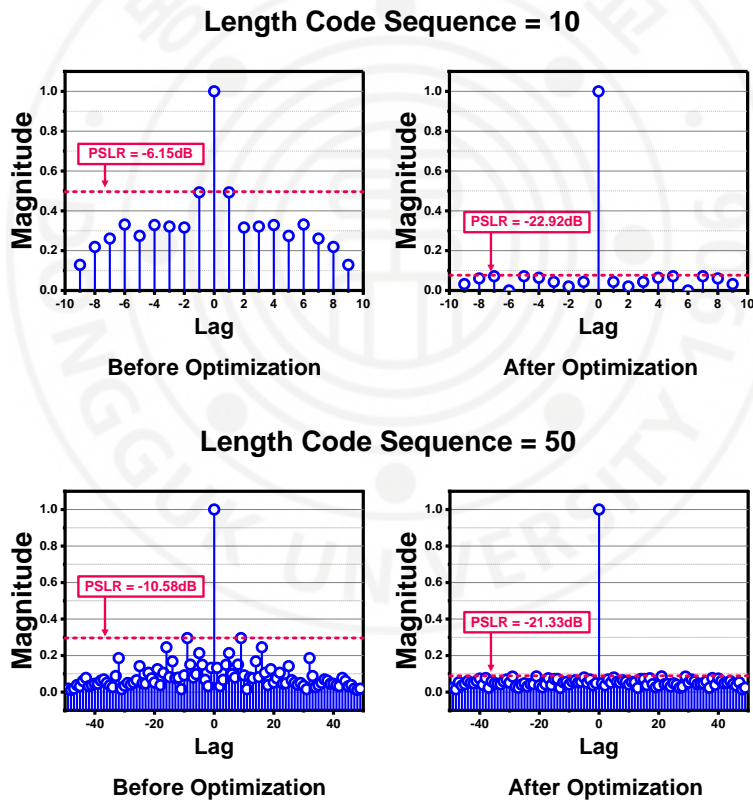


Figure 3.3–1 Autocorrelation result of before and after 16QAM code optimization for code sequence length 10 and 50 ($L=10$ and 50).

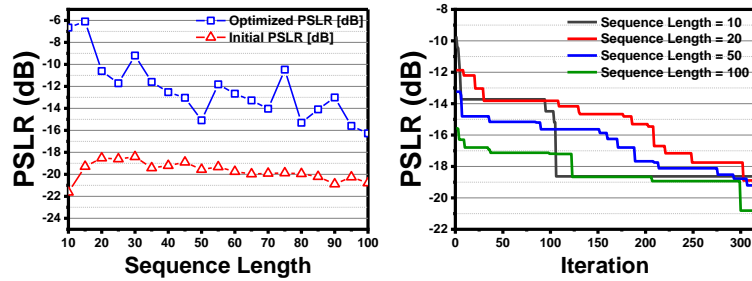


Figure 3.3–2 (a) PSLR according to code sequence length (b) 16QAM according to optimization iteration.

<Table 3.3–1> Comparison table of PSLR improvement in 16QAM signal.

Ref	PSLR [dB]	Code Length
This work	– 18.93	10
	– 22.92	50
[38]	– 23.28	512

Fig. 3.3–1 depicts the result of auto–correlation before optimization process and after optimization process when the code lengths are 10, 50 in 16QAM. As can be seen in Fig. 3.3–1, when the code length is 10 ($L=10$), the PSLR before optimization was -6.16dB and after it was -22.92dB . When the code length is 50 ($L=50$), the PSLR before optimization was -10.58dB and after it was -21.33dB . As shown in the results, 16QAM achieves lower PSLR compared to QPSK, which

may be attributed to its improved pulse compression characteristics. As can be seen in this result, the optimization process through simulation annealing successfully lowered the SLL of the code sequence in 16QAM.

Research on sidelobe suppression for 16-QAM has largely revolved around tone-reservation (TR) techniques. Liu et al.'s "TR-GS" first trims PAPR via a least-squares approximation (LSA) and then adds a Gerchberg-Saxton (GS) phase-retrieval loop, bringing the peak-to-sidelobe level ratio (PSLR) down to about -23 dB. LNCA and plain TR-LSA use, respectively, an MM-based modulus-equalisation update and a PAPR-only strategy; yet all three need long 256-512-symbol codes and still hover between -23 and -16 dB PSLR.

Our work applies simulated annealing (SA) alone and reaches -22.9 dB ($L = 10$) and -21.3 dB ($L = 50$) with codes just one-tenth that length. By jointly perturbing amplitude and phase and probabilistically escaping local minima, SA eases hardware implementation. This shorter length is inherently more hardware-friendly, confirming that the proposed SA method is the most efficient and practical option for minimizing PSLR in real DFRC systems.

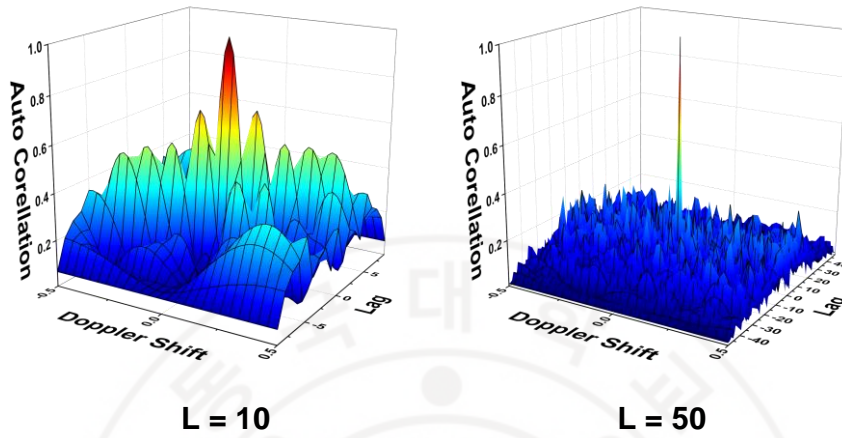


Figure 3.3–3 The ambiguity function of 16QAM of code length (L) (a) 10, (b) 50.

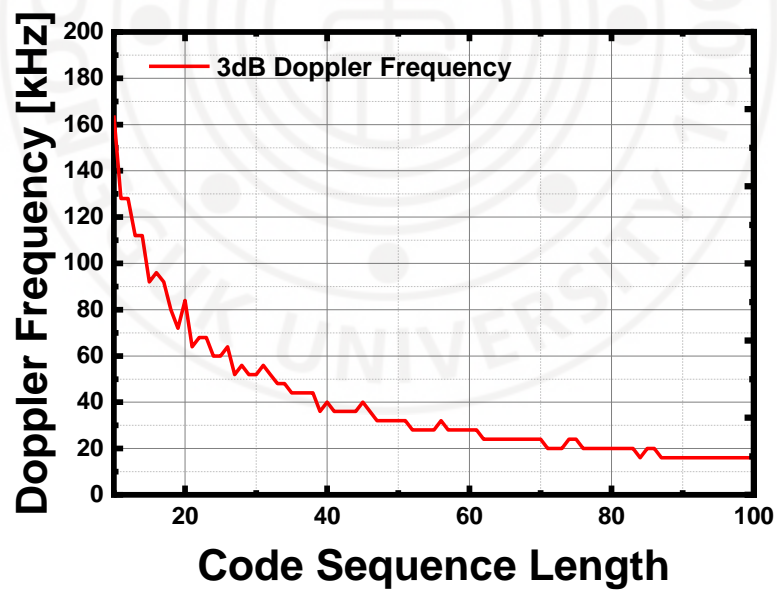


Figure 3.3–4 (a) The Doppler frequency according to code length(L).

Figure 3.3–3 illustrates the ambiguity function results for different code sequence lengths. Doppler tolerance is evaluated by examining how well an optimized code sequence maintains stable correlation under varying Doppler shifts. By sweeping the Doppler frequency f_d and applying a phase shift to the code sequence $s(n)$, the Doppler-shifted sequence $s_d(n)$ is generated. Cross-correlation with $s(n)$ is then used to calculate sidelobe levels and PSLR changes. Additionally, the two-dimensional ambiguity function is visualized by varying both time delay (τ) and Doppler frequency (f_d), enabling a comprehensive assessment of range and velocity resolution under target motion.

Figure 3.3–4 also shows that as the code sequence length increases, leading to a lower PSLR, the 3dB Doppler frequency decreases. This trade-off highlights the need for careful selection of code length based on system requirements.

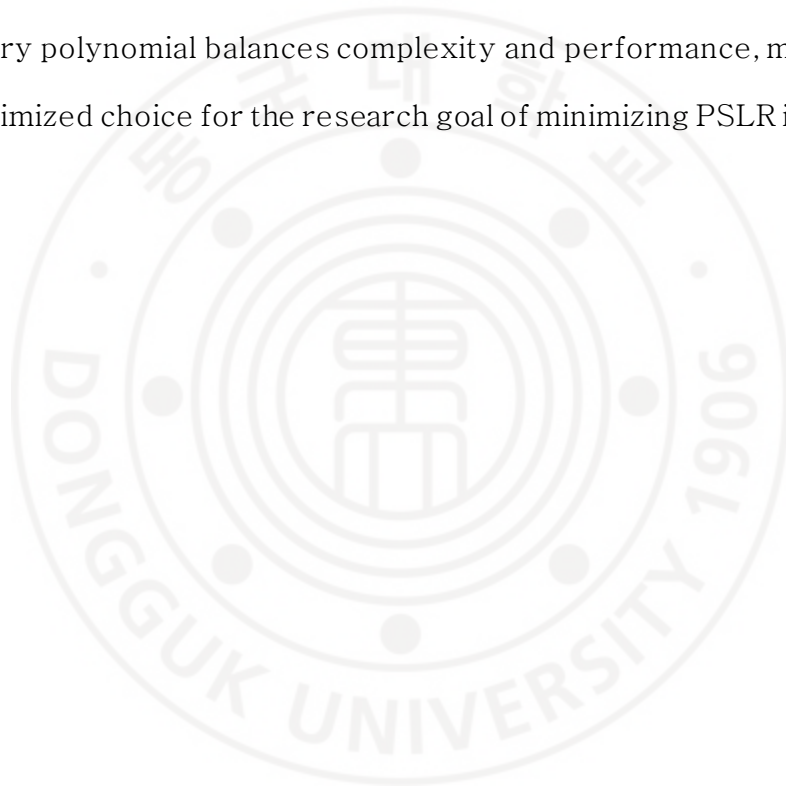
Chapter IV. Digital Predistortion

4.1 Memory Polynomial DPD

It has been widely recognized that the Digital predistortion (DPD) is a strong method in linearizing non-linear characteristics of power amplifier (PA). A memory polynomial-based DPD is designed to model and compensate for slow time-domain distortion components, partially mitigating gain and phase variations caused by memory effects [39]. Additionally, optimizing the pulse compression code to prevent excessive spectral asymmetry in output power distribution can help alleviate thermal accumulation and trapping effects in high-power regions. As a result, the accumulation of nonlinear distortions due to memory effects is reduced, suppressing unintended sidelobe elevation and ultimately lowering the SLL of radar signals in the time domain.

The memory polynomial structure effectively models the nonlinearity and memory effects of the PA while maintaining low computational complexity, making it suitable for radar systems that require real-time processing [40]. In contrast, Volterra series-based predistortion offers high accuracy but is difficult to implement due to its high computational complexity, and neural network-based

predistortion can model complex nonlinearities but involves significant complexity in training data collection and implementation [41–42]. Memoryless polynomial predistortion is simple to implement but ignores memory effects, resulting in decreased accuracy for high-speed or wideband signals [39]. Therefore, the memory polynomial balances complexity and performance, making it an optimized choice for the research goal of minimizing PSLR in QPSK.



4.2 MP-DPD PSLR Simulation

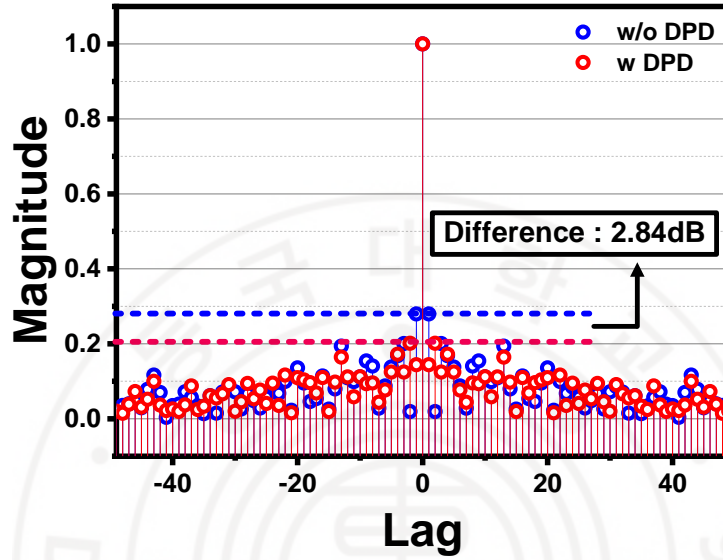


Figure 4.2–1 The autocorrelation result of 16QAM with DPD and without DPD.

To verify whether DPD can effectively reduce sidelobe levels, we conducted simulations using MATLAB.

The optimized code was first obtained and then input into a Memory Polynomial model representing a nonlinear PA. We observed the changes in the sidelobe levels of the autocorrelation function after applying the optimized code to the nonlinear PA model. Subsequently, the same code was input into the same PA model, but this time DPD was applied to compensate for the nonlinearity of the GaN PA.

Figure 4.2–1 illustrates the results of this simulation. In this simulation, we applied the previously used 16QAM modulation. As shown in Figure 4.2–1, when the optimized code was applied to the PA without DPD, the SLL was approximately -11.06 dB. After applying DPD, the simulation showed an SLL of approximately -13.90 dB, indicating an improvement of about 2.84 dB. This result demonstrates that DPD can effectively reduce the SLL caused by the nonlinearity of GaN PAs, confirming the efficacy of DPD as a solution to enhance sidelobe performance.

Chapter V. Measurement

5.1 Transceiver Measurement

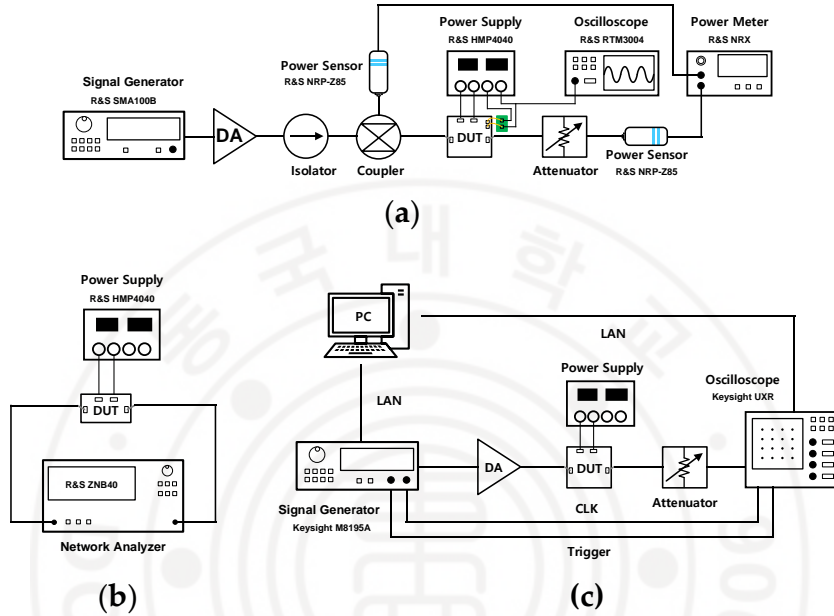


Figure 5.1-1 Block diagrams of measurement setup for (a) large signal, (b) small signal, (c) digital pre-distortion.

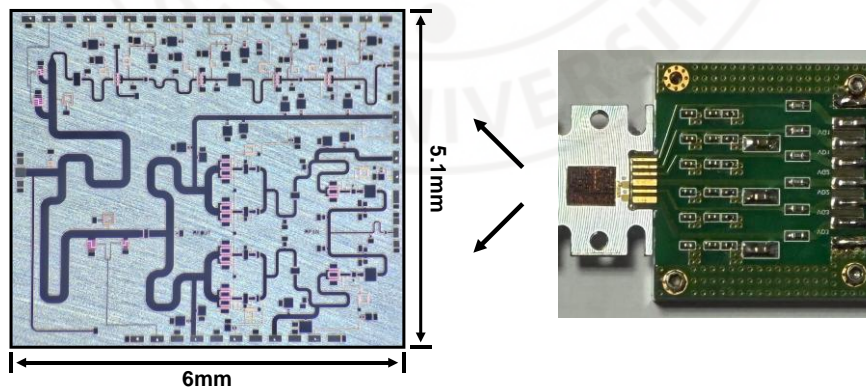


Figure 5.1-2 Photo of the implemented X-band transceiver;

Figure 5.1–1 shows the photo of the small and large signal and DPD and SLL measurement setup.

In the large–signal measurement, the GaN PA was characterized using the SMA100B signal generator, RTM3004 oscilloscope, NRP–Z85 power sensor, NRX power meter, and HMP4040 power supply from Rohde & Schwarz, as illustrated in Figure 5.1–1 (a).

In the small–signal S–parameters measurement, the designed PA was tested using the ZNB40 VNA and the HMP4040 power supply, as shown in Figure 5.1–1 (b).

Figure 5.1–1 (c) illustrates the SLL measurement setup diagram. During the PSLR measurement, optimized code sequences for QPSK or 16QAM were created using MATLAB and modulated signals were generated using Keysight N7608C software on a PC. For DPD implementation, Keysight N7614C software was utilized to perform DPD. The generated signals were then fed into the M8195A arbitrary waveform generator (AWG). To perform DPD, the clock (CLK) and trigger connections were established between the AWG and the UXR0104A oscilloscope. The output signal from the AWG was applied to the PA, and the VSA89600 software was used to observe the autocorrelation in the time domain through the oscilloscope.

Figure 5.1–2 shows the photograph of the GaN PA fabricated using a 250 nm process. The size of the transceiver is 30.6 mm^2 ($6 \times 5.1 \text{ mm}$).



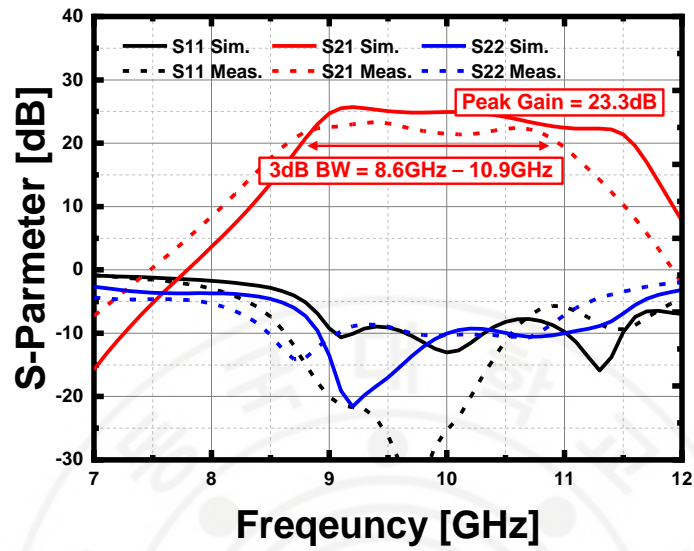


Figure 5.1-3 Small signal measurement result of the Tx side.

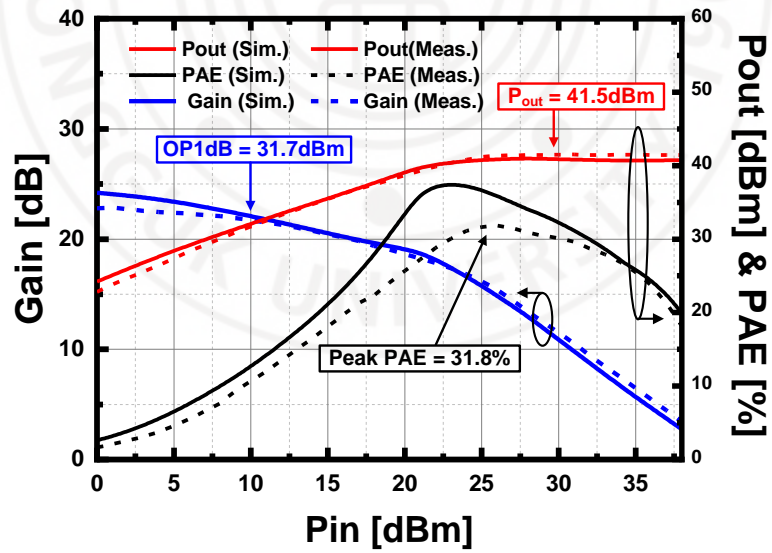


Figure 5.1-4 Large signal measurement result of the Tx side.

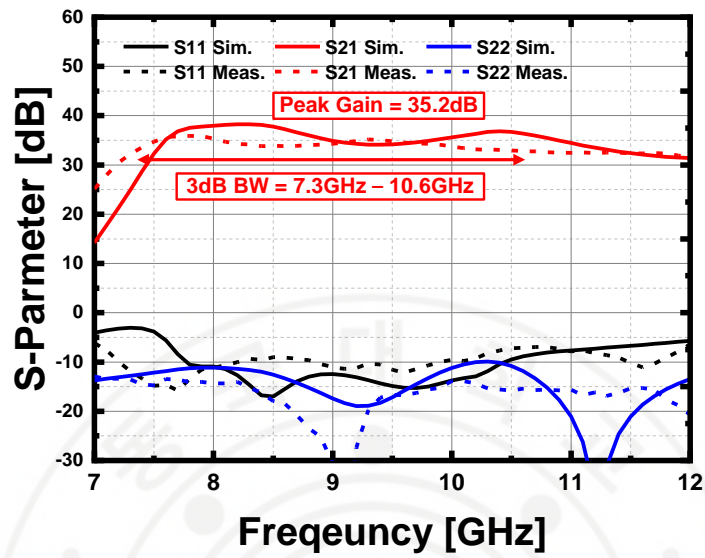


Figure 5.1–5 Small signal measurement result of the Rx side.

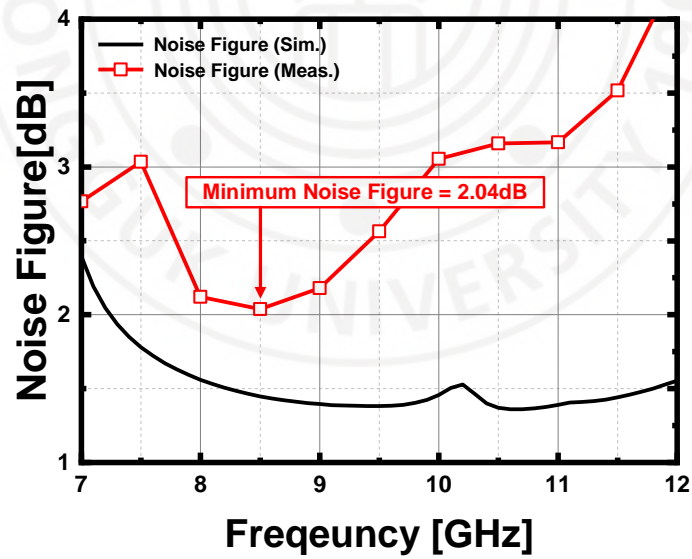


Figure 5.1–6 Noise figure measurement result of the Rx side.

<Table 5.1–1> Comparison table of fabricated transceiver.

	This work	[43]	[44]	[45]
Tech. [μm]	0.25 μm AlGaIn/GaN	0.25 μm AlGaIn/GaN	0.25 μm AlGaIn/GaN	0.25 μm AlGaIn/GaN
	Tx			
BW. [GHz]	8.6–10.9	8.6–11.2	9–12	7.7–12.2
Small– signal Gain. [dB]	<23.3	<25	<24.1	<35
Output Power. [dBm]	<41.5	<39	<38.2*	<42.3
PAE [%]	<31.8	<25	<28	<29
	Rx			
BW. [GHz]	7.3–10.6	7.5–11.5	7.8–10.2	7.7–12.2
NF. [dB]	>2.04	>2.5	>2.3*	>2.8
Gain. [dB]	<35.2	<16	<19	<14.5
Stage	4	2	2	2
Chip Size [mm ²]	6 × 5.1	3 × 3	3.6 × 3.3	4.8 × 2.7

In all measurements, the Tx drain bias voltage was $V_{DD,Tx} = 28V$, the Tx gate bias voltage was $V_{GG,Tx} = -2.2V$, the Rx drain bias voltage was $V_{DD,Rx} = 10V$, the Rx gate bias voltage was $V_{GG,Rx} = -2.2V$ and the control voltage was $V_{ctrl} = -28V$.

Figure 5.1–3 depicts the small–signal measurement results of Tx side of designed transceiver. In the small signal measurement, the measured 3dB bandwidth of the Tx was 8.6GHz – 10.9GHz. The measured gain of the transmitter chain was 23.3dB at 9.4GHz. The measured S11 of the input of the designed PA was $-26.2dB$ at 9GHz and the measured S22 of the designed PA was $-8.9dB$ at 9GHz.

Figure 5.1–4 depicts the large–signal measurement results of the designed PA. In the large signal measurement, the output power of the designed PA was 41.5dBm at 9.5GHz. The achieved peak PAE was measured to be 31.8% at 9.5GHz. And measured OP1dB was 31.7dBm.

Figure 5.1–5 depicts the small–signal measurement results of Rx side of designed transceiver. In the small signal measurement, the measured 3dB bandwidth of the Rx was 7.3GHz – 10.6GHz. The measured gain of the receive chain was 35.2dB at 9.2GHz. The measured S11 of the input of the designed PA was $-11.6dB$ at

9.5GHz and the measured S22 of the designed LNA was -16.7dB at 9.5GHz.

Figure 5.1-6 depicts the noise figure of Rx side of designed transceiver. In the noise figure measurement, the measured noise figure was 2.04dB at 8.5GHz.

Table 5.1-1 presents the comparison table of fabricated X-Band transceiver in GaN Technology. As can be seen in table 5.1-1, designed transceiver achieved the highest PAE of 31.8% and the lowest noise figure of 2.04dB whose value is highly comparable.

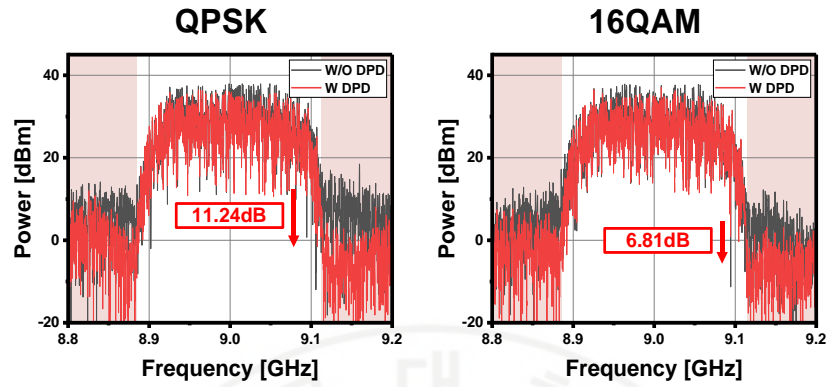


Figure 5.1–7 Output signal spectrum of QPSK and 16QAM with and without DPD.

	QPSK	
	w/o DPD	w DPD
Measured Constellation		
EVM	12.36%rms	6.21%rms
	16QAM	
	w/o DPD	w DPD
Measured Constellation		
EVM	5.64%rms	2.46%rms

Figure 5.1–8 QPSK and 16QAM constellation with and without DPD.

To assess the high-speed communication capability of the developed transceiver, performance measurements were carried out using modulated waveforms.

Figure 5.1–7 presents the spectral output of the transmitter when driven by QPSK and 16QAM signals centered at 9.5 GHz with a 100 MHz bandwidth, both before and after DPD was applied. As shown, the ACLR for the QPSK waveform improved by 11.24 dB with DPD, while the 16QAM signal exhibited a 6.81 dB enhancement.

In Figure 5.1–8, the output constellation diagrams for the QPSK and 16QAM signals are displayed, also at a 9.5 GHz carrier and 100 MHz bandwidth. These were captured both prior to and following the application of DPD. The error vector magnitude (EVM) achieved after DPD was 6.21% rms for QPSK, and 2.46% rms for 16QAM. These results confirm the stable and effective operation of the fabricated transceiver under complex modulation schemes, indicating its suitability for high-speed data transmission.

5.2 PSLR Measurement

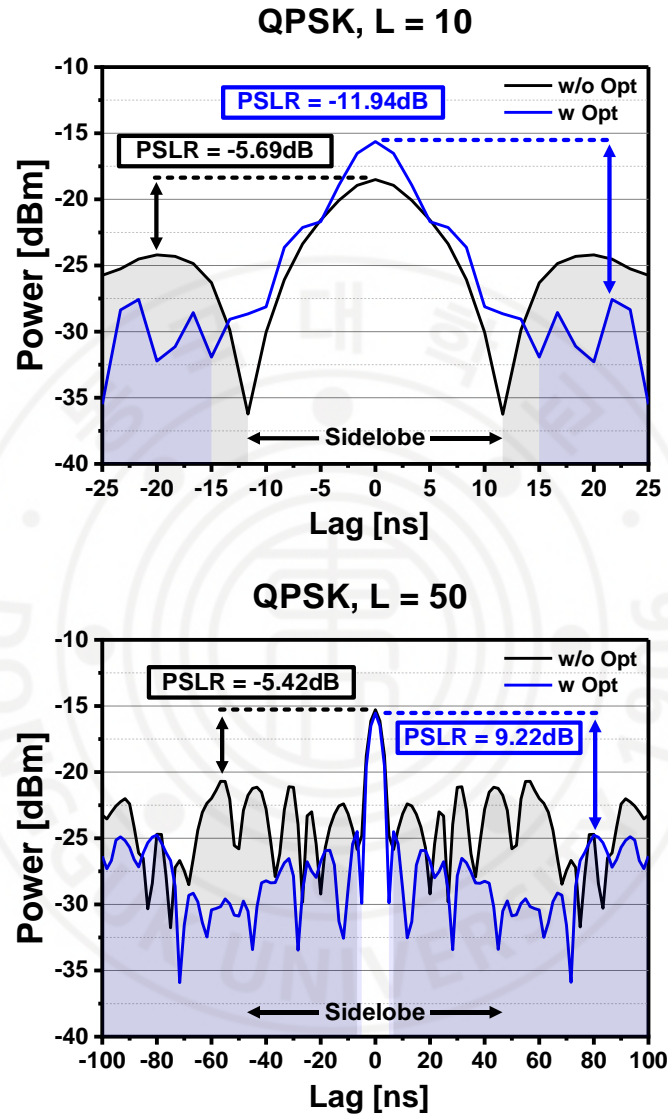


Figure 5.1–9 Autocorrelation and PSLR measurement results with and without code optimization in QPSK signal for code sequence lengths of 10 and 50.

In order to thoroughly verify the PSLR enhancement achieved through our code sequence optimization, a set of measurements was performed based on the experimental configuration previously described.

Figure 5.1–9 shows the autocorrelation outputs for unoptimized random code sequences and compares them with those obtained after applying the proposed optimization technique. The test was carried out using a 9.5 GHz QPSK–modulated signal transmitted via the Tx chain. To evaluate the robustness and scalability of the optimization, experiments were conducted with code sequence lengths of 10 and 50.

For a sequence length of 10, the PSLR improved notably from -5.69 dB to -11.94 dB after optimization. In the case of a length 50 sequence, the PSLR improved from -5.42 dB to -9.22 dB. These results verify the effectiveness of the proposed optimization technique in suppressing sidelobe levels and demonstrate its practical benefit in enhancing signal correlation characteristics under real–world transmission conditions.

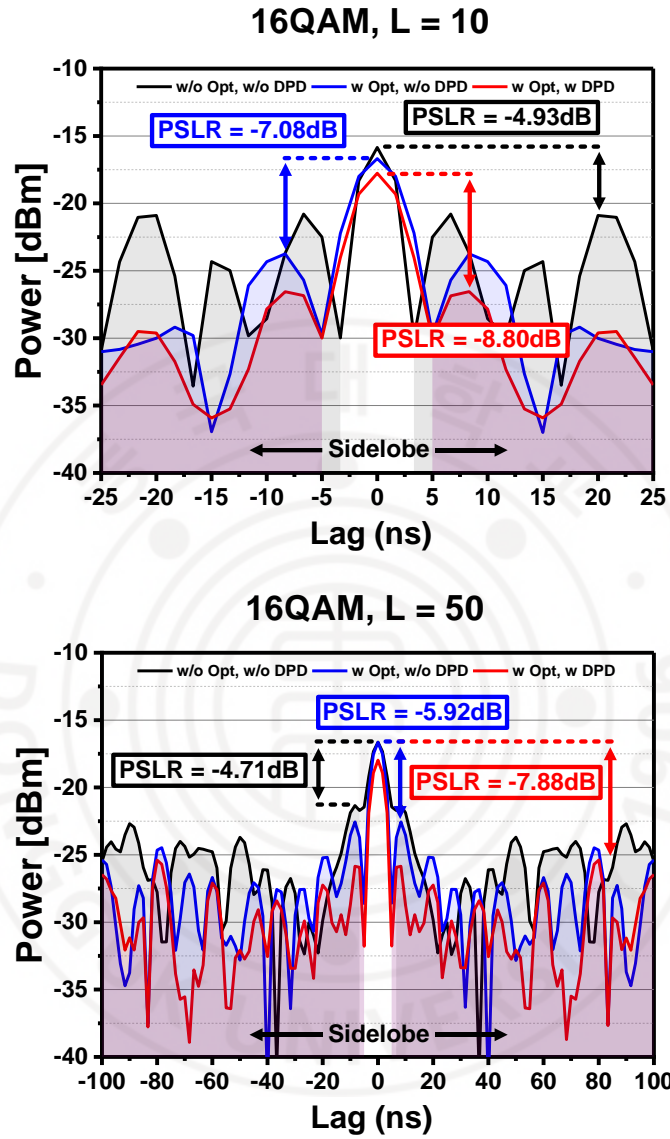


Figure 5.1–10 Autocorrelation and PSLR measurement results for a 16QAM signal with code sequence lengths of 10 and 50 in the cases of without code optimization & without DPD, with code optimization & without DPD, and with code optimization & with DPD.

To assess the degree of PSLR improvement enabled by our code sequence optimization technique and the application of DPD in the case of 16QAM modulation, a series of measurements was carried out using the previously described experimental setup.

Figure 5.1–10 presents a comparison of the autocorrelation outcomes for three scenarios involving a 9.5 GHz carrier modulated with 16QAM and transmitted through the Tx path: (i) using a random code sequence without optimization or DPD, (ii) after applying the code sequence optimization only, and (iii) after applying both optimization and DPD.

For a code length of 10, the PSLR was measured as -4.93 dB in the unoptimized and non-linearized case. This improved to -7.08 dB with only the optimization applied, and further to -8.80 dB when both optimization and DPD were applied.

For a code length of 50, the PSLR was measured as -4.71 dB in the unoptimized and non-linearized case. This improved to -5.92 dB with only the optimization applied, and further to -7.88 dB when both optimization and DPD were applied.

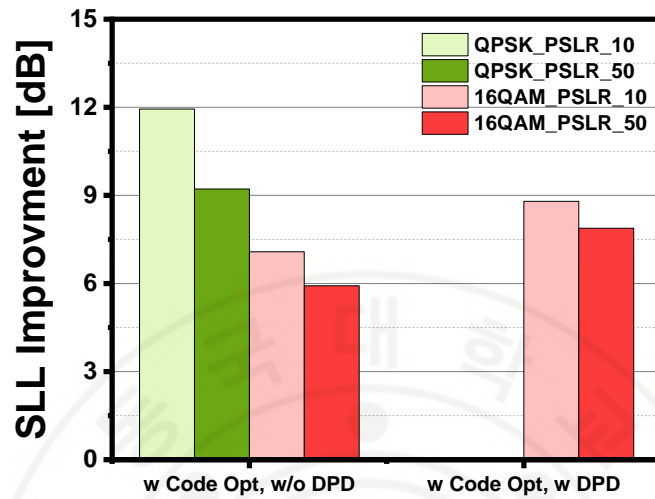


Figure 5.1–11 PSLR measurement result for QPSK and 16QAM signal when code length is 10 and 50

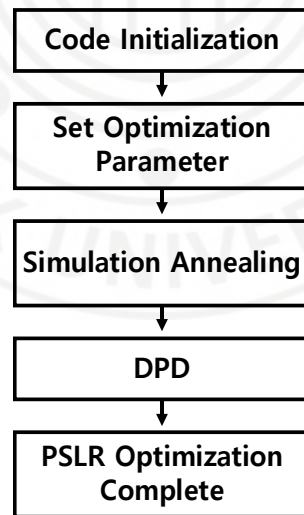


Figure 5.1–12 Overall flow chart of code sequence optimization

Figure 5.1–11 presents the PSLR measurement results for QPSK and 16QAM signals with code lengths of 10 and 50. As shown in Figure 5.1–11, a shorter code length resulted in more significant PSLR improvement. Moreover, the 16QAM signal, which has higher spectral efficiency, exhibited greater improvement in PSLR. The application of DPD also contributed to further enhancement of the PSLR performance.

Figure 5.1–12 depicts the overall flow chart of code sequence optimization. These results demonstrate that the proposed code sequence optimization effectively improves the PSLR. Furthermore, it highlights the synergistic effect of integrating both code sequence optimization and DPD in enhancing sidelobe suppression performance. In particular, the greater PSLR improvement observed for higher order modulation schemes, such as 16QAM, suggests that the proposed approach is well suited for high data rate communication scenarios where spectral efficiency is critical. The ability to maintain low sidelobe levels under such modulation formats is essential for ensuring reliable radar target detection and reducing interference in densely populated spectral environments. Therefore, the proposed method offers a promising solution for next generation DFRC

systems that demand both spectral efficiency and signal clarity.



Chapter VI. Conclusion

This study presents the design of a monolithic transceiver based on a 250 nm GaN process, integrating a 4-way Power Amplifier (PA), a 4-stage Low Noise Amplifier (LNA), and a T/R switch into a single MMIC. By incorporating $\lambda/4$ transmission lines and LC resonators, second- and third-order harmonics were effectively suppressed, achieving a peak PAE of 31.8% and a minimum NF of 2.04 dB. These results satisfy both linearity and efficiency requirements essential for dual-function radar-communication (DFRC) systems.

To maximize hardware performance, simulated annealing (SA)-based code sequence optimization was employed. For QPSK, the Peak Sidelobe Level Ratio (PSLR) improved from -10.46 dB to -16.99 dB ($L = 10$) and -19.36 dB ($L = 50$). For 16QAM, the PSLR was enhanced from -6.15 dB to -22.92 dB ($L = 10$) and -10.58 dB to -21.33 dB ($L = 50$). These results were statistically validated through 10,000 trials, confirming that the SA algorithm—configured with 5,000 iterations, an initial temperature of 10, a final temperature of 10^{-6} , and a cooling rate of 0.95—successfully escapes local minima and converges to globally optimal solutions.

In practical measurements, code optimization alone reduced the QPSK sidelobes from -5.69 dB to -11.94 dB ($L = 10$) and -5.42 dB to -9.22 dB ($L = 50$), while 16QAM showed improvements from -4.93 dB to -7.08 dB ($L = 10$) and -4.71 dB to -5.92 dB ($L = 50$). When combined with memory-polynomial DPD, the 16QAM PSLR further decreased to -8.80 dB ($L = 10$) and -7.88 dB ($L = 50$), offering an additional 3–4 dB gain over code optimization alone. Furthermore, ACLR improved by 6.81 dB and EVM was reduced by 3.18 percentage points. These findings experimentally demonstrate that the joint hardware (linearity-enhancement circuits) and software (SA-based code optimization and DPD) co-design approach effectively maximizes both radar detection performance and communication efficiency, even in high-order modulation environments.

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국문 초록

본 학위 논문은 GaN 기반 X-대역 AESA 레이더 송수신기에서 Peak Sidelobe Ratio (PSLR)를 개선하기 위한 방법을 제안한다. 제안된 송수신기는 250 nm GaN HEMT 공정을 기반으로 하여 전력 증폭기(PA), 저잡음 증폭기(LNA), 그리고 SPDT T/R 스위치를 단일 칩에 통합하였다. GaN 소자의 고유한 비선형 왜곡 및 고조파 성분을 억제하기 위해, $\lambda/4$ 전송선로와 LC 공진기를 활용한 2차 및 3차 고조파 필터링 구조가 도입되었다.

또한, 변조 복잡도 및 PA의 비선형성에 기인한 PSLR 열화를 완화하기 위해 시뮬레이션 어닐링(SA) 기반의 최적화 알고리즘을 적용하였다. 본 알고리즘은 코드 시퀀스 최적화를 효율적으로 수행할 수 있도록 설계되었다. 더불어, 특히 16QAM과 같이 PAPR이 높은 신호에 대해 선형성을 향상시키기 위해 메모리 다항식 기반의 디지털 사전왜곡(DPD) 기법을 적용하였다.

제작된 송수신기의 측정 결과, 41.5 dBm의 출력 전력, 31.8%의 전력 이득 효율(PAE), 2.04 dB의 잡음지수를 달성함으로써 우수한 성능을 확인하였다. PSLR 측정 결과에서는 코드 최적화 및 DPD 기법이 PSLR을 효과적으로 개선함을 보여주었다. 이러한 결과는 제안된 기법이 사이드 로브를 효과적으로 억제하고, 향후 레이더-통신 통합 시스템(DFRC)을 위한 실질적인 해결책이 될 수 있음을 입증한다.