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Doctoral Dissertation

Studies on RF Beamforming CMOS Frontends for 6G Communications

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2026

Doctoral Dissertation

Studies on RF Beamforming CMOS Frontends for 6G Communications

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Advisor Jung-Dong Park

Thesis submitted for the Degree of Doctor.

June, 2026

This thesis, submitted for the Degree of Doctor of Engineering and authored by Jeong-Moon Song, is hereby accepted and approved.

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ABSTRACT

This dissertation presents a systematic design framework for silicon-based RF beamforming frontends, addressing the strategic two-track spectrum expansion of next-generation 6G communication systems. To overcome the practical limitations of 5G millimeter-wave deployments, this work investigates the 'Upper Mid-band' (X-band) for highly reliable wide-area coverage and the 'Sub-THz' (sub-THz and D-band) for extreme data throughput. Rather than focusing on a single circuit block, this research strategically selects CMOS and SiGe BiCMOS technologies based on the dominant design constraints of each frequency band. By doing so, it addresses the beamforming-frontend problem through a continuous progression of topics, including accurate wideband signal alignment, multifunction frontend integration, high-frequency receiver architecture, and high-efficiency transmitter design. In this way, the dissertation organizes the essential challenges of RF beamforming frontends along the three axes of signal control, frontend integration, and frequency scaling.

Chapter 1 introduces the background and motivation of wideband beamforming systems and discusses why delay accuracy, channel consistency, and frontend integration become increasingly important as the operating frequency extends from X-band toward sub-THz and D-band regions. Chapter 2 presents a 5-11 GHz 8-bit passive true-time-delay circuit implemented in 65-nm CMOS. By combining a precision fine-delay structure for the lower bits and conventional LC-based delay cells for the upper bits, the proposed circuit achieves a minimum delay step of 1.56 ps, a maximum delay of 400 ps, and reduced insertion loss variation without DC power consumption. Chapter 3 presents a 65-nm CMOS X-band

multifunction chip integrating a hybrid passive phase shifter, attenuator, amplifier blocks, and Tx/Rx switching. The proposed multifunction chip achieves compact integration together with low RMS phase and gain errors, and its packaging effect is analyzed and minimized through appropriate design techniques. Chapter 4 presents two 275 GHz quadrature receivers implemented in 130-nm SiGe BiCMOS, namely mixer first and LNA first topologies. The measured results demonstrate that both architectures support broadband down conversion with high gain and wide IF bandwidth, while showing a clear trade-off among sensitivity, chip area, and power consumption. Chapter 5 presents a D-band transmitter implemented in 40-nm CMOS to improve transmitter efficiency under 16-QAM operation. By employing an uneven-saturation dual-PA architecture together with wideband phase equalization, the proposed transmitter achieves high output power and state-of-the-art modulated efficiency while maintaining acceptable modulation accuracy. Finally, Chapter 6 concludes the dissertation by summarizing the overall contributions, and Chapter 7 discusses future extensions toward fully integrated multi-channel beamforming transceivers and scalable sub-THz frontend systems.

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Chapter 1. Introduction

1.1. Research Background

Next-generation wireless communication systems demand not only high data rate transmission, ultra-low latency connectivity, and massive simultaneous access, but also precise spatial control [1.1]-[1.4].

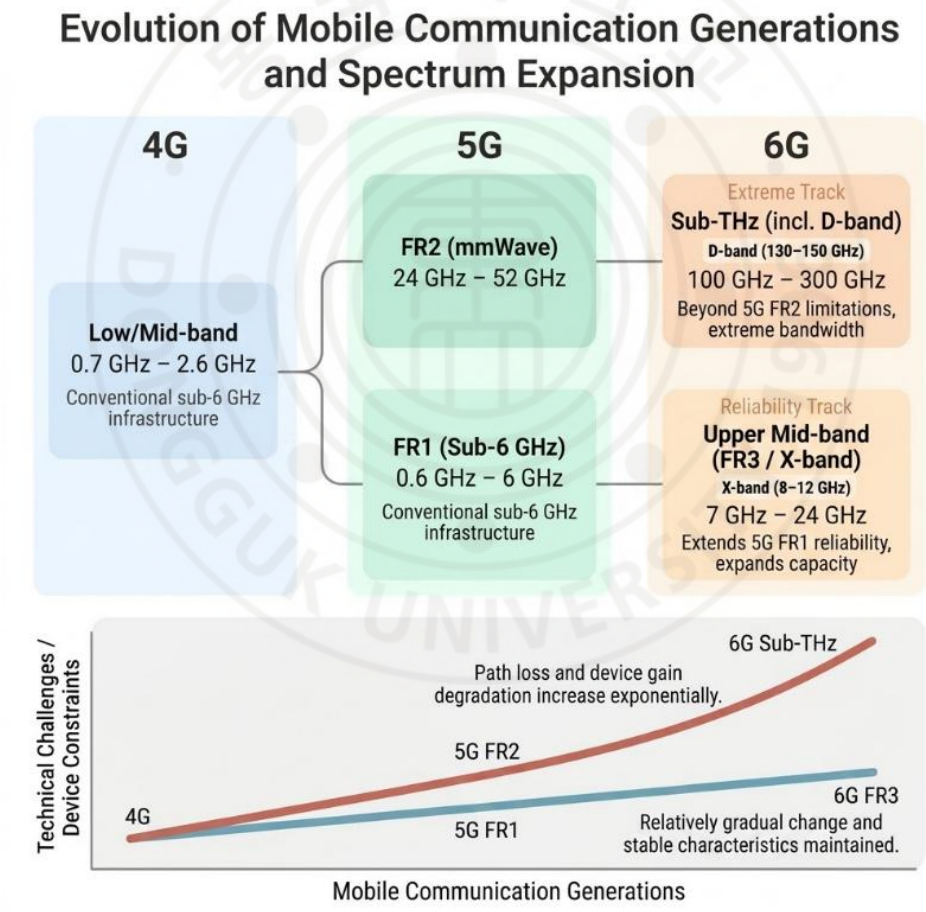


Figure 1.1 Evolution of next-generation wireless systems.

While 5G systems introduced mainstream sub-6 GHz (FR1) and millimeter-wave (FR2) bands to achieve high data rates, the practical deployment of FR2 (24–52 GHz) has faced significant challenges in terms of limited coverage, high path loss, and prohibitive infrastructure costs. Lessons learned from these commercial hurdles have driven a paradigm shift in the 6G roadmap toward a diversified spectrum expansion [1.5].

As illustrated in Figure **1.1**, 6G is simultaneously targeting the 'Upper Mid-band' (FR3, including X-band, 7–24 GHz) to ensure reliable wide-area coverage and the 'Sub-THz' (including D-band, 100–300 GHz) to secure extreme throughput for specialized short-range links [1.5], [1.6].

These higher-frequency bands provide large available bandwidths, but they also entail fundamental limitations, including increased free-space path loss, stronger sensitivity to blockage, reduced gain margin of active devices, and increased losses in passive components and packaging. As a result, in next-generation wireless systems operating at high frequencies, a single antenna path is no longer sufficient to secure an adequate link budget, and efficient control of electromagnetic energy in the spatial domain becomes indispensable [1.1]-[1.4].

Under these conditions, beamforming has emerged as a key enabling technology for high-frequency wireless systems.

Beamforming is a technique that concentrates electromagnetic energy in a desired direction by controlling the phase, time delay, and amplitude of the signals applied to the elements of an antenna array. In transmitters, it enhances the effective radiated power through array gain, whereas in receivers, it improves directional selectivity and suppresses interference through spatial filtering. The capacity gain of multi-antenna channels and the necessity of beamforming have been systematically established through classical MIMO theory and subsequent millimeter-wave MIMO studies [1.1]-[1.3].

Nevertheless, the actual performance of beamforming is not determined solely by ideal array theory. Although the complex weights assigned to array elements are mathematically concise, in practical hardware they must be realized by physical circuit blocks such as phase shifters, true-time-delay elements, attenuators, amplifiers, power dividers, switches, and package/interconnect structures. Therefore, the phase and amplitude relationships required at the array level ultimately depend on the signal-control accuracy of each RF frontend channel.

1.2. Technical Challenges of Beamforming Frontends

The essence of beamforming lies in imposing appropriate relative signal conditions on each channel of an antenna array. For a uniform linear array (ULA) consisting of N elements with spacing d, the array factor is expressed as

$$AF(\theta) = \sum_{m-0}^{N-1} \omega_m e^{jmkd\sin\theta} \tag{1.1}$$

where w_m denotes the complex weight applied to the m^{th} element, $k=2\pi/\lambda$ is the wavenumber, and θ is the observation angle. Ideally, when proper weights are applied to all channels, signals combine constructively in the desired direction and destructively elsewhere. In practical RF frontends, however, these relative signal relationships cannot be maintained ideally, and this is precisely where the core design challenges of beamforming circuits arise.

The first challenge is the limitation of phase-based steering in wideband environments. The phase response of a signal with a time delay τ is given by

$$\phi(\omega) = -\omega\tau \tag{1.2}$$

where ω is the angular frequency. In contrast, the equivalent time delay of a phase shifter imposing a fixed phase difference $\Delta\phi$ is

$$\tau_{eq}(\omega) = -\frac{\Delta\phi}{\omega} \tag{1.3}$$

which is frequency-dependent. In other words, a phase relationship established at one frequency does not guarantee the same time alignment over the entire signal band. For an array with a fixed phase difference $\Delta\phi$ between adjacent elements, the steering angle is written as

$$\sin\theta(f) = -\frac{c\Delta\phi}{2\pi fd} \tag{1.4}$$

where c is the speed of light. Equation (1.4) clearly indicates that the steering angle varies with frequency f, which leads to the beam-squint phenomenon in wideband systems [1.7].

Beam squint is not merely a phase error; it directly results in reduced array gain, degraded link quality, and distorted spatial response. This effect becomes more severe as the bandwidth and steering angle increase. For this reason, in wideband phased arrays, delay-control accuracy and group-delay characteristics emerge as critical design metrics. This has motivated the adoption of true-time-delay (TTD)-based beam steering, and recent CMOS TTD studies for wideband phased arrays have primarily focused on trade-offs among delay-bandwidth product, delay variation, insertion loss, and chip area [1.8], [1.9].

The second challenge is the accumulation of channel-control errors. A practical beamforming frontend must maintain not only phase or delay accuracy but also gain accuracy across channels. Phase, gain, and delay errors among channels make signal combination incomplete in the intended direction, thereby shifting the main beam or increasing sidelobe levels. Errors that appear negligible in a single channel may accumulate across many channels and substantially degrade the overall beamforming performance. Therefore, beamforming circuits must be evaluated not only by their absolute performance but also by their inter-channel consistency.

The third challenge is the complexity introduced by multifunction integration. A practical beamforming channel is not composed solely of a phase shifter or a delay cell. It must also include amplitude control, transmit/receive mode switching, amplification, impedance matching, and digital control interfaces. As these functions are integrated into a single channel, circuit area, insertion loss, parasitics, mutual interaction, and stability issues inevitably increase.

The fourth challenge is the shift in dominant design constraints dictated by this bifurcated spectrum strategy. In the reliability track (X-band and FR3), where large-scale arrays are prioritized for wide-area coverage, the focus lies on achieving extreme delay accuracy and compact multifunction integration to overcome beam-squinting and channel mismatch. In contrast, for the extreme throughput track (D-band and sub-THz), the primary bottlenecks shift toward overcoming severe device gain degradation, high passive loss, and maximizing power efficiency under high-order modulation. Thus, the design of high-frequency frontends requires not a simple frequency scaling of conventional structures, but rather a strategic redefinition of circuit architectures tailored to each frequency regime.

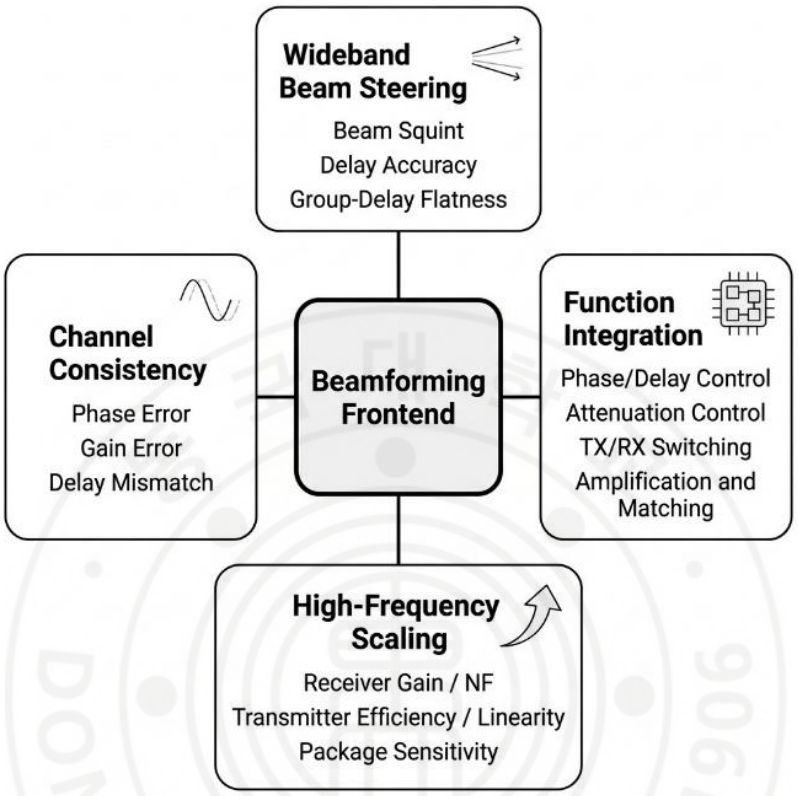


Figure 1.2 Major technical challenges of beamforming frontends.

The four challenges discussed above define the circuit level problem of practical beamforming frontends. Figure 1.2 summarizes these challenges in a unified manner: the limitation of phase-based wideband control, the accumulation of channel-to-channel errors, the increasing burden of multifunction integration, and the shift in dominant design constraints as the operating frequency extends from X-band to sub-THz and D-band regions. These four issues provide the technical basis for the chapter organization of this dissertation.

In particular, Chapters 2 and 3 focus on accurate signal control and multifunction integration in X-band CMOS frontends, whereas Chapters 4 and 5 address the gain, noise, and efficiency limitations that become dominant in sub-THz and D-band implementations.

Figure 1.3 illustrates the beam-squint phenomenon in a phase-controlled wideband array. When a fixed phase offset is applied between adjacent antenna elements, the corresponding effective time delay becomes frequency-dependent. As a result, the steering angle that is accurately established at the center frequency is not preserved over the entire signal band. Lower-frequency components experience a larger effective delay, whereas higher-frequency components experience a smaller one, so the main beam direction shifts across frequency. This frequency-dependent beam deviation reduces coherent array gain and distorts the intended radiation pattern, especially under wideband operation and large steering angles. Therefore, a phase-shifter-based frontend is fundamentally limited in broadband beamforming, which directly motivates the use of true-time-delay-based signal control.

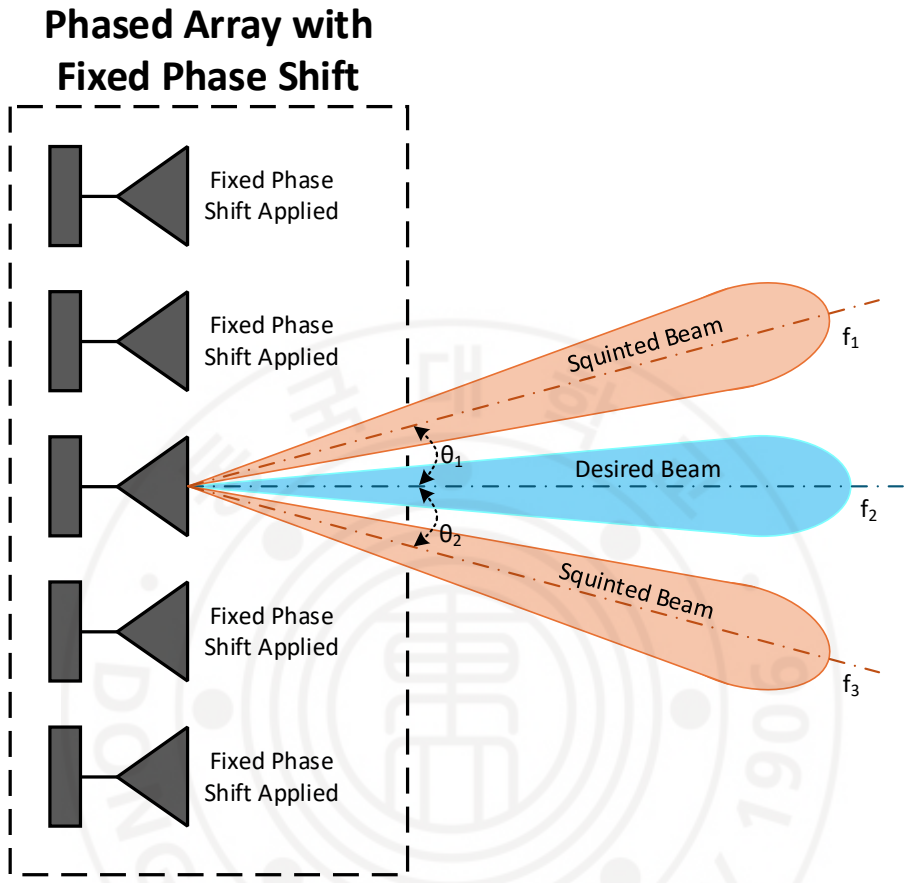


Figure 1.3 Conceptual illustration of beam squint in wideband phase-controlled beamforming.

1.3. CMOS as a Practical Platform for Wideband Beamforming Frontends

Several implementation technologies are available for high-frequency beamforming systems, including III-V compound semiconductors, SiGe, and CMOS. Among them, CMOS offers distinct advantages in low fabrication cost, high integration density, and

strong compatibility with digital circuitry. In large-scale array systems, as the number of channels increases, not only RF building blocks but also control logic, calibration circuits, and digital interfaces become necessary. Accordingly, CMOS becomes increasingly attractive as a platform capable of integrating both RF and digital functions.

Furthermore, a beamforming frontend is not a single isolated high-performance block such as a standalone power amplifier. Rather, it consists of a large number of medium-performance RF blocks repeated across many channels. In such systems, the key design criterion is not the maximum standalone performance of each device, but how uniformly, compactly, and controllably a large number of channels can be realized. In this sense, CMOS is particularly well suited for highly integrated beamforming frontends. In fact, previous studies have demonstrated the feasibility of CMOS-based X-band phase shifters, transceivers, bidirectional T/R chipsets, and phased-array receivers [1.10]-[1.13].

Despite these advantages, CMOS-based beamforming circuits also suffer from clear limitations. Low device breakdown voltage is unfavorable for high-output transmitters and low-loss switching networks. As the operating frequency increases, the gain margin of transistors decreases, thereby reducing the design margin of both receivers and transmitters. In addition, the limited quality factor of passive components and routing parasitics may introduce substantial

loss in matching networks, delay lines, transformers, and switch networks. Moreover, packaging and PCB interconnects have a direct impact on circuit behavior at high frequencies, making it difficult to guarantee final system performance solely through on-chip design.

Nevertheless, CMOS-based high-frequency beamforming circuits remain highly important because future 6G multi-channel beamforming systems will likely require a high degree of integration, digital controllability, inter-channel consistency, and compactness. CMOS is the most realistic platform capable of accommodating these requirements simultaneously. Therefore, the relevant question is not how to avoid the limitations of CMOS, but rather what circuit structures and design strategies are most effective under its constraints.

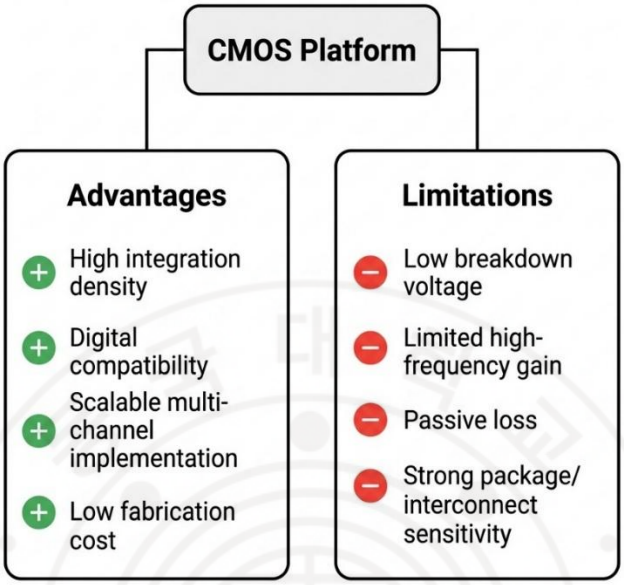


Figure 1.4 Advantages and limitations of the CMOS platform for high-frequency beamforming systems.

Figure 1.4 shows why CMOS is a practical platform for beamforming frontends despite its limitations. High integration density and digital compatibility make CMOS attractive for large-scale arrays, whereas low breakdown voltage, passive loss, and reduced gain margin remain the main constraints.

The figure highlights the dual nature of CMOS for beamforming frontends. CMOS is highly attractive because of its low cost and strong digital integration capability, but it simultaneously suffers from limited breakdown voltage, reduced high-frequency gain margin, and non-negligible passive and packaging parasitics.

1.4. Research Objectives

The objective of this dissertation is to establish a systematic design framework for silicon-based RF beamforming frontends applicable to next-generation 6G communication systems. To this end, this work strategically selects process technologies (CMOS and SiGe BiCMOS) based on the dominant design constraints of each frequency band. Rather than focusing on a single circuit block, it develops a continuous research framework that begins with the problem of signal control in highly integrated CMOS platforms (X-band), extends to high-frequency SiGe receiver architectures to overcome f_{max} limitations (sub-THz), and further expands to high-efficiency CMOS transmitter design (D-band).

The first objective is to address the problem of accurate signal alignment in wideband environments. Considering the beam-squint limitation inherent to phase-based beamforming, beamforming circuits should be reinterpreted in terms of time-alignment accuracy over the entire operating band rather than phase compensation at a single frequency.

The second objective is to extend this concept of signal control to the level of a practical frontend architecture. By integrating phase or delay control together with amplitude control, transmit/receive mode switching, amplification, and matching, this dissertation seeks to establish a channel architecture suitable for practical phased-array implementation.

The third objective is to investigate how the dominant design criteria evolve as the operating frequency is extended. As the problem framework established at X-band is extended into the sub-THz and D-band regions, this work examines what receiver structures become effective and how transmitter architectures can be designed to achieve both efficiency and linearity.

Ultimately, the dissertation aims to organize CMOS-based RF beamforming frontends from the perspectives of frequency scaling and functional expansion, and thereby provide a circuit level foundation for future highly integrated multi-channel 6G beamforming systems. The overall research flow corresponding to this objective is summarized in Figure 1.5.

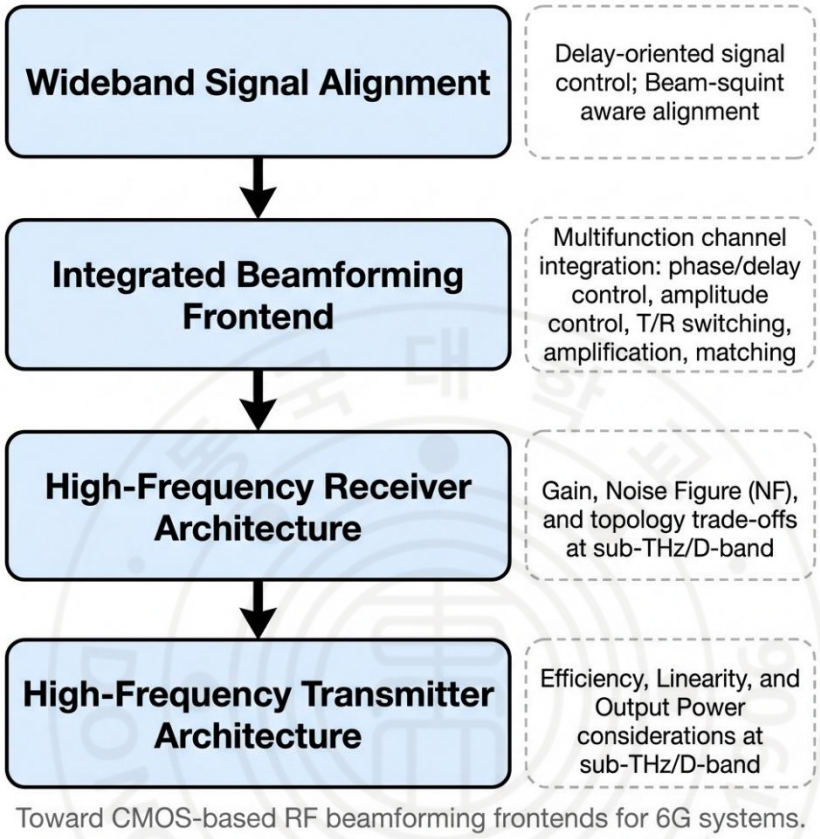


Figure 1.5 Research objectives and approach of this dissertation.

1.5. Significance and Distinctiveness of This Research

The significance of this research lies in the fact that it does not limit the beamforming-frontend problem in next-generation high-frequency wireless systems to the performance improvement of an isolated circuit block. Instead, it addresses the problem through the linked issues of signal control, multifunction frontend integration, and scalability toward higher frequency bands.

First, this work interprets beamforming not merely as an array-steering problem, but as a channel-wise RF signal-control problem. The ideal complex weights required at the array level are realized in hardware through phase, delay, gain, and loss characteristics, and the overall beamforming performance is therefore determined by the precision of each frontend channel. Second, this work identifies beam squint in wideband environments as a key circuit level issue and reinterprets the limitation of phase-based steering from the viewpoint of temporal alignment, thereby providing a frontend-oriented rationale for delay-based beamforming approaches. Third, this work extends the signal-control problem to the structure of an actual multifunction RF frontend, where amplitude control, transmit/receive reconfiguration, amplification, matching, and control interfaces must be integrated within a single channel. Fourth, this work extends the discussion from X-band to the sub-THz and D-band regions, thereby connecting lower-frequency frontend issues with the design of high-frequency receivers and transmitters within one continuous framework.

In summary, the distinctiveness of this research does not lie in maximizing the standalone performance of any single circuit. Rather, it lies in organizing the essential problems of beamforming in a stepwise manner along three key design dimensions: signal control, frontend integration, and high-frequency extension.

Circuit designs and measurement results presented in this

dissertation were obtained through collaborative research within the MEIC laboratory. The specific block level contributions of the author and co-workers are noted in the corresponding chapters, together with the design, measurement, and analysis results.

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Chapter 2. Passive True-Time Delay

2.1. Introduction

True-time delay (TTD) is a key beam-steering element for broadband phased-array systems because it directly controls the relative delay between antenna channels and thereby mitigates the beam-squint problem inherent to phase-shifter-based steering [2.1]-[2.6]. Unlike a phase shifter, which provides a fixed phase step only at a given operating frequency, a TTD maintains the desired temporal alignment over frequency and is therefore more suitable for broadband phased-array antennas and next-generation wideband wireless systems.

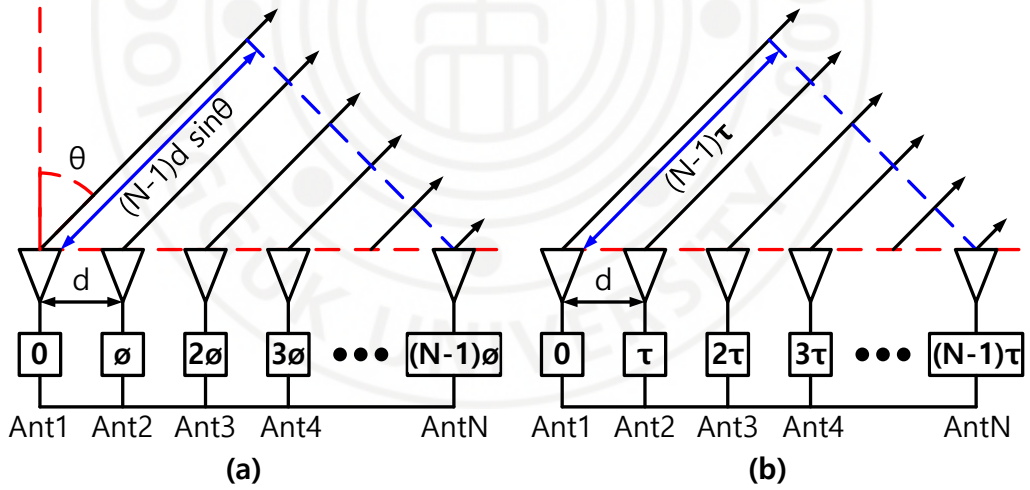


Figure 2.1 Basic concept of beam steering using (a) a phase shifter and (b) a true-time delay.

Phase shifters have nevertheless remained attractive because of their compactness and implementation simplicity. Conventional phase shifters have been implemented as quadrature, vector, and filter-based structures [2.7]-[2.12]. However, because the equivalent delay associated with a fixed phase shift is frequency-dependent, phase-shifter-based steering fundamentally suffers from beam squint in broadband operation [2.12].

In integrated implementations, TTD circuits are commonly realized using artificial transmission lines constructed from lumped inductors and capacitors [2.1], [2.5], [2.6]. Conventional LC-based delay cells, however, suffer from parasitic effects and self-resonance-frequency limitations of passive components. As the operating frequency approaches the self-resonance region, the effective passive values deviate from the intended design values, causing both delay error and insertion loss variation. Trombone-based and active-assisted approaches have been proposed to alleviate these limitations [2.1]-[2.4], but they generally involve either increased complexity or nonzero DC power consumption. Moreover, achieving sub-2-ps delay resolution is particularly difficult in conventional LC delay cells because the minimum controllable delay step is strongly constrained by parasitics [2.13]. The implemented circuit discussed in this chapter operates from 5 to 11 GHz, provides a minimum delay step of 1.56 ps and a maximum delay of 400 ps, consumes no DC power, and occupies $2.76 \times 1.01\ mm^2$ including RF and DC pads.

2.2. Analysis of Conventional LC-Based Delay Elements

A compact on-chip delay element can be realized using a π-type LC network consisting of a series inductor L and two shunt capacitors C/2. For a unit π section, the delay time and pole frequency are given by

$$t_D = \sqrt{LC} \tag{2.1}$$

And

$$f_C = \frac{1}{\pi\sqrt{LC}} \tag{2.2}$$

respectively. The passive values may be selected from the desired phase shift $\Delta\phi$ and characteristic impedance Z_0 as

$$L = -\frac{Z_0 \sin(\Delta\phi/2)}{\omega} \tag{2.3}$$

$$C = -\frac{\tan(\Delta\delta\phi/4)}{\omega Z_0} \tag{2.4}$$

where $\Delta\phi = \omega_0 t_D$. If n unit sections are cascaded, the total delay becomes

$$T_D = n\sqrt{LC} \tag{2.5}$$

As shown in Figure 2.2, the simplest implementation is a single π section delay element. This structure is compact, but it requires

relatively large values of L and C to realize a large delay. Under such conditions, the self-resonance frequency of the passive components may approach the operating band, and the effective reactance values change significantly with frequency. As a result, the group delay deviates from that of an ideal transmission line, and both group-delay error and insertion loss variation become substantial.

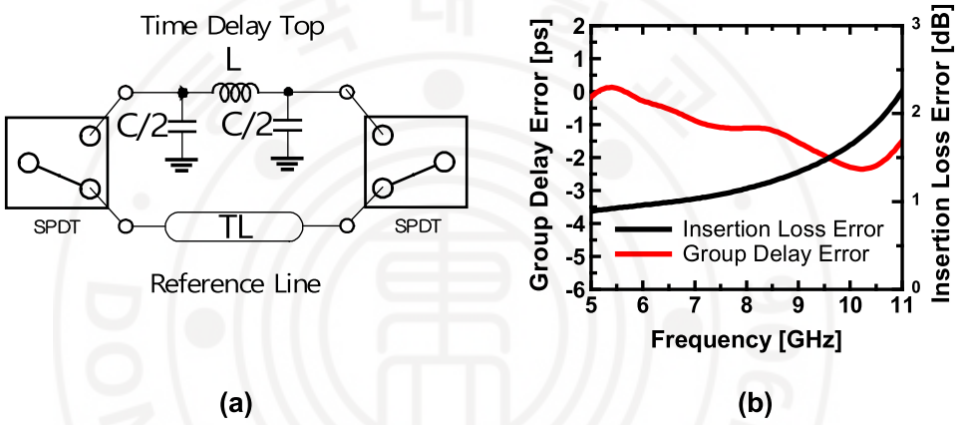


Figure 2.2 (a) Schematic diagram of the conventional delay element with a single π-section. (b) Group delay error and insertion loss error over frequency.

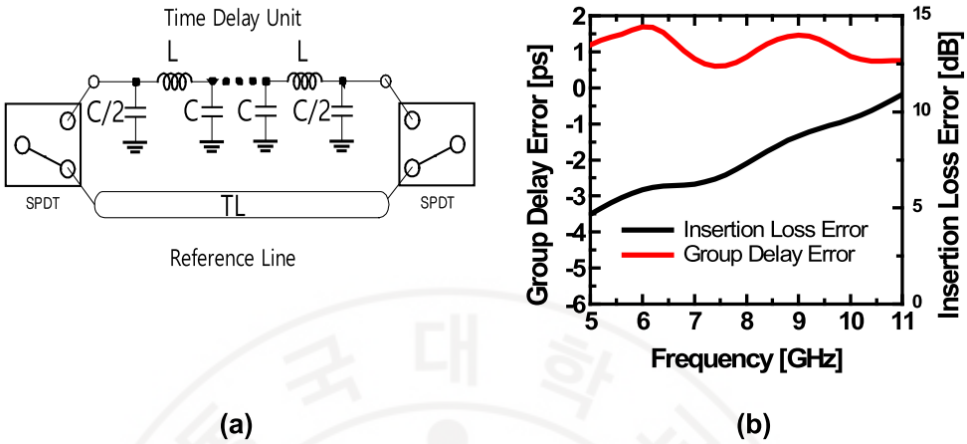


Figure 2.3 (a) Schematic diagram of the conventional delay element with cascaded multiple π −sections. (b) Group delay error and insertion loss error over frequency.

As shown in Figure 2.3, a common way to improve delay fidelity is to cascade multiple π sections while scaling down the passive values of each section. This increases the pole frequency of the unit delay element and reduces the group−delay error. However, the cascaded structure substantially increases both the insertion loss variation and the absolute loss difference between the delay and reference paths. Therefore, conventional LC−based passive TTDs exhibit a fundamental trade−off: the single π section structure offers compactness but poor delay fidelity, whereas the cascaded structure improves delay fidelity at the expense of larger loss and stronger loss imbalance. This limitation is also reflected in previously reported passive and active silicon−based TTDs [2.1]−[2.6].

2.3. Operating Principle of the Proposed Delay Cell

To reduce both group-delay error and insertion loss variation, the proposed precision delay cell employs π-type LC sections in both the delay path and the reference path. In the conventional structure, the delay path is realized using an artificial transmission line, whereas the reference path is implemented as a short real transmission line. Since the two paths exhibit substantially different frequency responses, the differential delay and insertion loss difference vary significantly with frequency.

In the proposed structure, by contrast, both paths are implemented using LC-based artificial transmission lines, and the required delay is obtained from the phase difference between the two paths. Since both branches exhibit similar frequency dependence, the common-mode variation is partially canceled, and the differential delay becomes more stable over the operating band.

The transfer function of the single π-type CLC network is expressed as

$$H(s) = \frac{R}{s^3 LC^2 R + s^2 LC + 2sRC + 1} \tag{2.6}$$

Accordingly, the phase response of the π-type network is written as

$$\angle H = \tan^{-1}\left(\frac{2\omega RC - \omega^3 LC^2 R}{1 - \omega^2 LC}\right) \tag{2.7}$$

If the upper branch is defined as the leading path and the lower branch as the lagging path, the differential phase becomes

$$\Delta\phi = \angle H_{leading} - \angle H_{lagging} \tag{2.8}$$

Thus, the differential delay is obtained as

$$\Delta\tau = \frac{\Delta\phi}{\omega} \tag{2.9}$$

These expressions show that the required delay is generated not by the absolute response of a single path, but by the relative phase difference between two LC-based paths. By properly selecting the passive values in the delay and reference branches, the differential delay variation can be significantly reduced over the operating band, as illustrated in Figure 2.4. The detailed circuit implementation of this fine-delay cell is shown in Figure 2.5, and the calculated delay curves in Figure 2.6 confirm that the proposed architecture is suitable for high-resolution delay control.

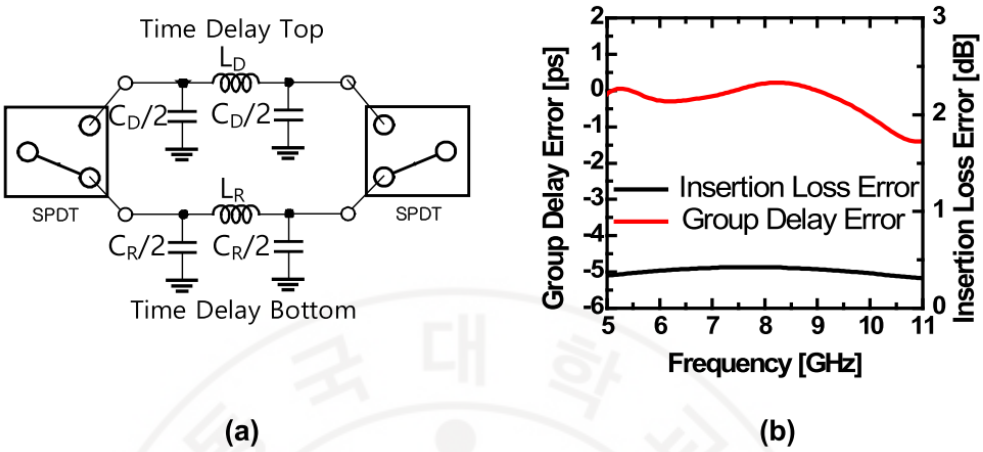


Figure 2.4 (a) Schematic diagram of the proposed delay element with the π −sections both at the delay and reference path. (b) Group delay error and insertion loss error over frequency.

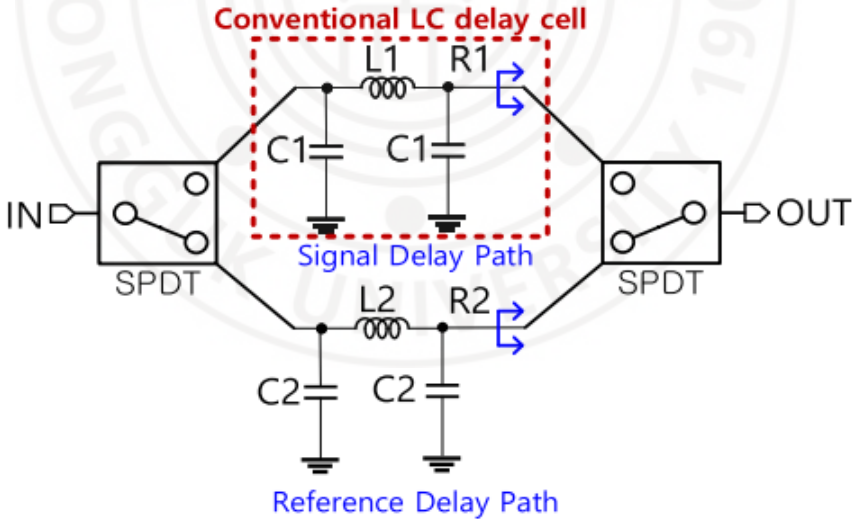


Figure 2.5 Schematic of the proposed precision time delay.

In Figure 2.5, the fine-delay core used for the lower bits of the proposed TTD generates delay from the relative phase difference between two closely related paths rather than from a single highly dispersive path, which is the main reason for the improved resolution and flatness.

The calculated delay response in Figure 2.6 verifies that the proposed fine-delay cell maintains a more stable relative delay over the operating band. In other words, the delay variation is suppressed even though the absolute responses of the two branches still vary with frequency.

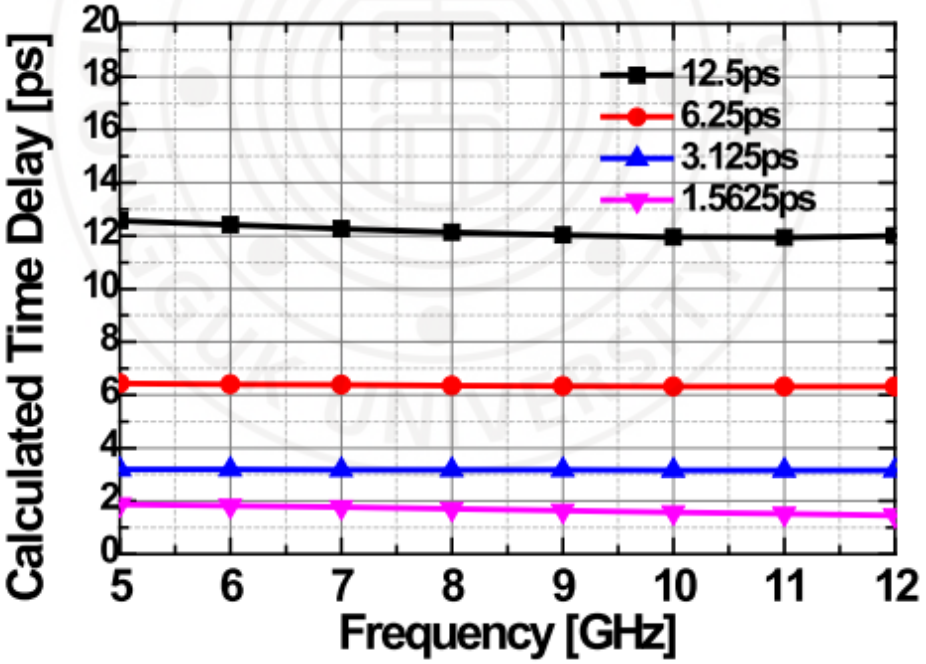
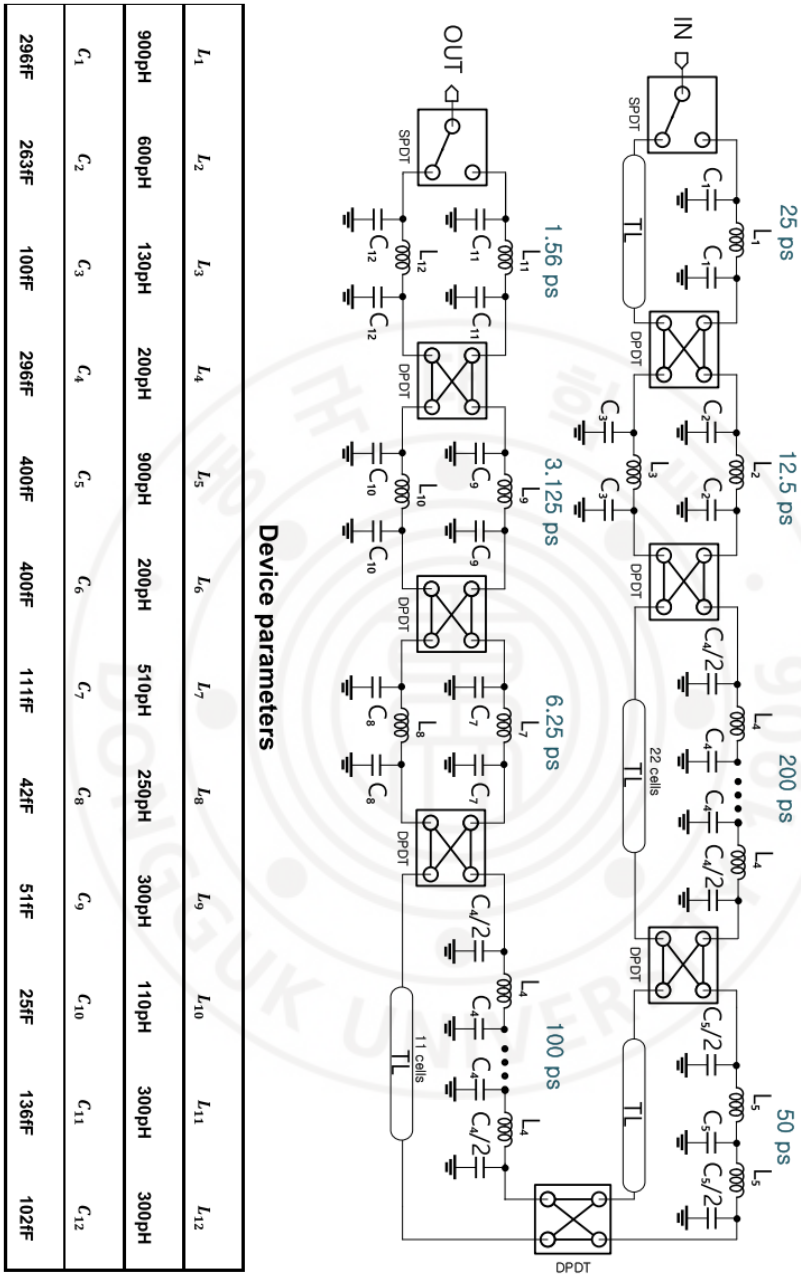


Figure 2.6 Calculated time delay over the operating frequency.

2.4. Circuit Design of the 8-Bit Passive True-Time Delay

The complete 8-bit TTD, shown in Figure 2.7, combines the proposed precision delay architecture for fine control and conventional LC-based delay cells for coarse control. The lower four bits correspond to delay cells of 1.56 ps, 3.13 ps, 6.25 ps, and 12.5 ps, all implemented using the proposed precision architecture. The upper four bits correspond to 25 ps, 50 ps, 100 ps, and 200 ps delay cells realized using conventional artificial transmission-line structures.



Device parameters

L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}
900pH	600pH	130pH	200pH	900pH	200pH	510pH	250pH	300pH	110pH	300pH	300pH
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
296fF	263fF	100fF	296fF	400fF	400fF	1111F	421F	511F	251F	136fF	102fF

Figure 2.7 Schematic of the proposed 8-bit true time delay (TTD) circuit.

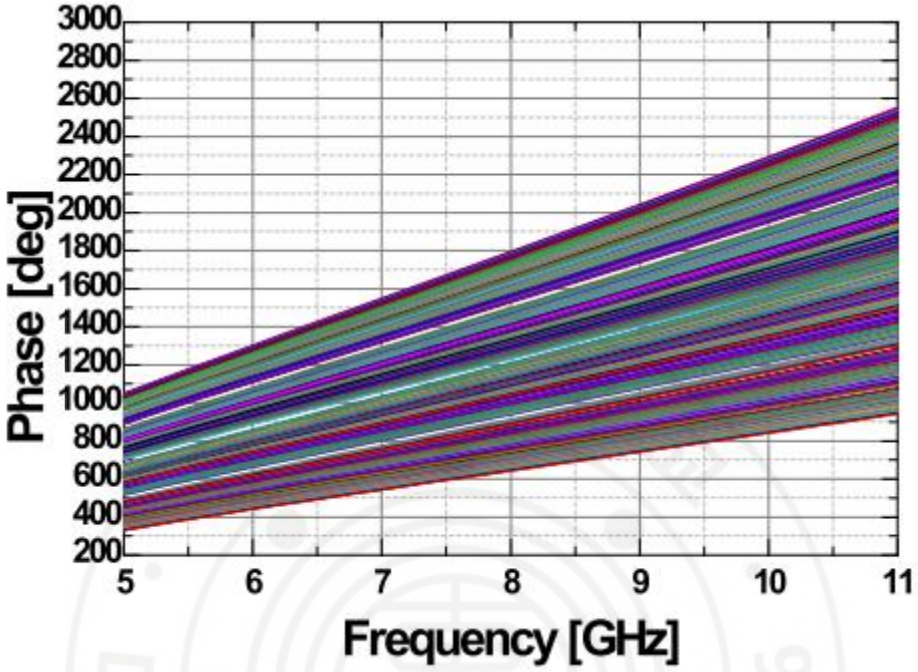


Figure 2.8 Simulated phase shift levels in all phase states.

The 25 ps delay cell employs a conventional π−type delay cell in the delay path together with a short transmission line in the reference path. The 50 ps delay cell is realized by cascading two 25 ps cells. For the 100 ps and 200 ps delay cells, multiple π−type LC networks are cascaded so that the self−resonance frequency of the required inductors remains sufficiently higher than the operating frequency. In addition, a characteristic impedance of 75 Ω is adopted to reduce insertion loss, and a 50–75–50 Ω matching network is applied to the reference line to minimize insertion loss variation and group−delay error. As shown in Figs. 2−8 and 2−9, through this partitioned

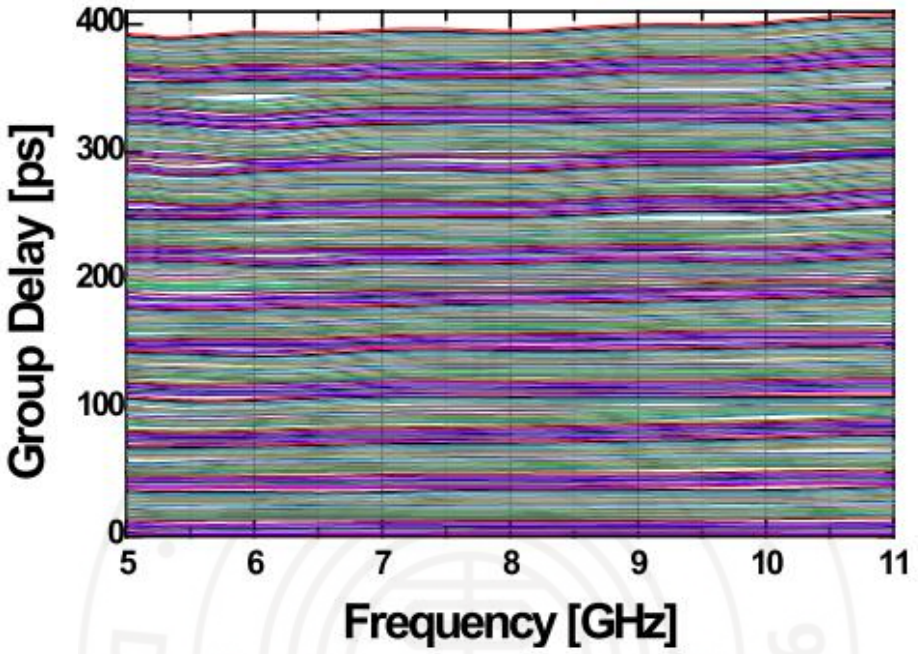
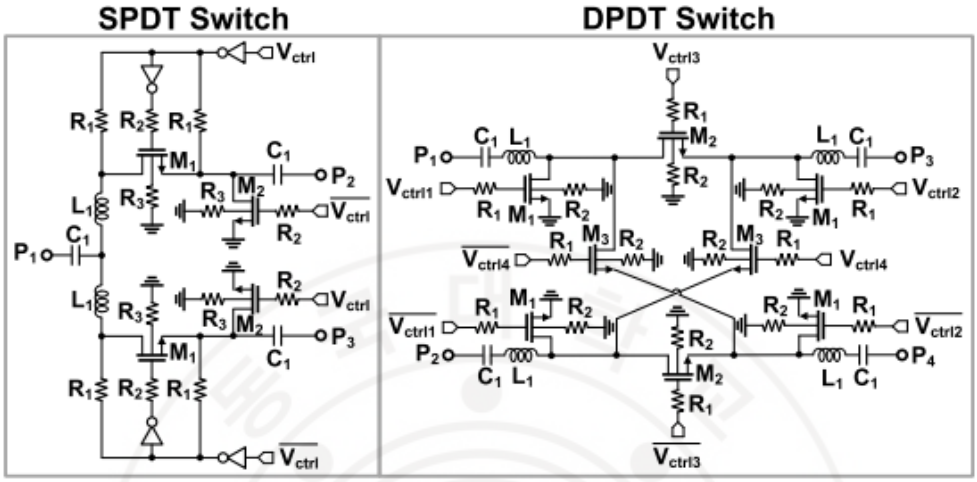


Figure 2.9 Simulated relative delay results in all time delay states.

architecture, the implemented TTD achieves a minimum delay step of 1.56 ps and a maximum delay of 400 ps, corresponding to an equivalent phase range of 1440◦ at 10 GHz in 5.625◦ steps.

As shown in Figs. 2−8 and 2−9, the simulated phase responses of all digital states increase linearly with frequency, which is consistent with the expected operation of a true−time−delay element. The simulated relative delay states likewise confirm that the 256 digital states cover the intended delay range with fine resolution.

2.4.1 Design Considerations for the Switching Network



Device parameters

M_1	M_2	L_1
130 μm(W) / 60 nm(L)	20 μm(W) / 60 nm(L)	610 pH

C_1	R_1	R_2	R_3
3.2 pF	20 kΩ	14 kΩ	11 kΩ

Device parameters

M_1	M_2	M_3
20 μm(W) / 60 nm(L)	130 μm(W) / 60 nm(L)	156 μm(W) / 60 nm(L)

L_1	C_1	R_1	R_2
510 pH	3.2 pF	14 kΩ	11 kΩ

Figure 2.10 Schematic and all device parameters of the SPDT (left) and DPDT (right) switches.

A passive TTD requires an efficient switching network because the routing mechanism directly contributes to insertion loss, path isolation, and state-to-state consistency. In the present design, two SPDT switches and seven DPDT switches are used to configure the desired signal path through the delay cells. The switch topology follows the low-loss switching concept used in previously reported TTD-related switching structures [2.14].

In the SPDT structure, the series transistor performs the primary switching function, while the shunt transistors improve isolation between alternative paths. The DPDT switch follows the same principle. A large gate resistor RG is used to stabilize the transistor bias condition against RF voltage swings at the source and drain nodes. This resistor helps maintain a nearly constant on-resistance and prevents excessive voltage stress across the gate oxide. The switch schematics and device parameters are shown in the implemented design.

Since each delay state is formed through a distinct routing combination, excessive switch loss or imbalance would directly degrade delay-state uniformity and insertion loss flatness. The switching network is therefore an essential part of the overall TTD architecture.

2.4.2 Fabrication and Measurement Setup

The proposed 8-bit precision passive TTD was fabricated in a 65-nm CMOS process. The chip occupies 2.76 × 1.01 mm^2 including RF and DC pads, and a 64-bit SPI scan chain was integrated on-chip for digital control of all delay states.

The fabricated chip was characterized using on-chip probing and a Keysight N5224A network analyzer. The measurement setup was used to obtain the S-parameters, phase responses, and group delays of the fabricated chip over the 5–11 GHz operating band.



Figure 2.11 Chip-photograph of the fabricated 5-11 GHz 8-bit true-time delay (TTD) in 65-nm CMOS technology.

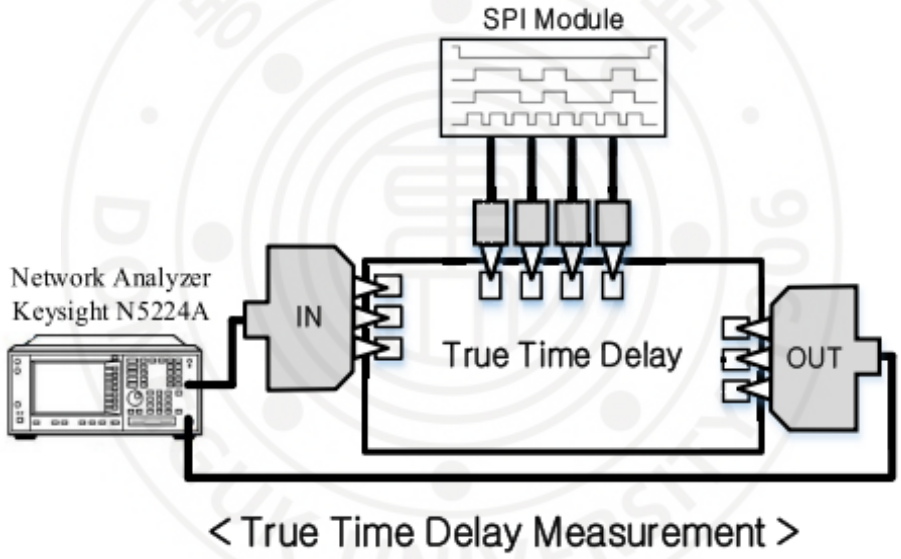


Figure 2.12 The measurement setup for the S-parameters, phase shift, and time delay over the frequency.

Because the circuit is fully passive, the measured responses directly reflect the behavior of the delay cells and switching network without the complication of active bias currents.

2.4.3 Measured Results and Discussion

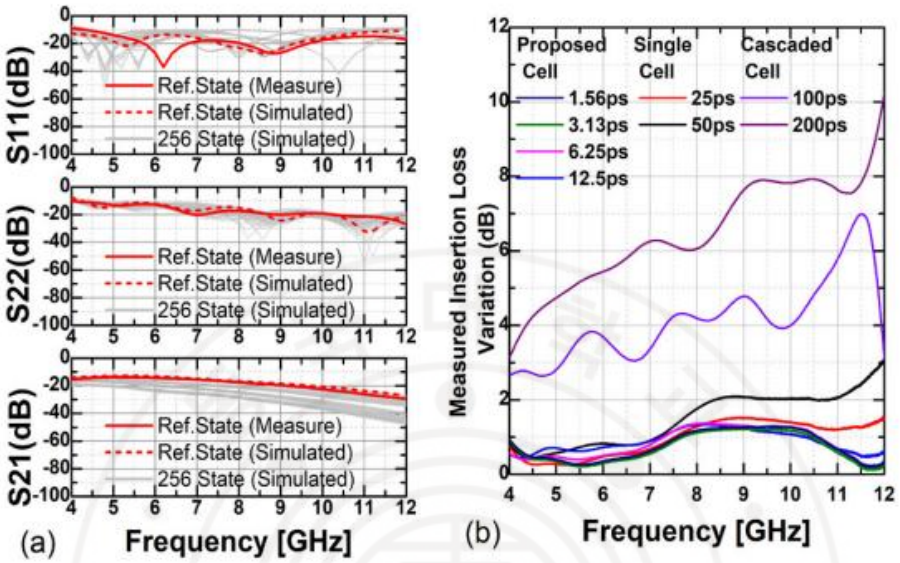


Figure 2.13 Simulated and measured results for the (a) S11, S22, and S21 and (b) the insertion loss variation of the true-time delay circuit based on 256 different group-delay states.

The measured S-parameters show that both the input and output return losses are better than 10 dB over the 5-11 GHz operating band. This confirms that the delay network and switching structure together maintain adequate matching over frequency. The measured insertion loss variation across all 256 delay states is also greatly reduced. Compared with the conventional structure, the relative

insertion loss variation is reduced from 8 dB to 1 dB over the operating band. This reduction becomes more pronounced at higher frequencies.

The large-signal performance was measured at the largest delay state and 8 GHz. The measured input 1-dB compression point is 11.2 dBm, indicating that the passive TTD can handle realistic RF input levels without severe nonlinear degradation.

The measured phase responses of the main delay states agree well with the simulated results. Within a 360° phase-shifting range using the first 6-bit controls, the RMS phase error remains below 5.2°. In addition, the measured group delays of representative states show that the phase of each state increases linearly with

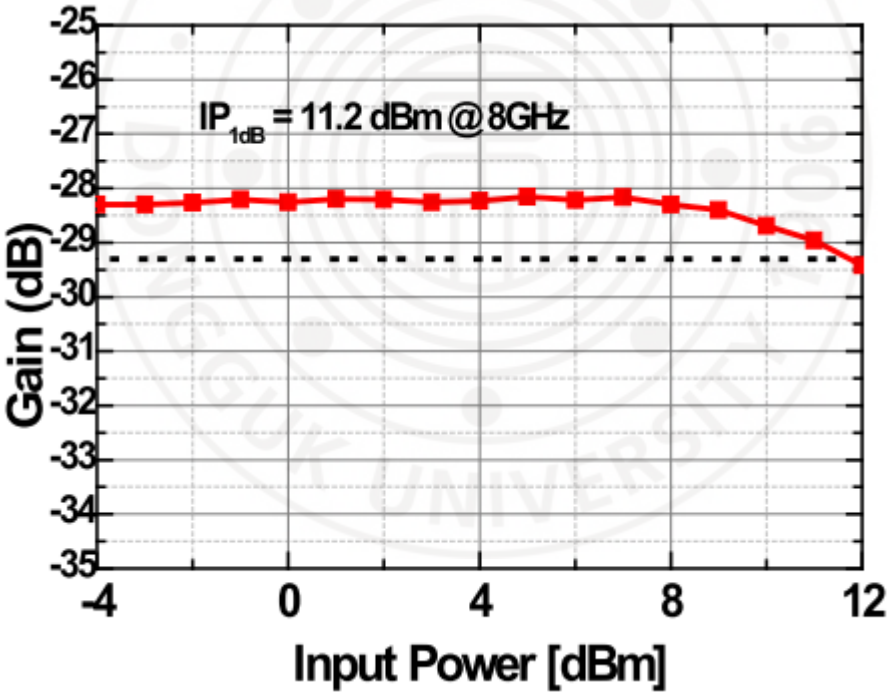


Figure 2.14 Measurement gain compression curve with the largest delay state at 8 GHz.

frequency, as expected from a true-time-delay element. The RMS delay error is less than 4.5 ps over the operating band, while the delay range extends up to 400 ps. The difference between simulation and measurement is approximately 2%.

Taken together, these results demonstrate that the proposed passive TTD achieves a practical combination of wide bandwidth, large delay span, fine resolution, reduced insertion loss variation, and adequate linearity.

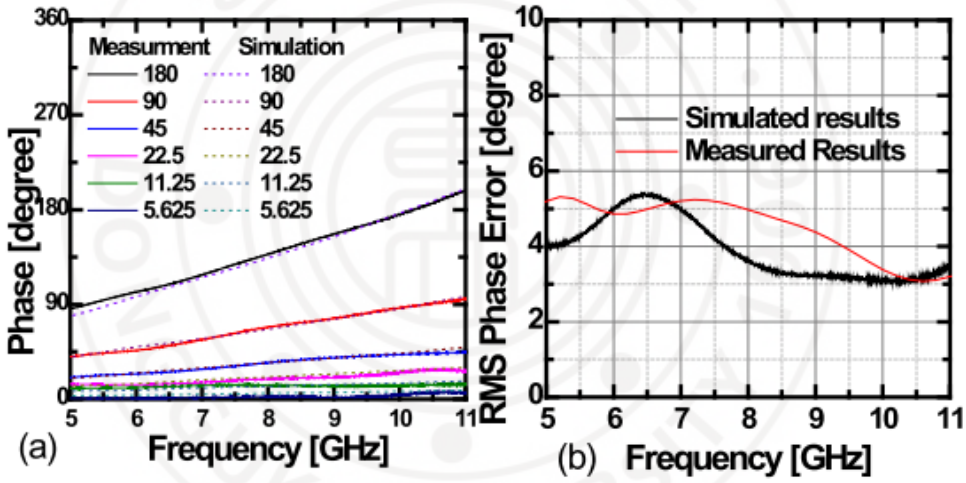


Figure 2.15 Simulated and measured results of the (a) phase for the main phase states and (b) the RMS phase error over the frequency.

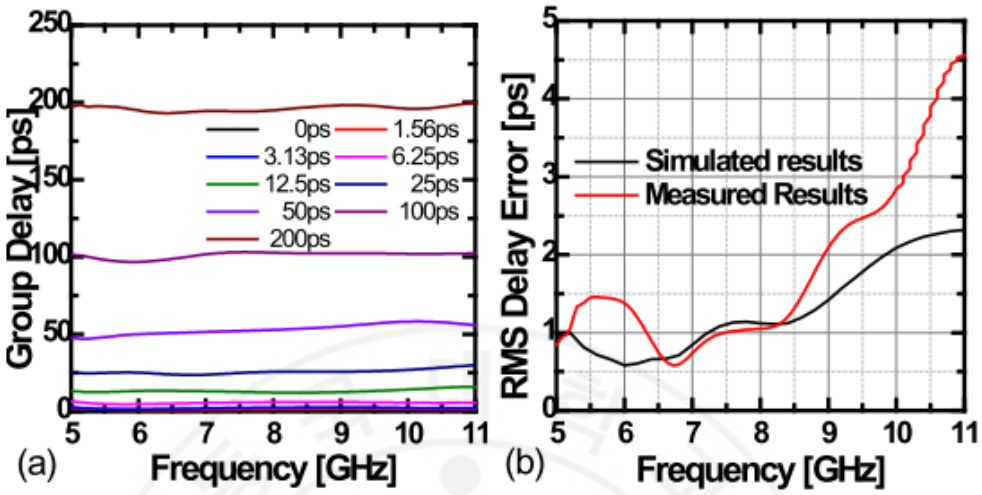


Figure 2.16 (a) Measured group delay of the main delay states, and (b) Simulated and measured results of the RMS group delay error over frequency.

2.5. Performance Comparison with Previously Reported True-Time Delay Circuits

The performance of the implemented TTD is compared with previously reported silicon-based TTD circuits, as summarized in Table 2.1. The comparison includes operating frequency, maximum delay, resolution, maximum loss, loss per delay, delay density, linearity, DC power, and chip area. The present work achieves a maximum delay of 400 ps, a resolution of approximately 1.54 ps, an IP1dB of 11.2 dBm, zero DC power consumption, and a loss per delay of 0.103 dB/ps. Most importantly, this loss-per-delay value is the smallest among the compared silicon-based TTD implementations [2.1]-[2.6], [2.13].

This comparison indicates that the proposed architecture achieves a well-balanced combination of wide delay range, fine resolution, passive operation, and low loss variation, which is particularly beneficial for broadband phased-array frontends.

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Table 2.1 Comparison with previously reported True-Time-Delay circuits.

Ref.	This work	[2.1]	[2.2]	[2.3]	[2.4]	[2.5]	[2.6]	[2.7]
Maximum Delay	400	35.2	400	32.8	42	12.5	106	68.5
f_{RF} [GHz]	5-11	20-30	1-20	10-50	15-40	20-40	5-20	3-30
Chip area [mm^2]	2.91 2.46(Core)	0.18(Core)	4	0.22(Core)	0.99	0.1(Core)	0.88	0.34(Core)
Resolution	1.54ps	0.56ps	5ps	cont	5.2ps	cont	3.3ps	4.9ps
Delay Steps	8-bit	6-bit	10 state (trombone) 3bit (switched)	6-bit + Analog	3-bit	3-bit + Analog	5-bit	4-bit
DC power [mW]	passive	passive	2.6-6	passive	8.6-24.6	33	passive	passive
Maximum Loss[dB]	41	12.3	45	25	14	-	38	13.5
Tech	65nm CMOS	65nm CMOS	130nm CMOS	250nm SiGe	130nm CMOS	250nm SiGe	180nm CMOS	28nm CMOS
Structure	TTD (artificial T-lines in parallel)	TTD (conventional)	TTD (with trombone)	TTD (with varactor lc)	TTD (with trombone)	TTD (with varactor lc,Gm-RC)	TTD (conventional)	TTD (conventional)
Delay/size [ps/ mm^2]	137 163(Core)	196(Core)	100	149(Core)	42	125(Core)	120	201(Core)
Loss/Delay [dB/ps]	0.103	0.35	0.113	0.76	0.33	-	0.36	0.2

2.6. Conclusion

In this chapter, a 5–11 GHz 8–bit precision passive true–time delay implemented in 65–nm CMOS technology has been presented. The proposed design uses a precision fine–delay architecture based on two LC delay networks in parallel for the lower four bits, while conventional LC–based delay cells are used for the upper four bits to realize coarse delay control. Through this hierarchical structure, the implemented circuit achieves a minimum delay step of 1.56 ps and a maximum delay range of 400 ps without any DC power dissipation.

The measured results show better than 10 dB input and output return losses over 5–11 GHz, a reduction of insertion loss variation from 8 dB to 1 dB compared with the conventional structure, an IP1dB of 11.2 dBm at 8 GHz, an RMS phase error below 5.2◦, and an RMS delay error below 4.5 ps. Compared with previously reported silicon–based TTD circuits, the proposed design achieves the smallest loss per delay while maintaining competitive overall performance.

Accordingly, the proposed passive TTD is not merely a compact delay element, but a practically meaningful wideband signal–alignment block for broadband phased–array frontends.

The results of this chapter have been published to IEEE Access and are detailed in [2.15].

2.7. References

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Chapter 3. An X-Band Multifunction Chip

3.1. Introduction

The increasing demand for active phased-array antennas (APAAs) has historically driven the widespread use of III-V MMIC based transmit/receive modules (TRMs) in active antenna arrays. At the same time, recent system requirements for miniaturization, lower cost, and reduced power consumption have accelerated the development of silicon-based multifunction chips (MFCs) using both SiGe BiCMOS and CMOS technologies [3.1]-[3.10]. Among these options, CMOS offers a more cost-effective platform, although the achievable output power and receive noise figure are limited by the relatively low supply voltage and inferior device performance compared with III-V processes.

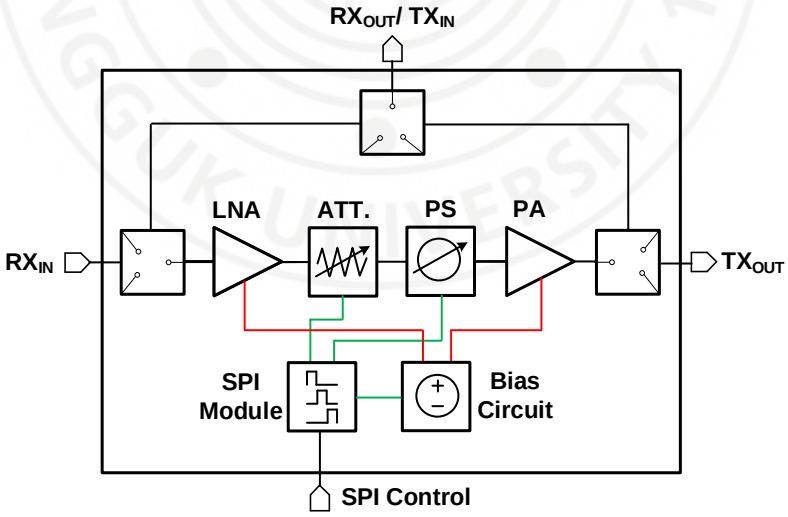


Figure 3.1 Proposed MFC structure.

Various types of phase shifters have been reported for microwave MFCs. Vector-modulator-based phase shifters can provide agile phase controllability and relatively high gain in a compact die area [3.11], [3.12], but they require DC power for the variable-gain amplifiers and substantial calibration overhead, including DAC/ADC assistance, offset cancellation, and temperature compensation circuits [3.13], [3.14]. Reflection-type phase shifters avoid DC power dissipation, but their narrow bandwidth, large insertion loss, strong load sensitivity, and limited phase-shift range hinder their application in robust X-band MFC design. By contrast, filter-based passive phase shifters are attractive because of their robustness to process, voltage, and temperature variation, stable phase control, and ease of integration with attenuators, mixers, and amplifiers [3.15], [3.16]. However, once multiple filter-based phase-shifter cells are cascaded, impedance mismatch between cells induces cumulative phase distortion, particularly in lower-bit cells.

To address this problem, this chapter presents a packaged X-band multifunction chip implemented in a 65-nm CMOS process. The proposed MFC employs a 6-bit hybrid passive phase shifter in which the lower bits are realized using TTD cells and the higher bits are implemented using filter-based phase-shift cells. The complete chip also integrates a 6-bit attenuator, SPDT/DPDT switching networks, LNA, PA, SPI control, and bias circuitry, while maintaining the same

RF signal path in both transmit and receive modes. The architecture is shown in Figure 3.1.

The proposed MFC achieves an RMS phase error below 3.3◦ and an RMS attenuation error below 0.31 dB in the 8–10 GHz range. After QFN packaging, the measured RMS phase error remains 3.5◦ with gain error maintained below 0.39 dB, indicating only minimal degradation due to packaging. The packaged MFC also achieves an output power of 8.8 dBm at 1−dB compression, Tx/Rx gain of 12.9/12.3 dB, a 3dB bandwidth of 3.54 GHz, and a receive noise figure below 16.2 dB across the X−band. With a bare chip size of 3 × 1.3 mm^2 , the chip draws 80 mA from a 1 V supply in normal operation and consumes 18 mW in a low−power mode.

3.2. Hybrid Phase Shifter Design

3.2.1 Analysis of mismatch effects on phase error

A phase shifter is a key element in active phased−array systems because it determines the steering accuracy of the synthesized radiation pattern. In addition to a sufficiently wide phase range and fine resolution, a practical phase shifter must maintain low phase error, low insertion loss, sufficient bandwidth, high linearity, and low power consumption. Among passive implementations, filter−type phase shifters and true−time−delay (TTD) networks are representative low−power solutions because both realize the

required phase shift through the phase difference between a reference path and a delay path.

For a general two-port network, the transducer gain is expressed as

$$G_T = \frac{|S_{21}|^2 (1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_S\Gamma_L|^2} = \frac{4\,\mathrm{Re}(Z_S)\,\mathrm{Re}(Z_L)}{|Z_S+Z_0|^2\,|Z_L+Z_0|^2} \tag{3.1}$$

where Z_S and Z_L are the source and load impedances, respectively, and Z_0 is the characteristic impedance of the network. From (3.1), the complex transfer function of a two-port network is written as

$$|T|^2 = G_T,\ \ T(\omega) = |T(\omega)|e^{j\phi_T(\omega)} \tag{3.2}$$

and the phase is expressed in closed form as

$$\phi = \angle S_{21}(\omega) + \angle[1-\Gamma_S(\omega)\Gamma_{in}(\omega)] - \angle[1-S_{22}(\omega)\Gamma_L(\omega)] \tag{3.3}$$

Under ideal 50 Ω matching ($\Gamma_S=\Gamma_L=0$), all reflection-induced phase terms vanish and the phase difference between two networks reduces to

$$\Delta\phi_{ideal}(\omega) = \angle S_{21,b}(\omega) - \angle S_{21,a}(\omega) \tag{3.4}$$

Equations (3.1)-(3.4) show that mismatch directly perturbs the realized phase through reflection-related terms, even if the intended network phase response is correct.

Filter-type phase shifters typically realize the desired phase difference using a high-pass path and a low-pass path. For an ideal filter-type phase shifter referenced to a characteristic impedance Z_0 and center angular frequency ω_c, the reactive element values of the T-type HPF and the π-type LPF are expressed as

$$L_H = \frac{Z_0}{\omega_c \sin(\phi_H)},\ C_H = \frac{1}{\omega_c Z_0 \tan\left(\frac{\phi_H}{2}\right)}$$
$$L_L = -\frac{Z_0 \sin(\phi_L)}{\omega_c},\ C_L = -\frac{\tan\left(\frac{\phi_L}{2}\right)}{\omega_c Z_0} \quad (3.5)$$

Although these equations realize the desired phase difference at the center frequency, each LC filter is accurately matched to 50 Ω only around a single operating point. Therefore, when many HPF/LPF cells are cascaded, mismatch-induced phase distortion accumulates through inter-cell reflections. As shown in Figure 3.2, even when the reflection coefficients of the unit cells are constrained within typical limits, the accumulated phase error increases rapidly with the number of cascaded filter-type phase-shifter cells, and a 6-bit structure can exhibit phase error larger than 40◦.

By contrast, a TTD cell realizes phase shift through the group delay of matched transmission lines. Its ideal phase response is given by

$$\phi_{TTD}(\omega) = -\omega\tau \tag{3.6}$$

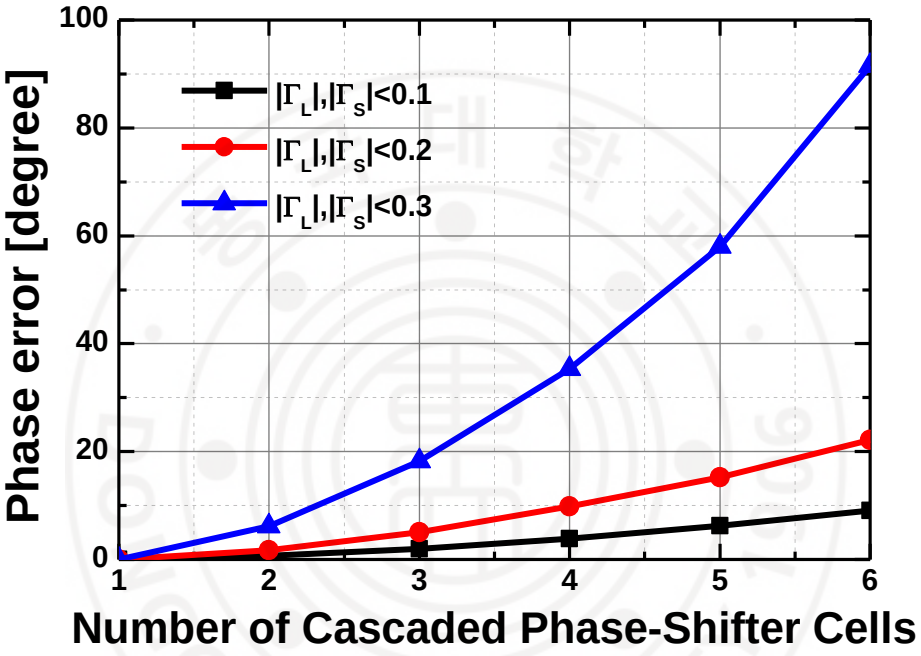


Figure 3.2 Accumulated Phase Error versus Number of Cells under $|\Gamma|$ Mismatch.

where τ is the group delay of the line. Since both the reference and delay paths of a TTD cell maintain the same characteristic impedance Z_0, the reflection coefficient between the n^{th} and $(n+1)^{th}$ cells becomes

$$\Gamma_{n\to n+1}=\frac{Z_{0,n}-Z_{0,n+1}}{Z_{0,n}+Z_{0,n+1}}=\frac{Z_{0,n}-Z_{0,n}}{Z_{0,n}+Z_{0,n}}=0 \tag{3.7}$$

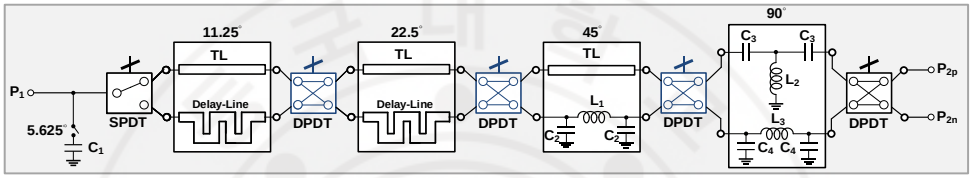
Accordingly, cascading identical TTD cells preserves impedance continuity and suppresses multiple-reflection-induced phase distortion. This structural uniformity makes TTD especially suitable for lower-bit phase-shifter stages, where fine phase resolution is required and mismatch-induced phase error is most severe in filter-based implementations.

3.2.2 Design of the hybrid phase shifter

Based on the above analysis, the proposed phase shifter adopts a hybrid architecture that combines filter-based phase-shift cells and TTD cells. The 6-bit hybrid phase shifter is shown in Figure 3.3. In the proposed allocation, the 5.625° cell uses a parallel-capacitor structure to reduce insertion loss caused by the switching network. The 11.25° and 22.5° cells use transmission-line-based TTD structures because TTD ensures minimal frequency-dependent phase error at relatively small phase-shift angles and provides excellent phase accuracy.

For the 45° cell, a pure TTD would result in excessive frequency-dependent phase variation and large chip area. To mitigate this, an LC-based pseudo-TTD structure is adopted and designed with a group-delay slope opposite to that of the TTD cells, thereby compensating for cumulative phase error across the operating

frequency band. For the 90◦ cell, both TTD and pseudo−TTD structures are impractical because of substantial cumulative phase error and area overhead. Since the mismatch effect is not significant when a 90◦ unit cell is used alone, a standalone filter−type phase shifter is adopted for this stage. This hybrid approach simultaneously suppresses cumulative phase error and minimizes chip area.



C_1	C_2	L_1	C_3	L_2	C_4	L_3
140 fF	145 fF	200 pH	180 fF	725 pH	130 fF	650 pH

Figure 3.3 Block diagram of 6−bit hybrid phase shifter.

3.2.3 DPDT-based tuning mechanism

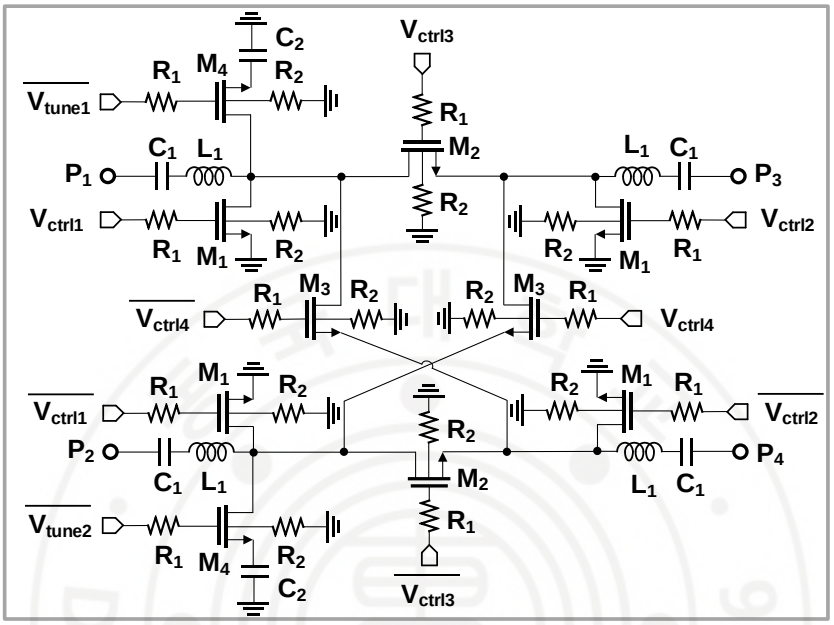


Figure 3.4 Modified structure of the DPDT switch.

A double-pole double-throw (DPDT) switching network augmented with parallel capacitors at both ports provides additional phase error tuning in the hybrid phase shifter. This DPDT structure is an improved version of the switching network employed in Chapter 2. In the previous design, blocking capacitors were required in the signal path, which introduced additional insertion loss and limited the phase-shifter efficiency. In the proposed DPDT, the LC matching network is re-optimized so that the blocking capacitors can be removed while maintaining the required impedance condition. As a result, the signal path is simplified and the insertion loss is reduced.

These parallel capacitors compensate for the inherent frequency-dependent phase error of the TTD cells at the center frequency and improve phase flatness across the operating band. The modified DPDT structure is shown in Figure 3.4, and the tuning mechanism is shown in Figure 3.5. By adjusting the capacitance at both ends of the DPDT switch, the phase response can be fine-tuned to compensate for minor deviations caused by manufacturing variation and parasitic effects.

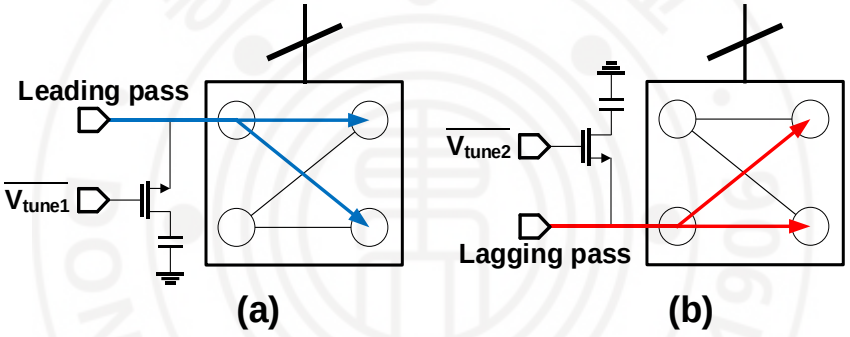


Figure 3.5 Tuning mechanism of the proposed DPDT: (a) leading tune and (b) lagging tune.

3.3. Multifunction Chip Design

3.3.1 Attenuator Design

The attenuator is designed to provide a 0–31.5 dB range in 0.5 dB steps, as shown in Figure 3.6, and employs a resistive π-type network to guarantee accurate impedance matching. In the proposed MFC, a conventional series-connected layout is adopted to minimize chip

area. Because the LNA output stage uses a transformer, its impedance exhibits pronounced frequency dependence; therefore, inserting the attenuator directly between the LNA and the phase shifter improves impedance matching at both interfaces and mitigates phase distortion in the phase-shifter block. Each 8 dB cell includes an additional capacitor to suppress the phase error introduced by signal attenuation, and the 16 dB step is realized by cascading two 8 dB cells. The simplified cell schematics are shown in Figure 3.7.

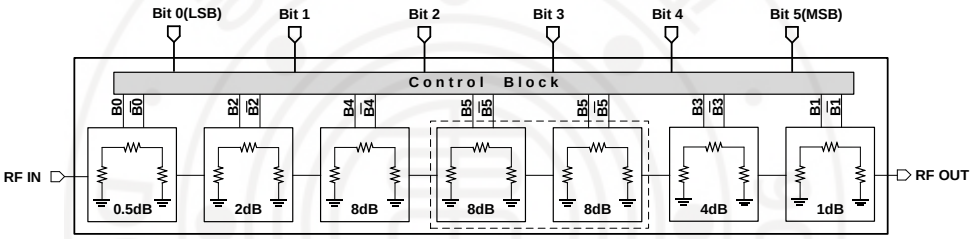
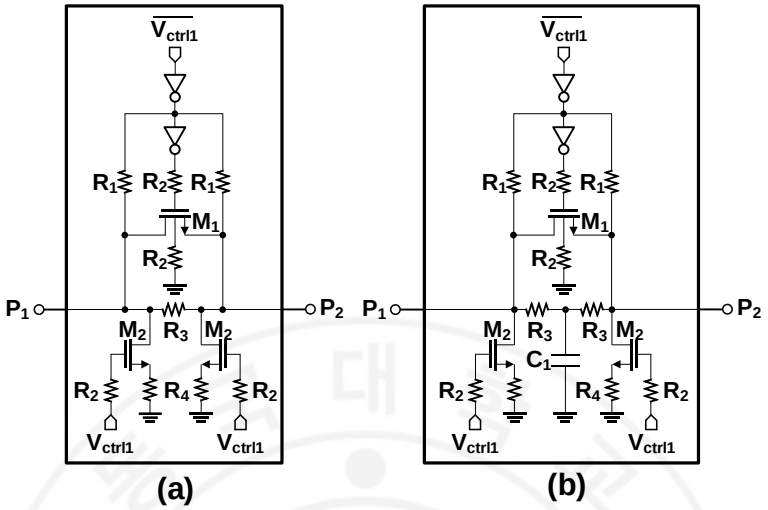


Figure 3.6 Block diagram of the 6-bit attenuator.



Device parameters

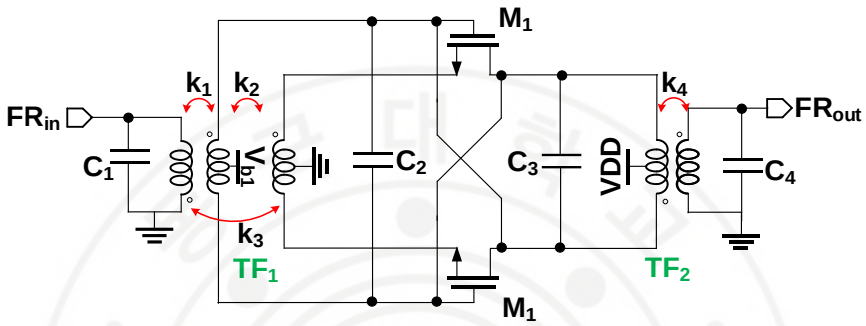
	M_1	M_2	R_1	R_2	R_3	R_4	C_1
0.5dB	40 µm(W) / 60 nm(L)	20 µm(W) / 60 nm(L)	20.2 kΩ	13 kΩ	5 Ω	11 kΩ	-
1dB	40 µm(W) / 60 nm(L)	20 µm(W) / 60 nm(L)	20.2 kΩ	13 kΩ	14 Ω	11 kΩ	-
2dB	40 µm(W) / 60 nm(L)	20 µm(W) / 60 nm(L)	20.2 kΩ	13 kΩ	22 Ω	11 kΩ	-
4dB	40 µm(W) / 60 nm(L)	20 µm(W) / 60 nm(L)	20.2 kΩ	13 kΩ	45.6 Ω	11 kΩ	-
8dB	40 µm(W) / 60 nm(L)	20 µm(W) / 60 nm(L)	20.2 kΩ	13 kΩ	46 Ω	11 kΩ	114 fF

Figure 3.7 Simplified cell schematics of the attenuator.

3.3.2 Low-noise amplifier design

The LNA employs a magnetic-coupled source-degeneration structure to optimize linearity and noise figure while simultaneously improving the input impedance of the RF signal-modulation stage [3.18]. To minimize the size of the transformer-based amplifier, a tertiary-coil configuration is adopted. The simplified schematic is shown in Figure 3.8, and the 3D structure of the transformer is shown

in Figure 3.9. The primary coil, formed on the top−metal layer, serves as the input stage; the secondary coil, fabricated on Metal−8, is connected to the gates of the differential amplifier; and the tertiary coil is tied to the amplifier source to provide source degeneration.



Device parameters

M_1	C_1	C_2	C_3	C_4	k_1	k_2
80 µm(W) / 60 nm(L)	150 fF	500 fF	200 fF	100 fF	0.78	0.65
TF_1 L_p	TF_1 L_s	TF_1 L_t	TF_2 L_p	TF_2 L_s	k_3	k_4
1.43 nH	435 pH	425 pH	1.19nH	347pH	0.83	0.82

Figure 3.8 Simplified schematic of the LNA.

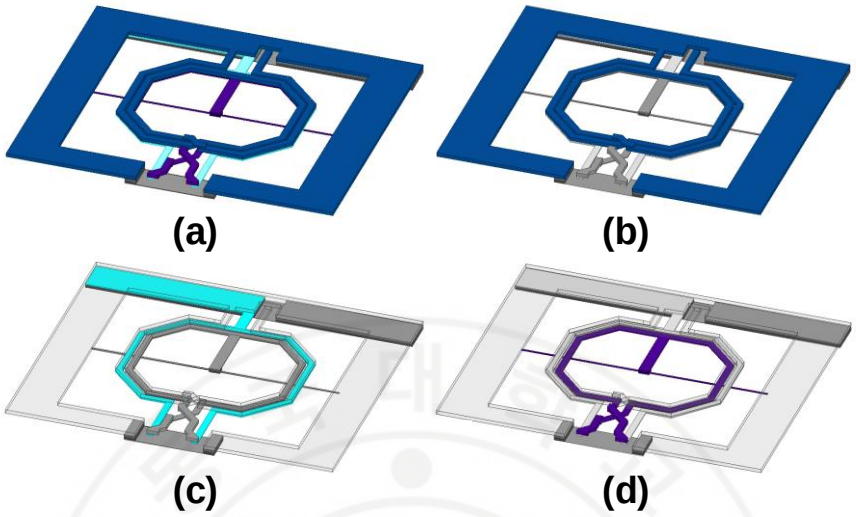
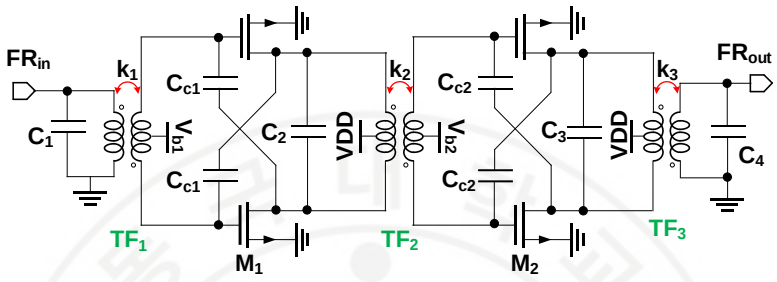


Figure 3.9 3D structure of the proposed transformer for the LNA: (a) full structure, (b) primary coil, (c) secondary coil, and (d) tertiary coil.

3.3.3 Power amplifier design

The PA, shown in Figure 3.10, is implemented in a fully differential architecture to suppress ground related parasitic distortion and improve common mode rejection. To reduce chip area, the conventional LC matching network and discrete balun are replaced by a single transformer that inherently provides a 180◦ phase inversion, while a two stage topology compensates for the insertion loss of the preceding phase shifter and delivers the required output power. In the first stage, the transformer is cross−connected through a DPDT switch, reversing the primary−winding current to realize both single to differential balun functionality and a 180◦ phase shift within one device, as shown in Figure 3.11. Because the

transformer’ s equivalent impedance and coupling coefficient remain invariant across switch states, the proposed structure suppresses phase error growth associated with input/output impedance variation.



Device parameters

M_1	M_2	C_{c1}	C_{c2}	C_1	C_2
240 µm(W) 60 nm(L)	512 µm(W) 60 nm(L)	113 fF	168 fF	200 fF	150 fF
C_3	C_4	TF_1 L_P	TF_1 L_S	TF_2 L_P	TF_2 L_S
400 fF	50 fF	252 pH	746 pH	707 pH	245 pH
TF_3 L_P	TF_3L_S	k_1	k_2	k_3	
303 pH	791 pH	0.71	0.62	0.66	

Figure 3.10 Simplified schematic of the PA.

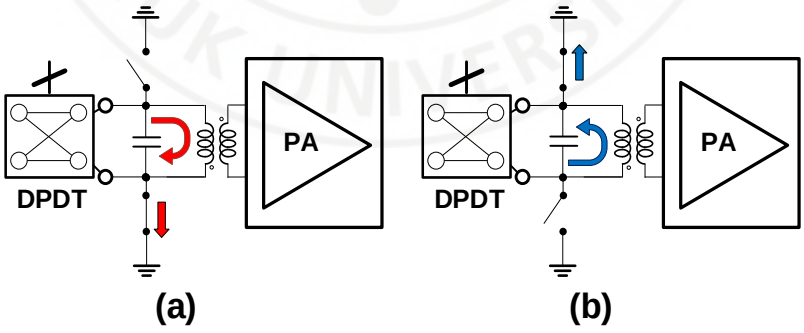


Figure 3.11 180◦ switching mechanism of the proposed PA.

3.4. Chip Implementation and COB Measurement Results

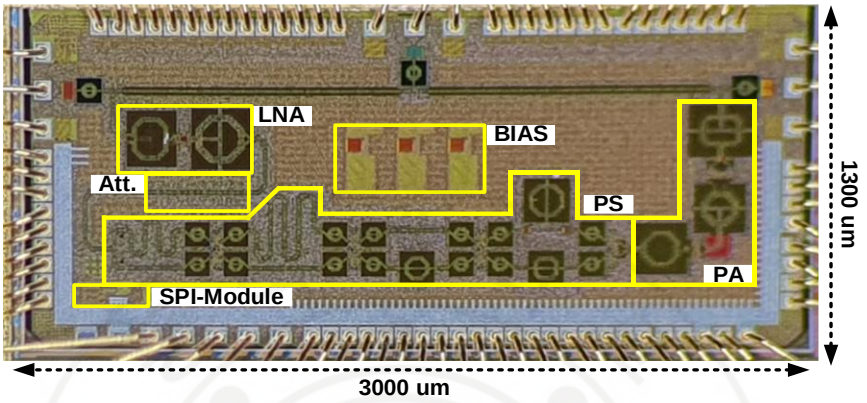


Figure 3.12 Die chip photo of fabricated MFC.

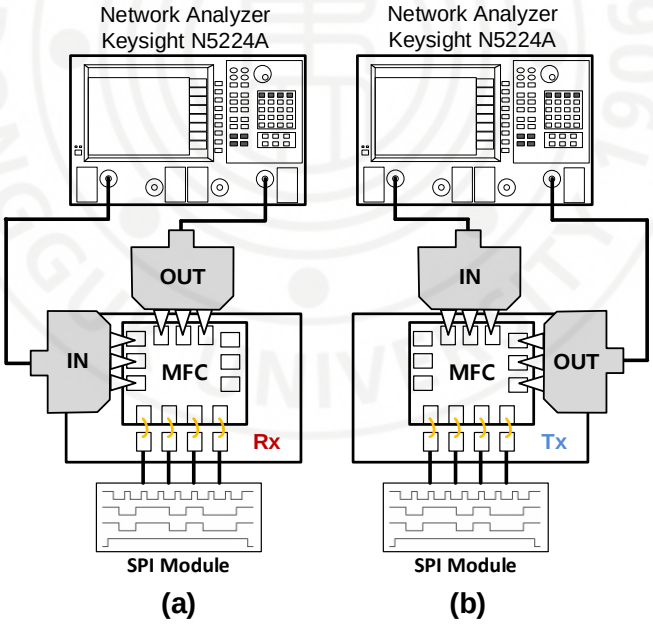


Figure 3.13 Measurement setup of the MFC: (a) Tx and (b) Rx.

The designed X-band MFC was fabricated using a 65-nm CMOS process. The die photograph in Figure 3.12 shows that the fabricated chip size, including RF/DC pads and ESD protection, is $3 \times 1.3\ mm^2$. The chip was characterized using on-chip probing with a Keysight N5224A network analyzer, and a 26-bit SPI scan chain was integrated for digital control of each unit. The measurement setup is shown in Figure 3.13 The measured S-parameter results in the reference state are shown in Figure 3.14. In the proposed MFC topology, the small-signal gain is identical for both transmit and receive paths, and the measured gain difference between the two paths remains within 0.1 dB. At the center frequency of 9 GHz, the small signal gain in Tx mode is 14.1 dB, and the 3dB bandwidth is 2.84 GHz. Across all phase and attenuation states, the input and output reflection coefficients remain below -10 dB, as shown in Figure 3.15.

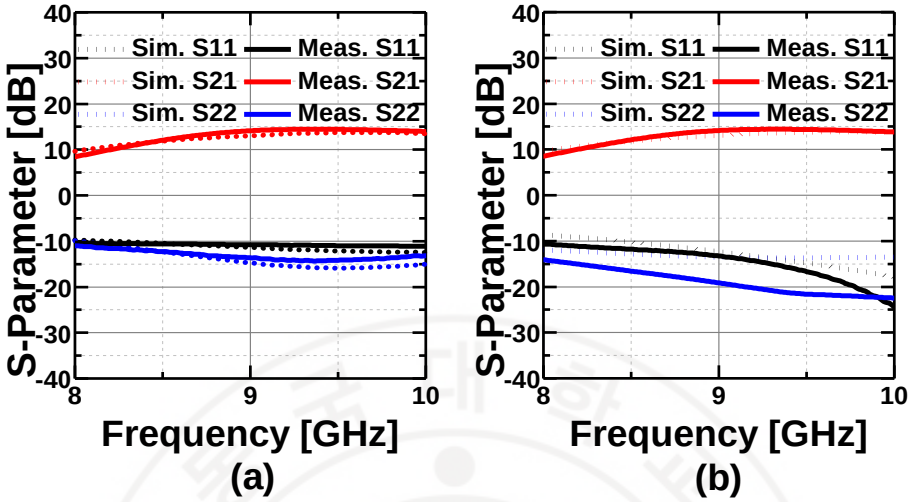


Figure 3.14 Measured S-parameter results of the MFC: (a) Tx and (b) Rx.

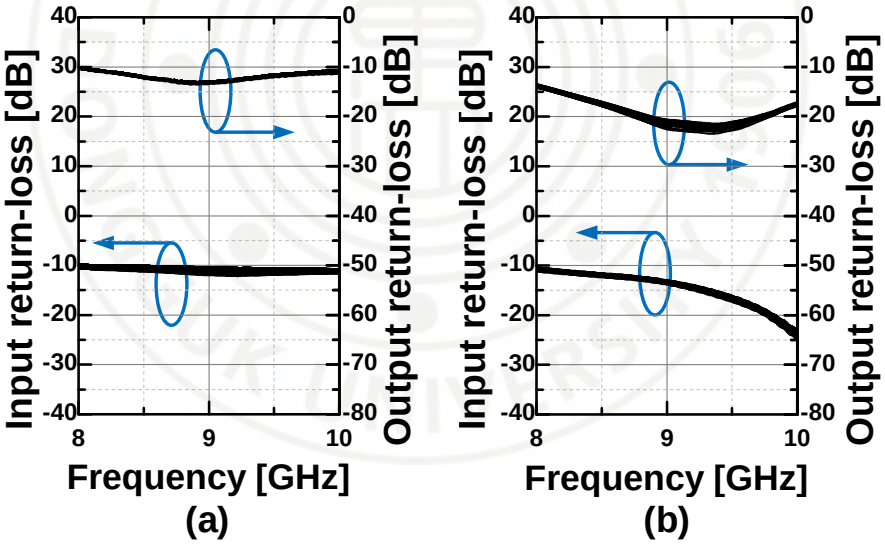


Figure 3.15 Input and output return loss over all phase and attenuation states: (a) Tx and (b) Rx.

The measured phase characteristics over all phase states are shown in Figure 3.16. In the 8–10 GHz range, the RMS phase error is within 5.57◦, and the RMS gain error is within 0.97 dB before tuning. After applying the designed tuning bits, the RMS phase error is reduced to 3.33◦, while the RMS gain error remains within 1.11 dB. The attenuation state results in Figure 3.17 show that the RMS gain error across all attenuation states is within 0.31 dB, while the attenuation–state phase variation remains within 3.2◦.

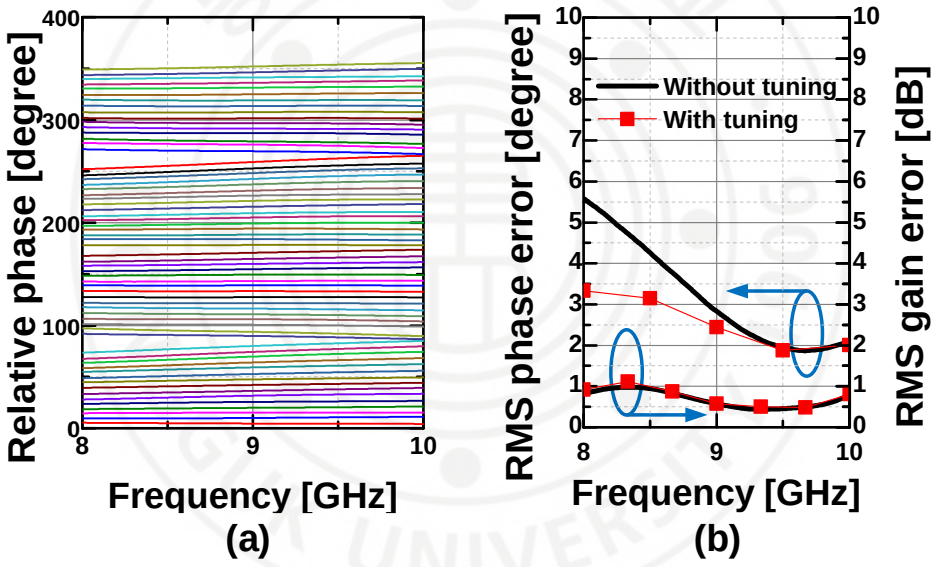


Figure 3.16 Measured (a) relative phase (b) RMS phase, gain error of all phase state.

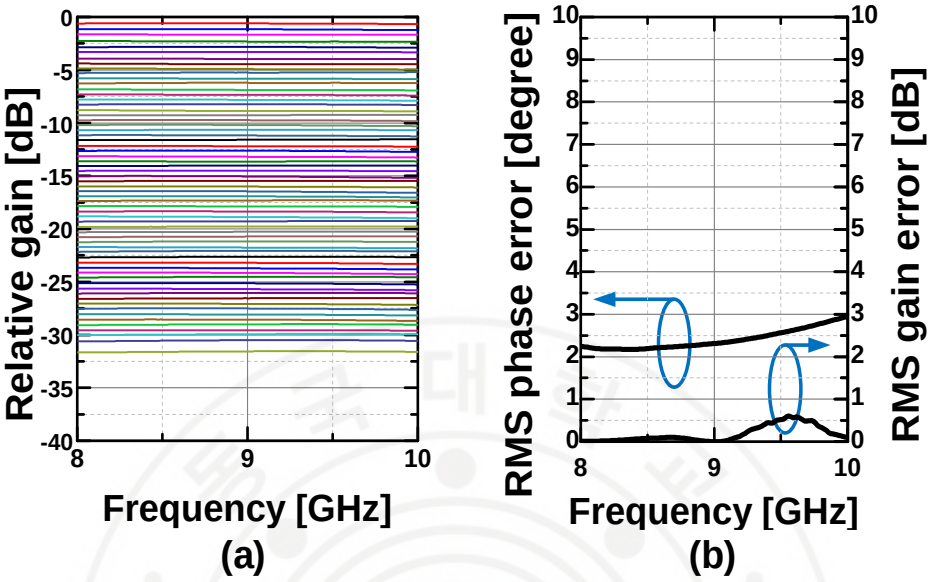


Figure 3.17 Measured attenuation characteristics of all attenuation states: (a) relative gain and (b) RMS phase/gain errors.

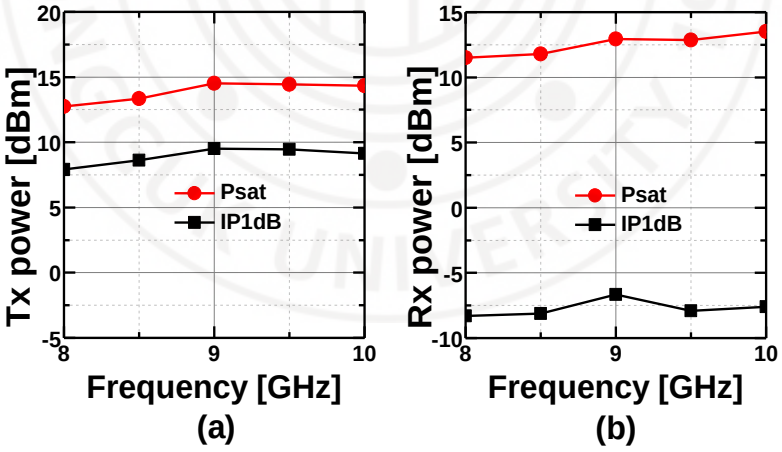


Figure 3.18 Measured saturated power and 1-dB compression point: (a) Tx and (b) Rx.

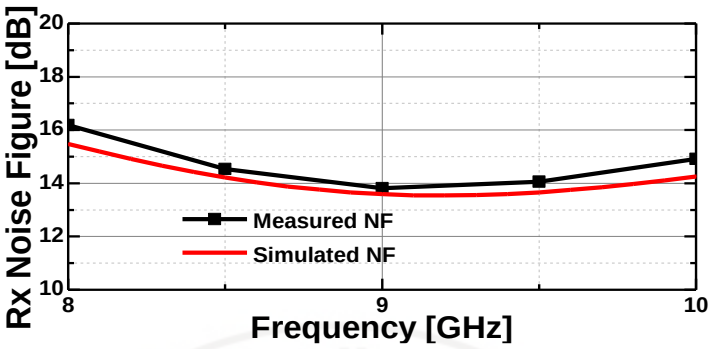


Figure 3.19 Measured Rx noise figure.

The large signal performance is summarized in Figure 3.18. Operating from a 1 V supply with a total current consumption of 80 mA, the MFC achieves a Tx OP1dB of 9.51 dBm and a saturated output power of 14.51 dBm at 9 GHz. In receive mode, the input-referred 1-dB compression point is -6.6 dBm, and the corresponding saturated output power is 12.9 dBm. The receive noise figure, shown in Figure 3.19, remains below 16.2 dB throughout the 8-10 GHz band, with a minimum value of 13.8 dB at 9 GHz.

3.5. Effect of Packaging

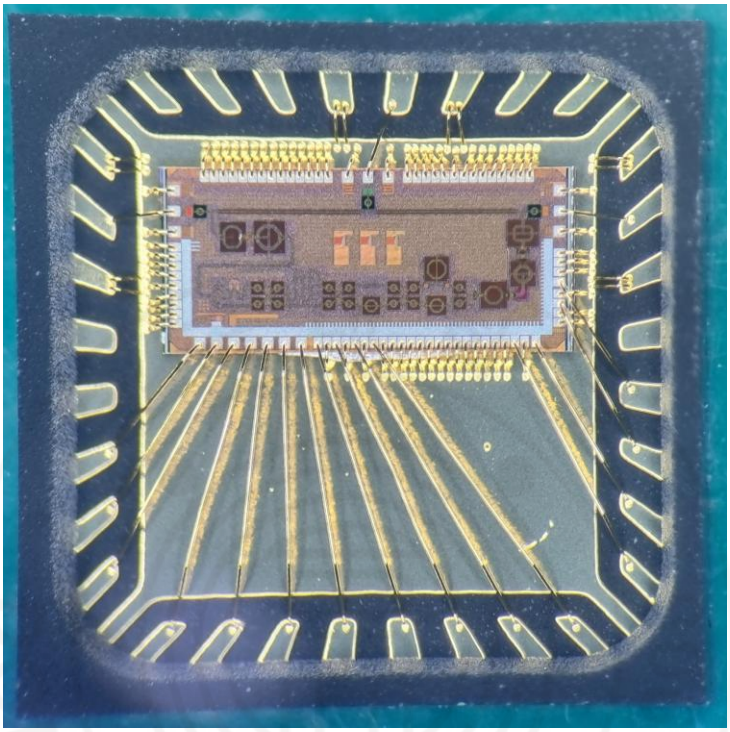
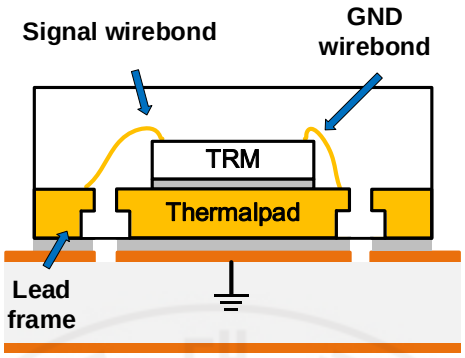
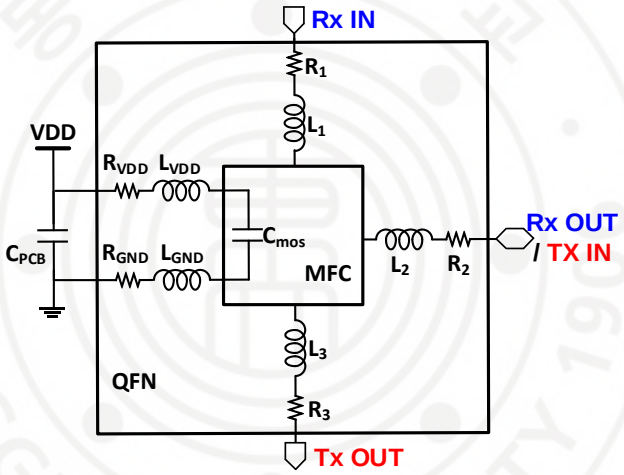


Figure 3.20 Packaged MFC with 5 × 5 32−pin QFN.

The MFC was also assembled in a 5 × 5 mm, 32−pin QFN package, as shown in Figure 3.20. The simplified cross−sectional view and equivalent circuit of the package are shown in Figure 3.21. Because the phase shifter is a passive network, the dominant package−induced error originates from the parasitic elements between the chip ground and the PCB ground. These parasitics cannot be de−embedded using standard transmission−line techniques, so accurate characterization and minimization through simulation are essential.



(a)



Equivalent Circuit Parameters

R_1	L_1	R_2	L_2	R_3	L_3
283mΩ	820pH	265mΩ	760pH	283mΩ	820pH
R_{VDD}	L_{VDD}	R_{GND}	L_{GND}	C_{MOS}	C_{PCB}
10mΩ	475pH	93uΩ	2.4 pH	100 pF	10 pF

(b)

Figure 3.21 Simplified (a) cross-sectional view and (b) equivalent circuit model of the package.

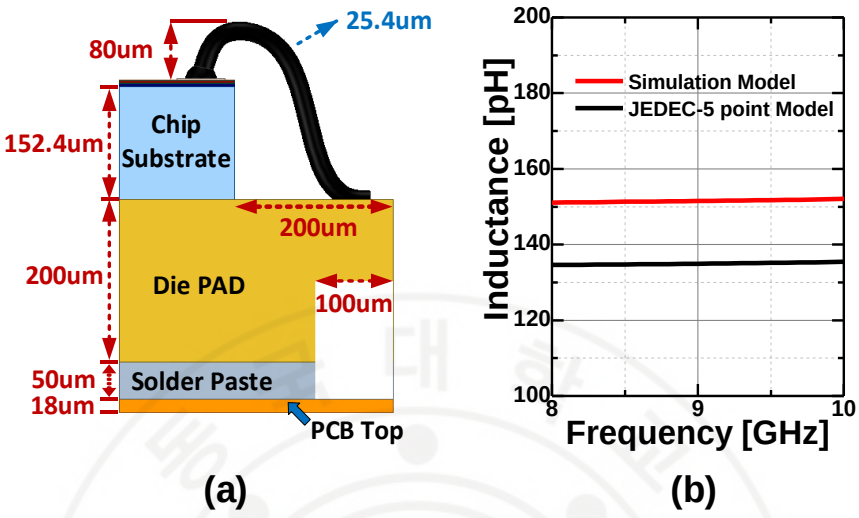


Figure 3.22 (a) Specific dimensions for ground-bonding simulation and (b) simulated parasitic inductance of a single GND bond.

The packaging modeling approach used in this analysis follows the methodology presented in [3.19].

The EM model used for ground-bonding analysis is shown in Figure 3.22. A single ground bond exhibits approximately 150 pH of inductance, which is roughly 20 pH higher than the JEDEC-5 specification. By using 60 parallel ground-bond wires, the total parasitic inductance is reduced to approximately 2.45 pH. The simulated relative RMS phase error versus ground parasitic inductance is shown in Figure 3.23, where the proposed hybrid phase shifter exhibits substantially lower phase distortion than a conventional filter-type phase shifter under the same ground-parasitic conditions.

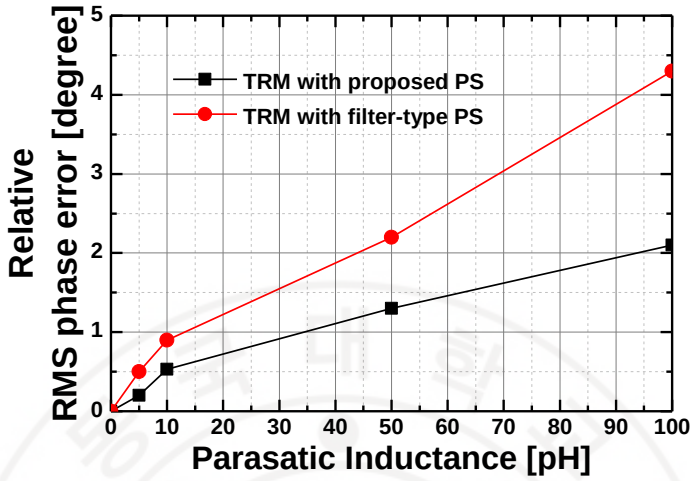


Figure 3.23 Simulated relative RMS phase error according to ground parasitic inductance at 9.5 GHz.

For RF signal bonding, three structures were considered: the proposed bonding structure, a conventional bonding structure, and a custom QFN structure, as shown in Figure 3.24. The parasitic inductance comparison in Figure 3.25 shows that the proposed bonding structure yields substantially lower parasitic inductance than the conventional one while achieving performance comparable to the custom package, but without the increased design and manufacturing complexity associated with the fully customized package. The full 3D EM model of the package is shown in Figure 3.26.

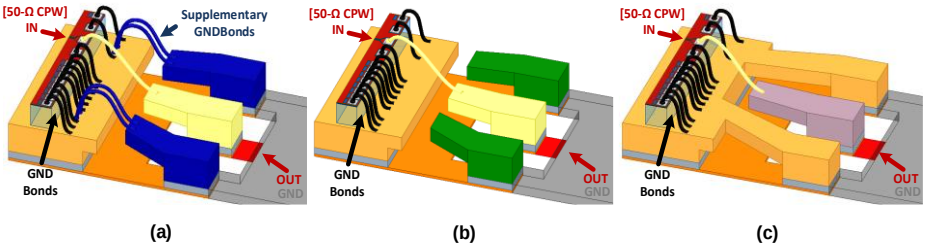


Figure 3.24 3D-EM simulation model of RF signal bonding: (a) proposed, (b) conventional, and (c) custom package.

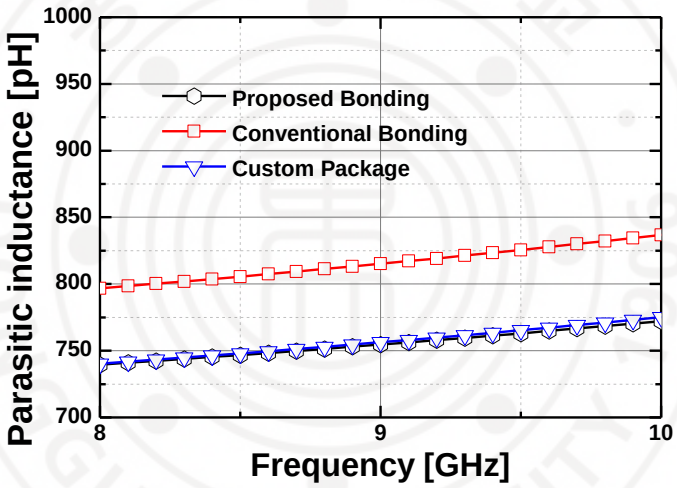


Figure 3.25 Simulation result of parasitic inductance for different bonding structures.

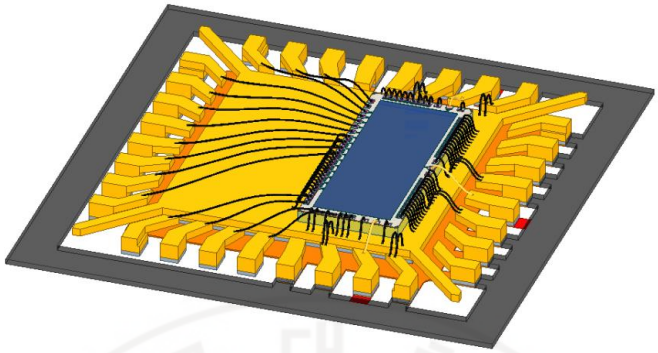


Figure 3.26 Full 3D EM simulation model of the QFN package.

Based on the full package model, the RMS phase error introduced by the package remains within 0.3◦, corresponding to less than 5% of the phase error observed in the COB configuration, as shown in Figure 3.27. To validate the package model, Figure 3.28 compares the equivalent−circuit simulation, the full wave EM package simulation, and the measured S21 response in the Tx reference state. The discrepancy is limited to within 0.4 dB, confirming the accuracy of the package model.

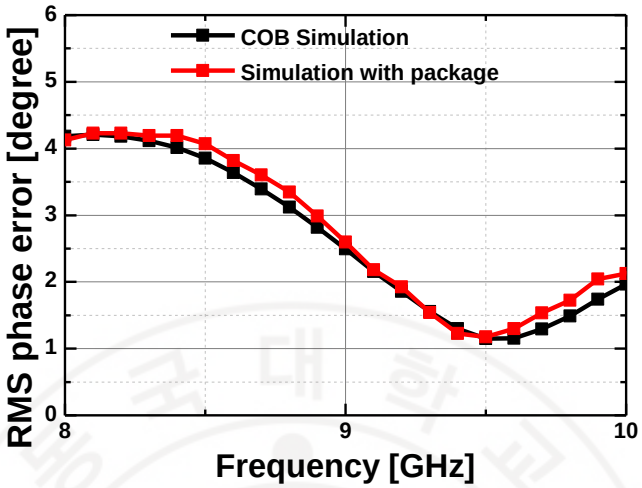


Figure 3.27 RMS phase error simulation results for COB and packaged MFC.

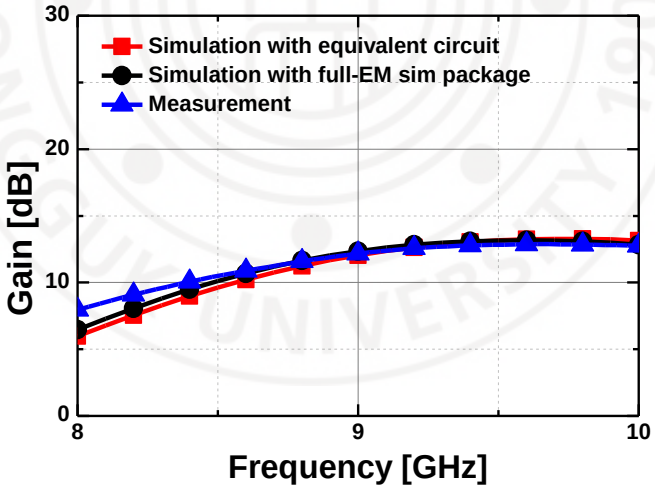


Figure 3.28 Gain comparison among equivalent-circuit simulation, full-EM package simulation, and measurement.

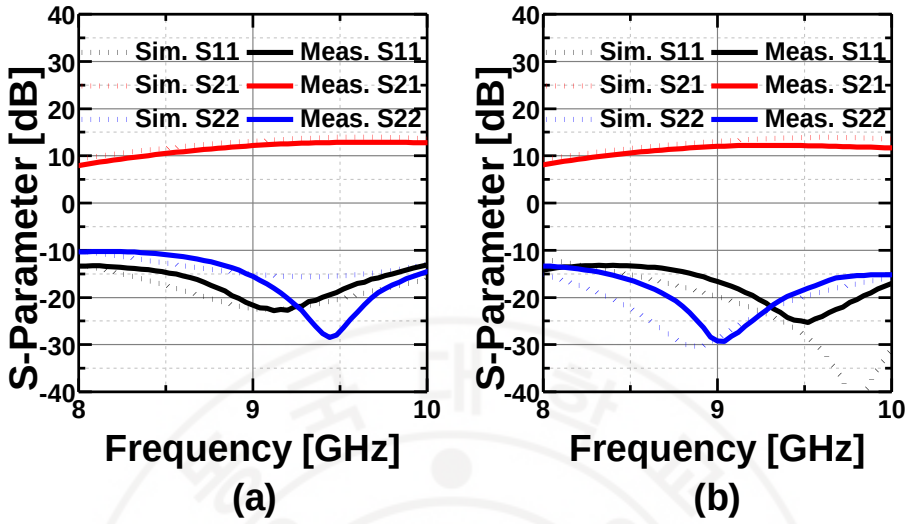


Figure 3.29 Measured S-parameter results of the packaged MFC: (a) Tx and (b) Rx.

The measured S-parameters of the packaged chip are shown in Figure 3.29. At 9 GHz, the packaged MFC achieves a Tx gain of 11.9 dB, and the 3dB bandwidth extends to 3.54 GHz. The gain difference between Tx and Rx paths remains within 0.1 dB. The return-loss results over all phase and attenuation states remain below -10 dB, as shown in Figure 3.30. Large-signal measurements in Figure 3.31 show a Tx OP1dB of 8.8 dBm and saturated output power of 12.9 dBm at 9 GHz, while the Rx IP1dB is -4.2 dBm and the corresponding saturated output power is 9.3 dBm. The packaged receive noise figure in Figure 3.32 remains below 16.8 dB across the 8-10 GHz band. Finally, Figure 3.33 presents the measured polar diagram for all 4096 phase/attenuation states at 9.5 GHz, confirming that the

intended beamforming states are accurately realized in the packaged MFC with minimal degradation.

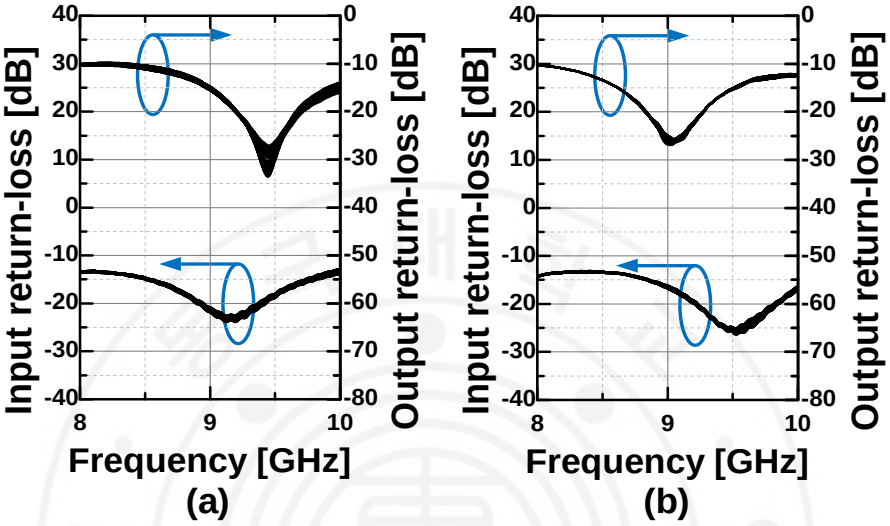


Figure 3.30 Input and output return loss over all phase and attenuation states of the packaged MFC: (a) Tx and (b) Rx.

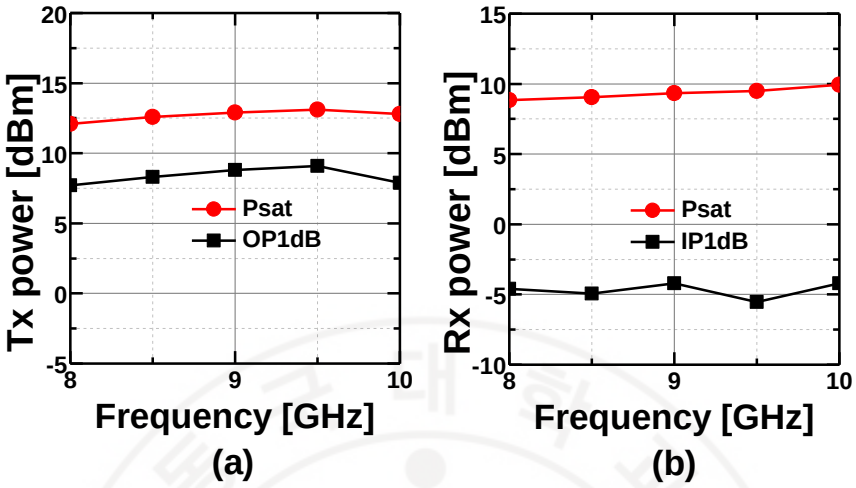


Figure 3.31 Measured saturated power and 1−dB compression point of the packaged MFC: (a) Tx and (b) Rx.

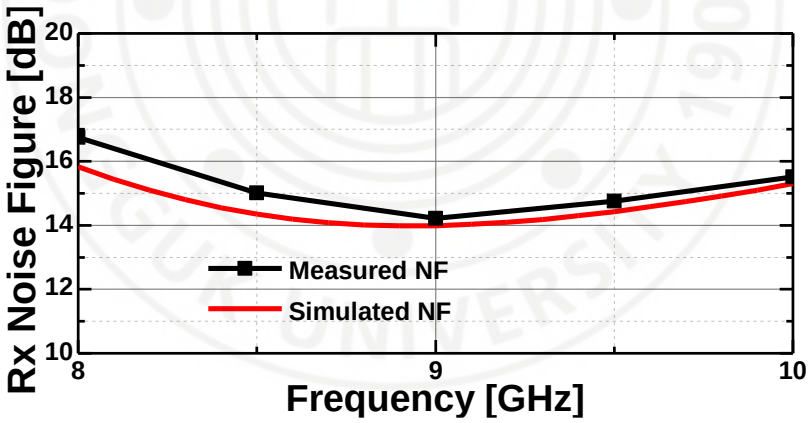


Figure 3.32 Measured Rx noise figure of the packaged MFC.

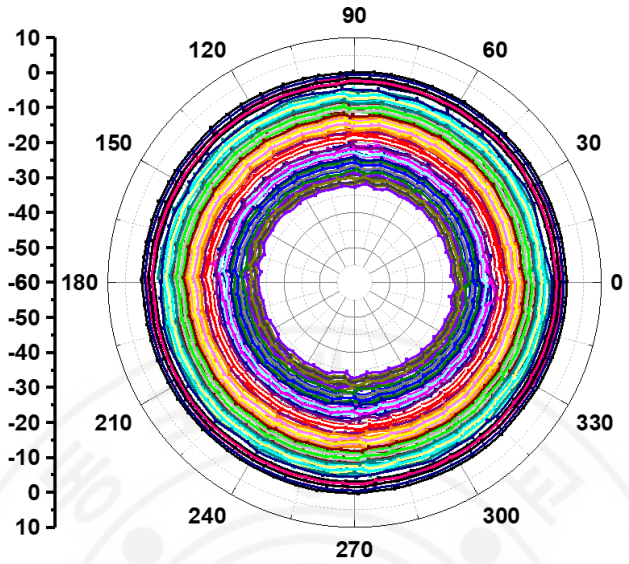


Figure 3.33 Measured polar diagram for all 4096 states of the packaged TRM.

3.6. Comparison With Previously Reported X-Band MFCs

Table 3.1 compares the proposed MFC with recently reported III-V and silicon-based MFCs around the X-band. Table 3.1 shows that the proposed work achieves the smallest chip area, lowest power consumption, and highest power efficiency among recently reported MFCs with the same topology, while maintaining excellent phase and gain accuracy. In the packaged condition, the MFC achieves RMS phase error 3.5°, RMS gain error 0.39 dB, Tx OP1dB 8.8 dBm, Tx/Rx gains 12.9/12.3 dB, and Rx NF 14.3 dB at 9 GHz.

This comparison confirms that the hybrid TTD/filter-based phase-shifter approach provides a balanced solution that combines accurate beamforming control, compact area, low power consumption, and strong packaging robustness, all of which are highly desirable for cost-efficient APAA applications.

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Table 3.1 Comparison of State-of-the-Art MFC Around the X-band.

Ref.		This work		[3.1]	[3.2]	[3.3]	[3.4]	[3.5]	[3.6]	[3.7]	[3.8]	[3.9]	[3.10]
		COB	QFN										
Tech		65nm CMOS	65nm CMOS	GaAs	250nm GaAs	150nm GaAs	130nm SiGe	250nm SiGe	65nm CMOS	65nm CMOS	130nm CMOS	130nm CMOS	180nm CMOS
Topology		MFC with SPDT	MFC with SPDT	MFC with SPDT	*Bi-Directional	MFC with SPDT	**Bi-Directional	***Bi-Directional	Bi-Directional	Bi-Directional	*Bi-Directional	MFC with SPDT	MFC with SPDT
# of Channel		1	1	1	1	1	1	1	1	1	1	1	1
Frequency [GHz]		8~10	8~10	8-12	6-18	8~11	8~24	8~12	8~10.5	8~12	8.5~10.5	9~10.5	8.5~10
Gain [dB]	Tx	14.1/1.2†	12.9/-0.6†	6	12	15.9	16.1	-11.5	3.7	15	3.5	20	12
	Rx	14.0/1.2†	12.3/-0.6†	6	12	8.9	16.1	-11.5	3.7	15	3.5	12	11
Rx NF [dB]		13.8	14.3	-	18	-	11.6	-	10	8.4	7.5	8.5	8.5
Gain Tuning Range/Step [dB]		31.5/0.5	31.5/0.5	31.5/0.5	31.75/0.25	31.5/0.5	31.5/0.5	31.5/0.5	31.5/0.5	31.5/0.5	31/1	31.5/0.5	31.5/0.5
RMS Gain Error [dB]		0.31	0.39	0.4 @10GHz	0.5	0.28	0.4	0.57	0.5	0.45	0.8	0.44	0.25
Phase Step [°]		5.625	5.625	5.625	3.6*** @10GHz	5.625	11.25	5.625	5.625	5.625	5.625	5.625	5.625
RMS Phase Error [°]		3.3	3.5	3 @10GHz	6.1*** @10GHz	3.3	4.4	4	4	5	4.3	4.3	2
TX OP1dB [dBm]		9.5	8.8	11	16.5	11.9	-8.09	-	5.1	11.84	6.5	9.7	11.5
RX IP1dB [dBm]		-6.6	-4.2	-	-	-0.1	-	12	-	-	-	-	1.5
P_{DC}/CH [mW]	Tx	80/18†	80/18†	360	1600	-	55	143	170	216	154	250	640
	Rx	80/18†	80/18†		1600	-	55	143	170	110	154	120	670
PE @ OP1dB		11.1%	9.5%	2.5%	0.8%	-	0.3%	-	1.9%	7.1%	2.9%	3.7%	2.2%
Chip Area [mm^2]		3.9 (with ESD)	5x5 QFN	17.86	20	12.2	3.28	3.25	9.56	7.52	1.19	17.2	12.8

†Low Bias Mode
*TTD Design
**Without PA, LNA
***calculated from TTD

3.7. Conclusion

This chapter has presented a fully integrated X-band multifunction chip implemented in a 65-nm CMOS process. The key idea of the design is the use of a hybrid passive phase shifter in which TTD cells are assigned to the lower bits and filter-based phase-shifter cells are assigned to the higher bits, thereby suppressing mismatch-induced phase distortion while minimizing chip area. The chip also integrates a 6-bit attenuator, transformer-based LNA and PA, SPI control, and path-preserving SPDT switching, thereby enabling a compact and efficient MFC for X-band phased-array systems.

The COB measurements verified an RMS phase error of 3.33° after tuning, an RMS attenuation error of 0.31 dB, a Tx small-signal gain of 14.1 dB, a Tx OP1dB of 9.51 dBm, and an Rx noise figure below 16.2 dB over the 8–10 GHz band. After QFN packaging, the phase error degradation remained minimal, with packaged RMS phase error of 3.5°, gain error below 0.39 dB, Tx/Rx gains of 12.9/12.3 dB, a Tx OP1dB of 8.8 dBm, and receive noise figure below 16.8 dB. Compared with previously reported X-band MFCs of similar topology, the proposed design achieves the smallest chip area, lowest power consumption, and highest power efficiency.

The package-related implementation and bias circuit were developed with contributions from Jun Kwon, and the ESD protection circuit was designed with contributions from Hyeong-Geun Park.

The remaining MFC integration, measurement, analysis, and validation presented in this chapter were conducted by the author.

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Chapter 4. 275 GHz Quadrature Receivers

4.1. Introduction

As the operating frequency of wireless systems extends toward the sub-THz region, the dominant design priorities of RF frontends change significantly. In contrast to X-band beamforming frontends, where phase accuracy, delay control, and multifunction integration are the primary concerns, sub-THz receiver design is mainly constrained by the limited gain margin of active devices, the high loss of passive structures, and the difficulty of efficient local oscillation generation. In particular, the 275-296 GHz band has attracted considerable interest because it provides extremely wide available bandwidth for short range ultra high data rate wireless links and future indoor fiber-wireless networks [4.1], [4.2].

Recent studies have demonstrated the feasibility of high data rate sub-THz wireless links using both SiGe and CMOS technologies [4.3]-[4.10]. In addition, various receiver architectures operating in similar frequency bands have been reported in recent years [4.11]-[4.16]. Among them, direct conversion I/Q receivers are attractive for broadband demodulation because they directly translate the RF signal into baseband or IF outputs suitable for subsequent digital signal processing. However, at 275 GHz, sufficient LO power, quadrature accuracy, broadband down conversion, and acceptable noise performance must all be achieved simultaneously, which makes

the receiver architecture and LO generation scheme critical design issues.

Another important question in sub-THz receiver design is whether the RF front end should employ a mixer first or an LNA first architecture. A mixer first structure can improve the conversion gain and noise performance of the receiver chain under limited RF device performance, whereas an LNA first structure can improve the receiver noise figure and increase the signal to noise ratio by amplifying the RF signal before down conversion [4.14], [4.16]. Therefore, a direct comparison between these two receiver organizations under the same process and operating band is meaningful from both circuit and architecture perspectives.

This chapter presents two 275 GHz quadrature receivers implemented in a 130-nm SiGe BiCMOS process: a mixer first receiver (Rx1) and an LNA first receiver (Rx2). Both receivers down convert RF signals from 260 to 290 GHz into differential I and Q IF outputs from 0.1 to 30 GHz. To realize a compact quadrature receiver, a complete 260 GHz LO chain is integrated on-chip, consisting of an E-band driving amplifier, a frequency tripler, two 260 GHz driving amplifiers, and a differential hybrid coupler. In addition, a modified Gilbert-cell mixer with swapped RF and LO ports is employed to improve noise and conversion characteristics at sub-THz frequencies [4.16]. Measured results show that the implemented receivers achieve peak conversion gains of 21.4 dB and 27.5 dB,

minimum single sideband noise figures of 22.3 dB and 20.1 dB, and 30 GHz IF bandwidth in both architectures. The overall architectures of the proposed receivers are shown in Figure 4.1. This chapter is organized as follows. Section 4.2 describes the architecture and core building blocks of the proposed quadrature receivers. Section 4.3 presents the measured results and discusses the trade-offs between the two receiver topologies. Section 4.4 compares the implemented receivers with previously reported sub-THz receivers. Finally, Section 4.5 concludes the chapter.

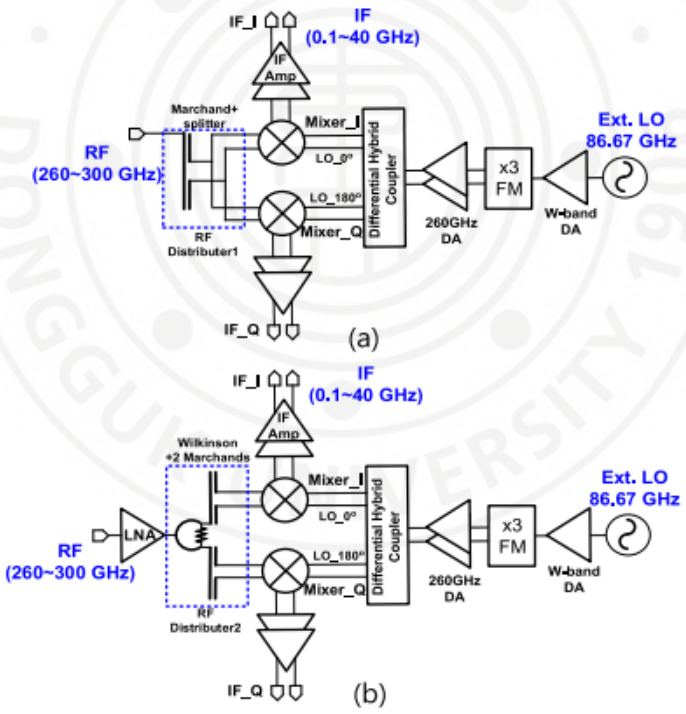


Figure 4.1 Block diagrams of the proposed 275 GHz quadrature receivers: (a) mixer first receiver (Rx1), and (b) LNA first receiver (Rx2).

4.2. 275 GHz Integrated Quadrature Receivers

The proposed sub-THz receivers are designed to convert a single-ended RF signal in the 260–290 GHz band into differential I and Q IF outputs over a 0.1–30 GHz band. Both receivers share the same down conversion principle and LO generation strategy, but differ in the arrangement of the RF front end. In the mixer first receiver, the RF input is first converted into a differential signal and then directly distributed to the RF ports of the I and Q mixers. In the LNA first receiver, the RF input is first amplified by a 275 GHz low-noise amplifier and is then distributed to the I and Q mixers. Thus, the two receivers provide a direct comparison between reduced front end complexity and improved RF gain before down conversion.

A compact quadrature LO chain is integrated into each receiver. An external 86.67 GHz signal is applied to the chip and frequency-tripled to 260 GHz. The generated LO signal is then amplified and split by a differential hybrid coupler to provide quadrature LO signals for the I and Q mixers. The down converted IF outputs are amplified by broadband IF amplifiers to drive external DSP or measurement instruments. This architecture is intended to provide a cost-effective receiver solution for the indoor fiber-wireless interface envisioned in future 6G systems. As illustrated in Figure 4.1, the two receivers share the same LO and IF concept, while differing in the placement of the RF front end gain stage.

4.2.1 275 GHz Low-Noise Amplifier

In the LNA first receiver, a 275 GHz low-noise amplifier is placed at the RF input to improve the receiver sensitivity. The amplifier consists of six cascaded common-emitter stages, where impedance matching is achieved using microstrip transmission lines and series matching capacitors. Rather than introducing a dedicated output matching network, the output impedance of the LNA is co-designed with the input impedance of the following RF distributor, so that the interface approximates conjugate matching over the operating band. The circuit schematic of the designed LNA is shown in Figure 4.2.

Simulation results show that the designed LNA achieves a peak gain of 8 dB and a 3dB gain bandwidth of 56 GHz from 245 GHz to 301 GHz. The simulated noise figure ranges from 14.2 dB to 16.5 dB. Large-signal simulation also shows an IIP3 of 14.22 dBm while consuming 31.6 mA from a 1.6 V supply. These results indicate that the LNA can provide broadband RF gain with acceptable noise performance in the target frequency range. The simulated small-signal and noise characteristics are summarized in Figure 4.3, and the simulated large-signal behavior is shown in Figure 4.4.

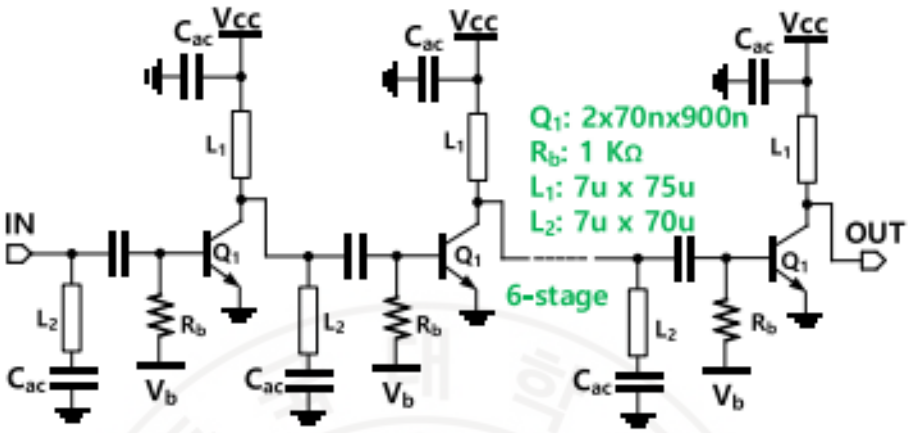


Figure 4.2 Schematic of the 275 GHz low-noise amplifier.

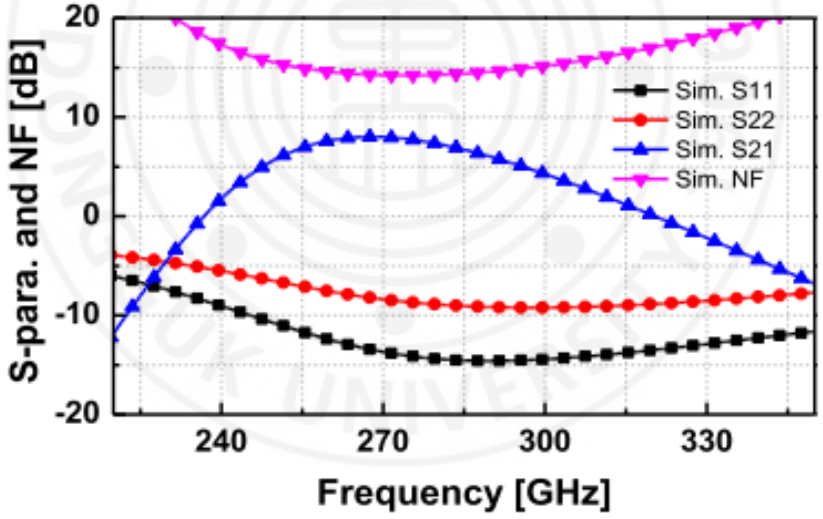


Figure 4.3 Simulated S-parameters and noise figure of the designed 275 GHz low-noise amplifier.

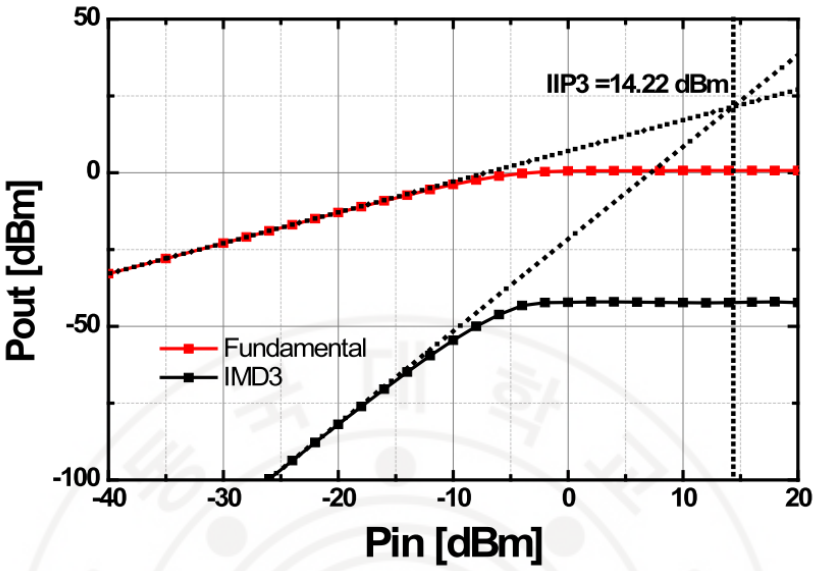


Figure 4.4 Simulated large-signal characteristic of the designed 275 GHz low-noise amplifier.

4.2.2 RF Signal Distributor

To drive the I and Q mixers, the RF signal must be converted into appropriate differential forms and evenly distributed to the two paths. In the mixer first receiver, a compact RF distributor composed of a Marchand balun followed by a power splitter is used. This structure offers a relatively small form factor and achieves around 2 dB insertion loss and about 11 dB isolation between the I and Q RF ports at 275 GHz. The three-dimensional EM structure of the RF distributor is shown in Figure 4.5.

In the LNA first receiver, a different RF distributor is employed to improve the I/Q path balance. Specifically, a Wilkinson divider

followed by two Marchand baluns is used. Although this arrangement occupies a larger area, it achieves less than 2 dB intrinsic insertion loss from 260 GHz to 300 GHz, better than 10 dB return loss at the input and output ports, and more than 25 dB isolation between the I and Q paths. This improved balance later appears in the measured quadrature accuracy of the LNA first receiver. The simulated S-parameters of the designed distributor are shown in Figure 4.6.



Figure 4.5 Three-dimensional EM structure of the 275 GHz RF signal distributor.

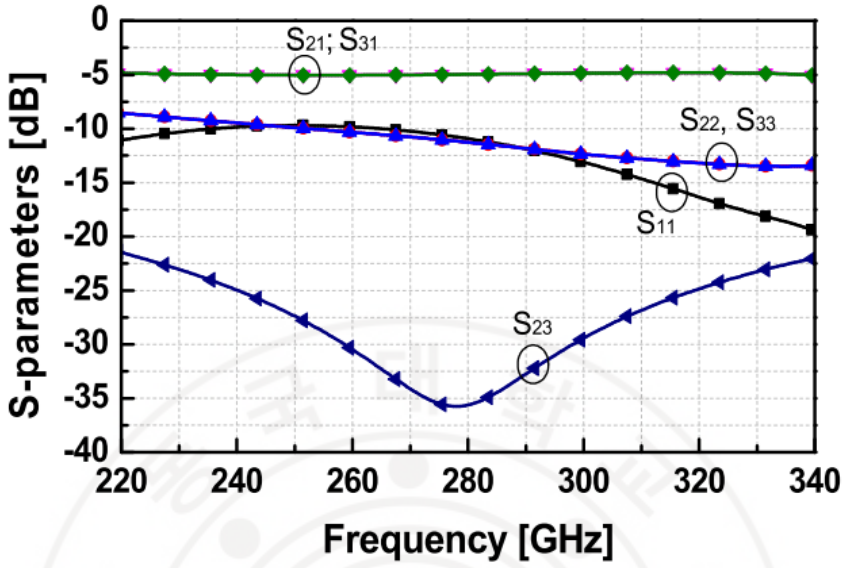


Figure 4.6 Simulated S-parameters of the designed RF signal distributor.

4.2.3 Modified Gilbert-Cell Down Conversion Mixer

To realize wideband down conversion with improved isolation and operation efficiency, both receivers employ active double-balanced mixers based on a modified Gilbert-cell structure, as shown in Figure 4.7. In a conventional Gilbert-cell mixer, parasitic capacitance at the common node can significantly degrade the effective conversion gain and noise performance at very high frequencies. To reduce this effect, the proposed design swaps the RF and LO ports relative to the conventional configuration. Although the theoretical mixed current depends on the product of the RF and LO switching functions and is therefore fundamentally symmetric with respect to port assignment,

the practical parasitic environment is not symmetric. As compared in Figure 4.8, the modified mixer achieves approximately 2.3 dB lower minimum noise figure and 0.8 dB higher maximum available gain than the standard Gilbert-cell mixer at P_{LO}=0 dBm.

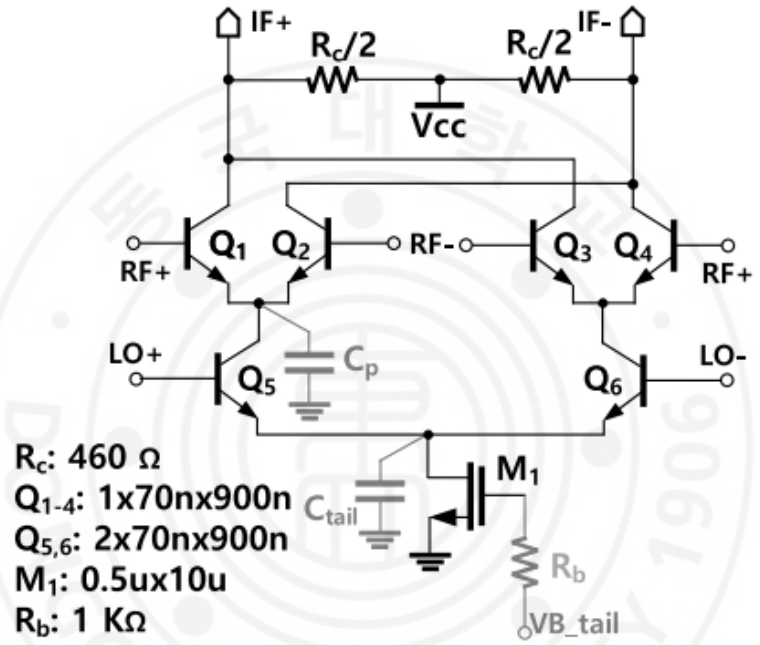


Figure 4.7 Schematic of the modified Gilbert-cell mixer.

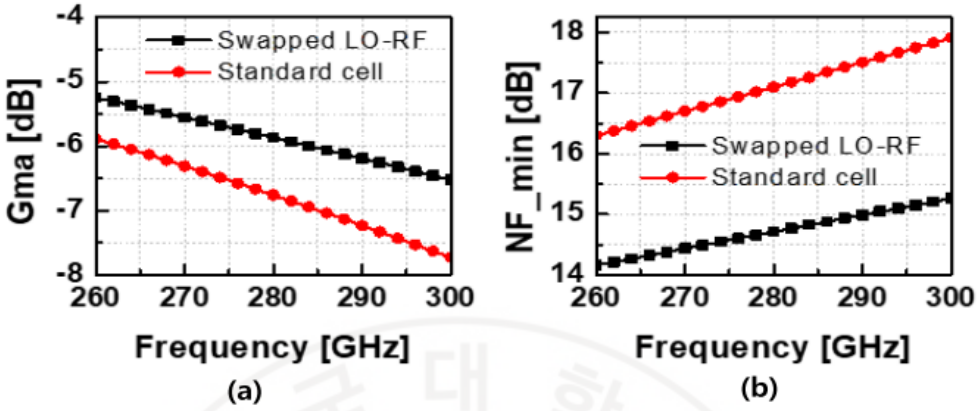


Figure 4.8 Simulated maximum available gain and minimum noise figure of the standard Gilbert-cell mixer and the modified mixer with swapped RF and LO ports.

4.2.4 Broadband IF Amplifier

After down conversion, the IF signal is amplified by a broadband IF amplifier to support the wide IF band required for high-data-rate operation. The amplifier schematic is shown in Figure 4.9. To achieve broad bandwidth, the amplifier employs inductive peaking and staggered matching. Spiral inductors and resistors are connected in series as wideband loads, and the load resistances are adjusted from stage to stage so that the resonance peaks of the individual stages are slightly shifted, thereby broadening the overall frequency response. As seen in Figure 4.10, the simulated IF gain peaks at 35 dB around 40 GHz with approximately 4% group-delay variation from 1 GHz to 40 GHz. The simulated large-signal response in Figure 4.11 further shows an output 1dB compression point of about −12.3

dBm at 25 GHz. The amplifier consumes 40 mA with Vb = 1V and Vcc = 2.3 V.

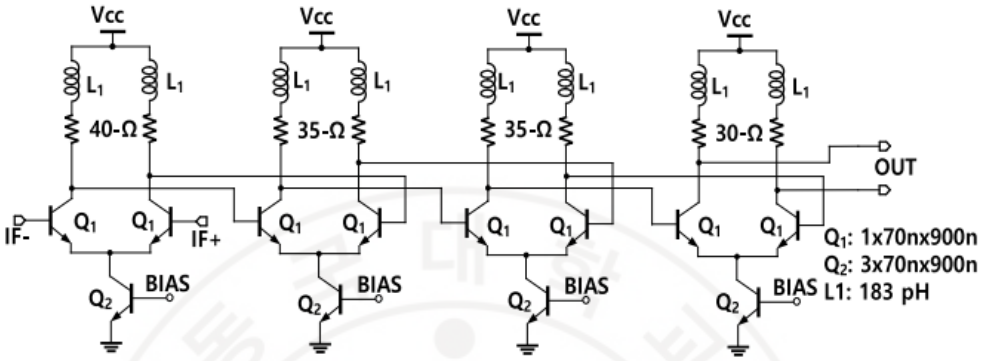


Figure 4.9 Schematic of the broadband IF amplifier.

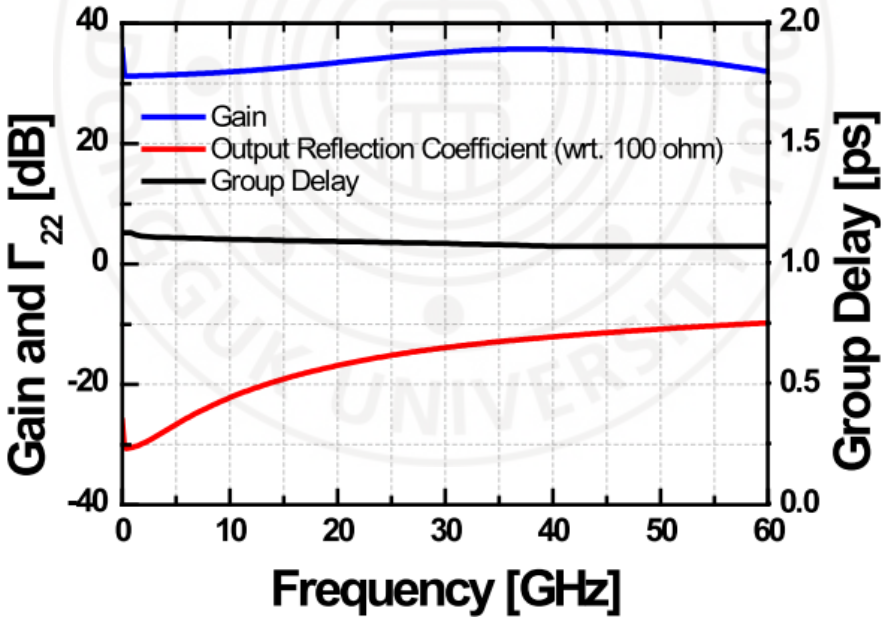


Figure 4.10 Simulated voltage gain, output reflection coefficient, and group delay of the broadband IF amplifier under down conversion operation.

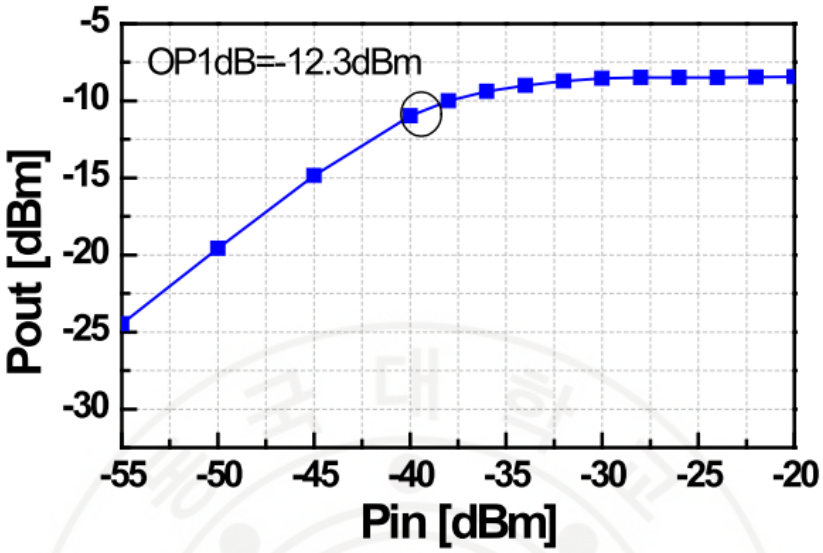


Figure 4.11 Simulated output power versus input power of the broadband IF amplifier at 25 GHz.

4.2.5 260 GHz Quadrature LO Chain

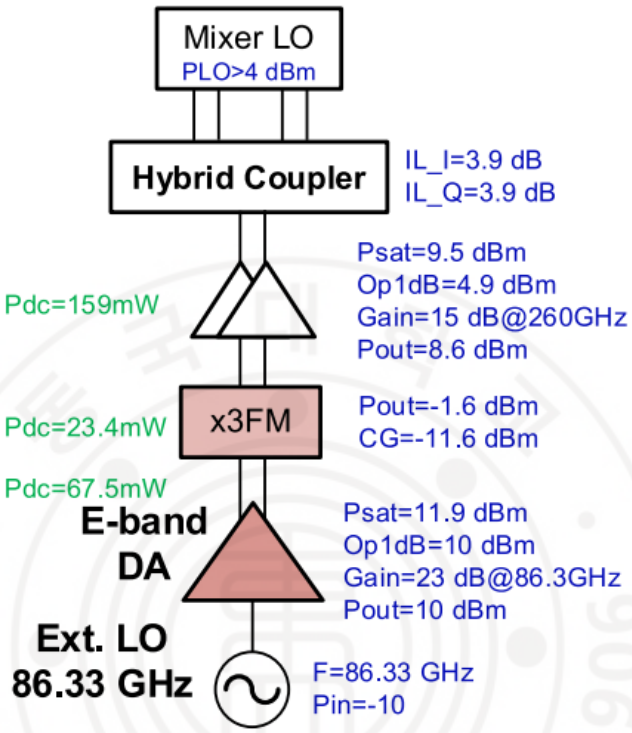


Figure 4.12 Power budget of the designed 260 GHz LO chain.

To realize a compact and cost-effective quadrature receiver, a complete 260 GHz LO chain is integrated on-chip. The LO power budget of the overall chain is summarized in Figure 4.12. The chain accepts an external 86.67 GHz sinusoidal input and converts it into 260 GHz quadrature LO signals for the I and Q mixers. The LO chain consists of an E-band driving amplifier, a frequency tripler, two 260 GHz driving amplifiers, and a differential hybrid coupler.

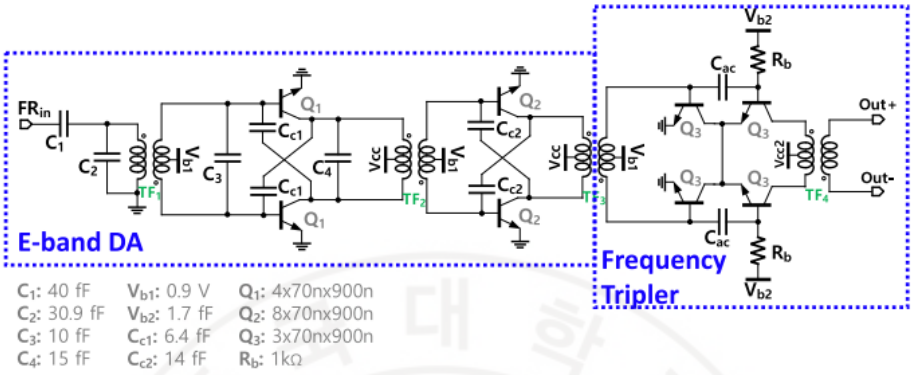


Figure 4.13 Schematic of the E-band driving amplifier cascaded with the frequency tripler.

The tripler is implemented as a push-push doubler followed by a single-balanced mixer. This arrangement is beneficial because the unwanted harmonic leakage from the LO chain is kept away from the 0-30 GHz IF band. The E-band driving amplifier provides sufficient drive for the tripler with a relatively small external input power of about −10 dBm. The circuit topology of the E-band amplifier and the tripler is shown in Figure 4.13. According to the harmonic-balance and transient simulations in Figure 4.14 and Figure 4.15, the integrated tripler produces a differential 260 GHz output of approximately −1.7 dBm from a −10 dBm input signal.

The generated 260 GHz signal is then amplified by two 260 GHz driving amplifiers, whose schematic is shown in Figure 4.16. The simulated small-signal characteristics in Figure 4.17 show a peak

gain of 18 dB at 240 GHz, while the large-signal results in Figure 4.18 and Figure 4.19 confirm that the amplifier can provide the LO power required for the intended double-balanced down conversion operation.

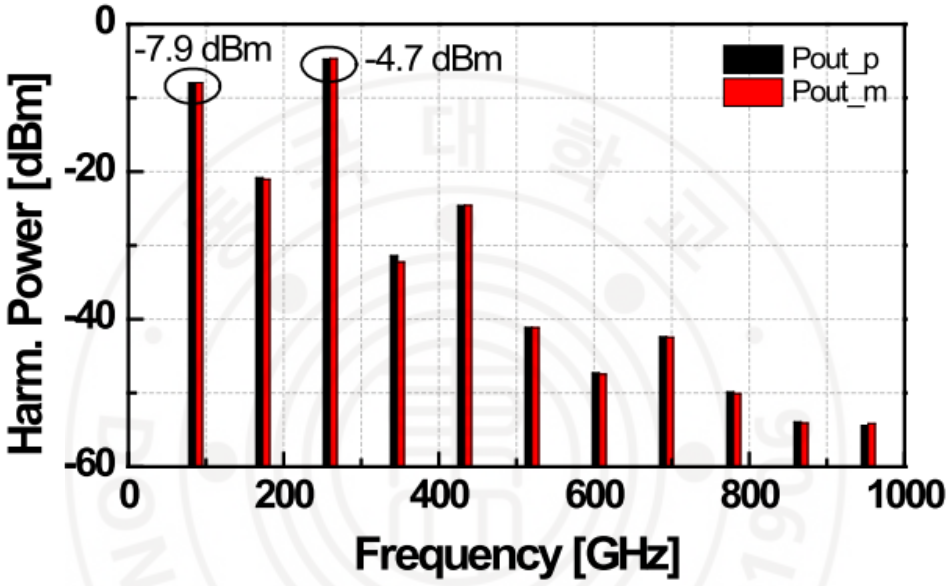


Figure 4.14 Harmonic-balance simulation results of the frequency tripler combined with the E-band driving amplifier

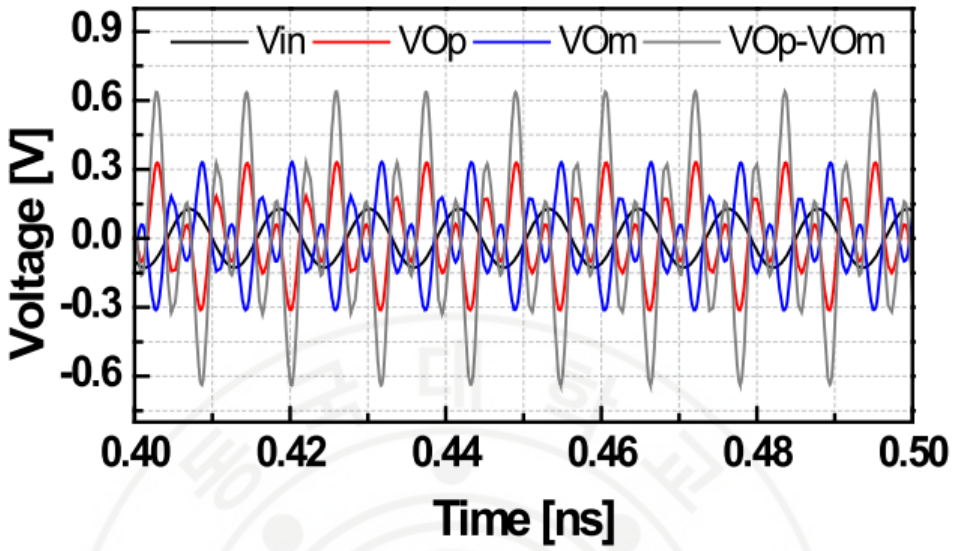


Figure 4.15 Transient simulation results of the frequency tripler combined with the E-band driving amplifier.

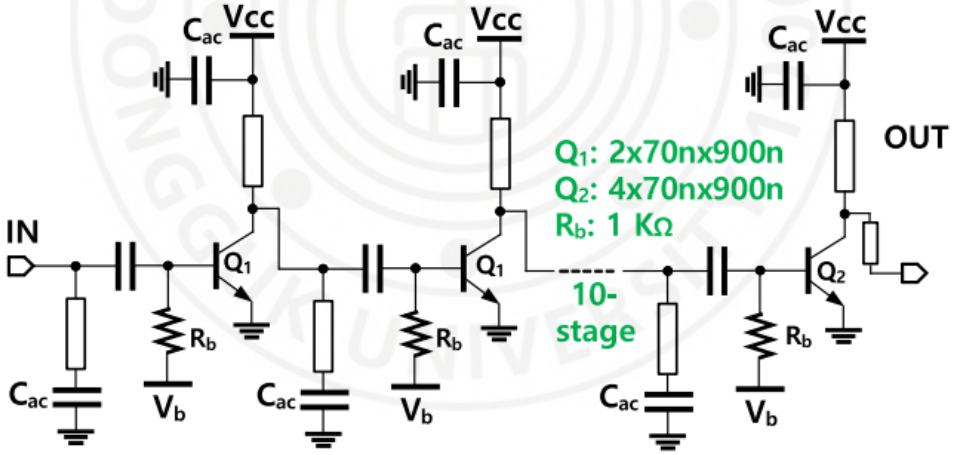


Figure 4.16 Schematic of the 260 GHz driving amplifier in the LO chain.

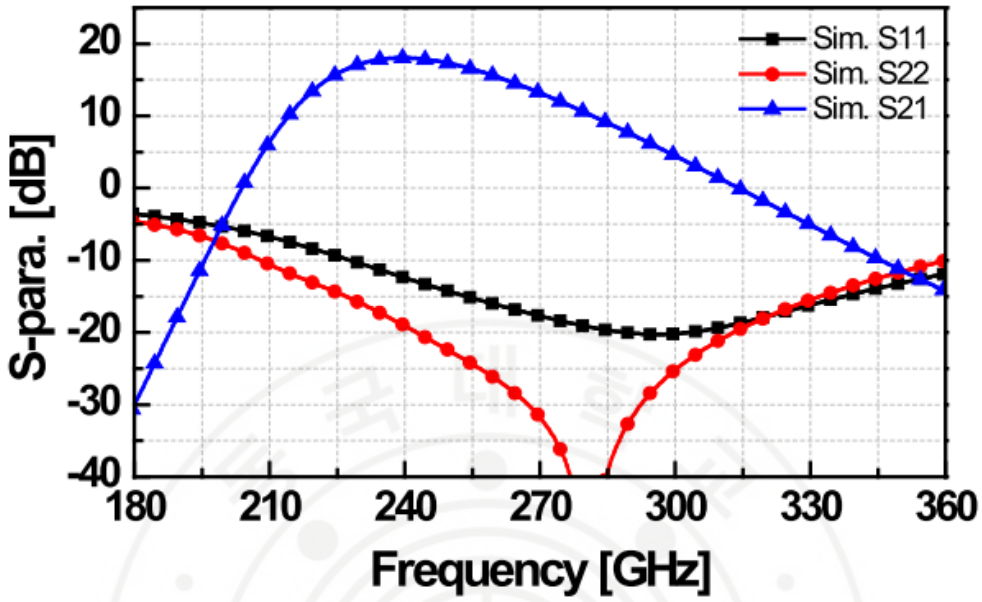


Figure 4.17 Simulated S-parameters of the 260 GHz driving amplifier.

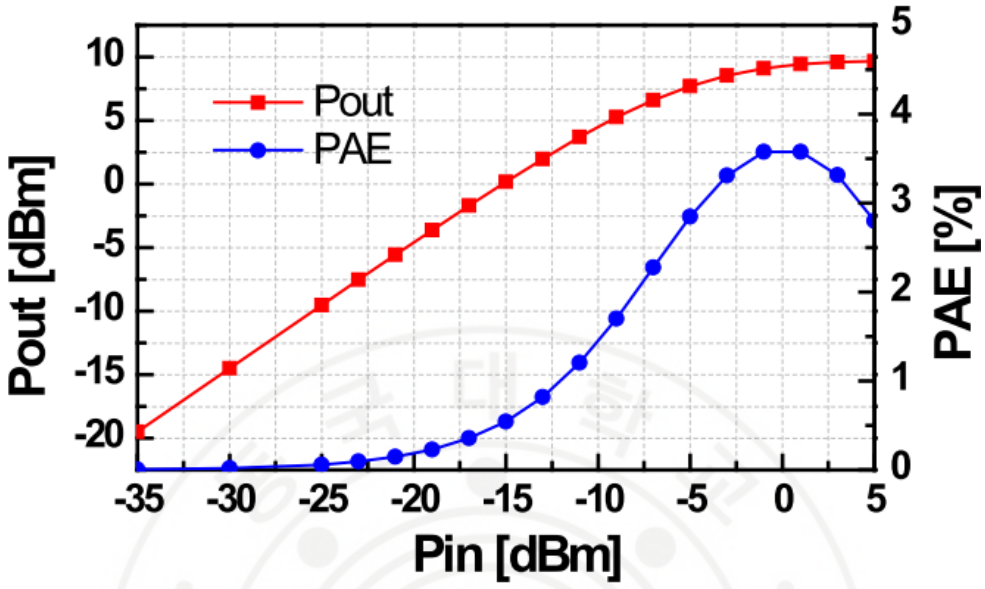


Figure 4.18 Simulated output power and power-added efficiency of the 260 GHz driving amplifier at 260 GHz.

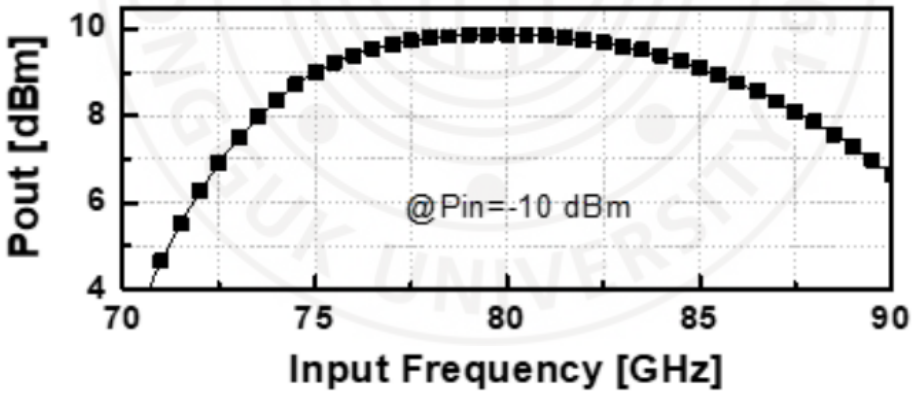


Figure 4.19 Simulated output power of the 260 GHz driving amplifier versus W-band input frequency.

4.3. Measurement Results and Discussion

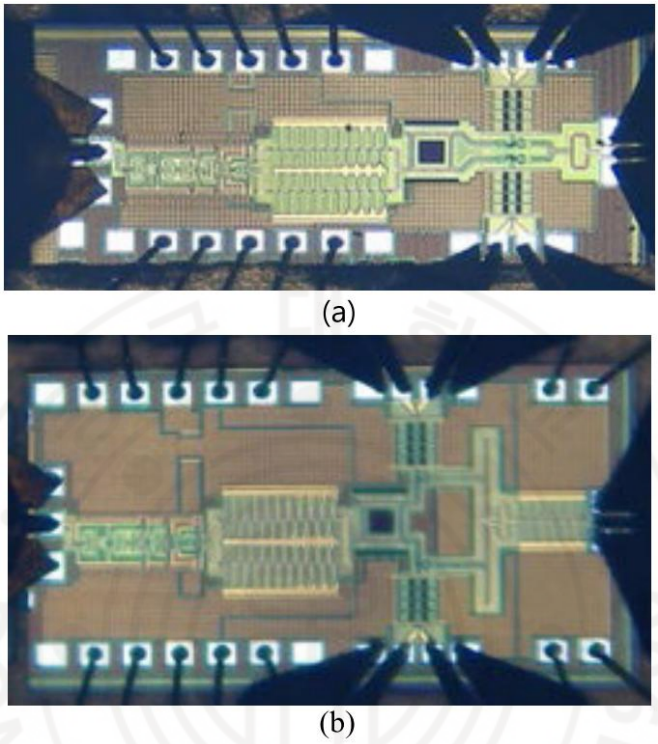


Figure 4.20 Chip photographs of the fabricated 275 GHz quadrature receivers: (a) mixer first receiver, and (b) LNA first receiver.

Figure 4.20 shows the fabricated chip photographs of the implemented mixer first and LNA first receivers. The measured chip area is 1.418 mm^2 for Rx1 and 2.030 mm^2 for Rx2, while the corresponding DC power consumptions are 438 mW and 490 mW, respectively. The increase in both area and power for the LNA first receiver mainly results from the addition of the RF LNA and the more balanced RF distribution network.

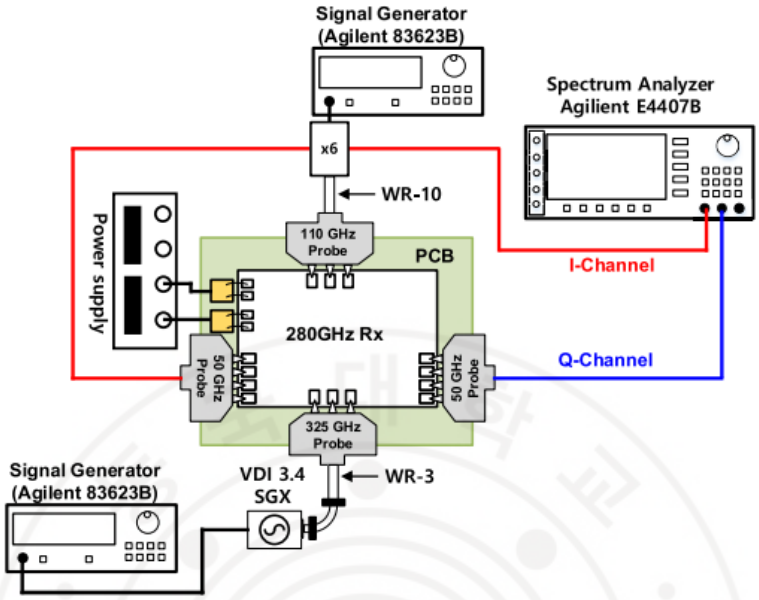


Figure 4.21 Measurement setup for gain characterization of the 275 GHz quadrature receiver.

The conversion gain was measured using the setup shown in Figure 4.21, where the RF signal was generated through an up-conversion mixer and the 86.67 GHz LO input was externally provided through a signal generator and multiplier chain. As plotted in Figure 4.22, the mixer first receiver achieves a peak conversion gain of 21.4 dB, whereas the LNA first receiver achieves a peak conversion gain of 27.5 dB. In both cases, the IF bandwidth reaches 30 GHz. The gain mismatch between the I and Q channels is about 1 dB in Rx1 and 0.7 dB in Rx2, indicating good quadrature-path balance.

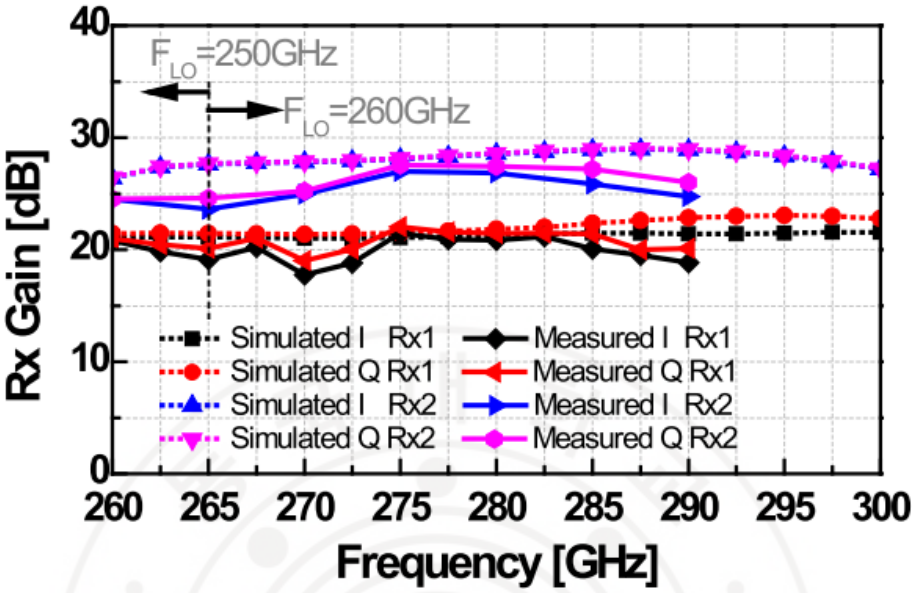


Figure 4.22 Measured and simulated conversion gains of the proposed receivers.

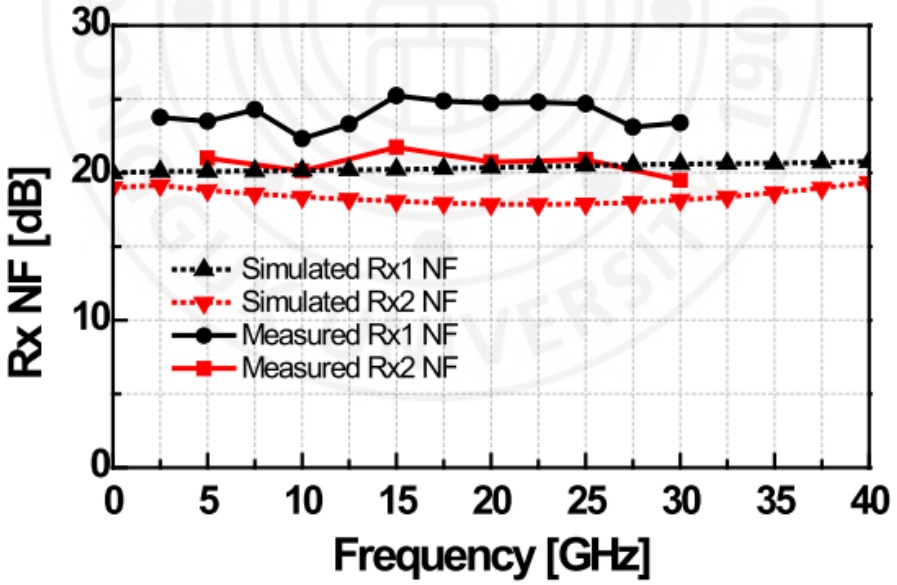


Figure 4.23 Measured and simulated single-sideband noise figures of the proposed receivers.

The noise figure was evaluated using the gain method based on the IF output noise floor. As shown in Figure 4.23, the measured single-sideband noise figure of Rx1 is around 23 dB, with a minimum value of 22.3 dB at 10 GHz IF, whereas Rx2 shows an approximately 21 dB noise figure with a minimum value of 20.1 dB at the same IF frequency. Therefore, the LNA first topology improves the receiver noise figure by about 1.3 dB relative to the mixer first topology, although this improvement is obtained at the cost of higher power dissipation and larger chip area.

To evaluate the I/Q balance, the two IF outputs were monitored simultaneously and the relative phase difference was extracted. The measured and simulated phase mismatches are compared in Figure 4.24. The measured phase imbalance of Rx1 remains about 4° within the 30 GHz IF bandwidth. Because the RF distribution structure of Rx2 is more symmetric, using a Wilkinson divider followed by two Marchand baluns, the LNA first architecture exhibits improved phase balance relative to the mixer first case.

Based on the measured I/Q amplitude and phase mismatches of Rx1, the image rejection ratio was calculated, and the result is presented in Figure 4.25. The image rejection ratio is approximately 27 dB on average and reaches a maximum value of 34.2 dB at 260 GHz. These results indicate that the implemented receivers support broadband quadrature operation suitable for high-order modulation.

From an architecture point of view, the measurement results verify a clear trade-off. Relative to Rx1, the LNA first receiver increases power dissipation by approximately 13% and chip area by approximately 43%, while improving the receiver noise figure by about 1.3 dB. Thus, the mixer first receiver is advantageous when compactness and lower power are more important, whereas the LNA first receiver is preferable when sensitivity and gain are prioritized.

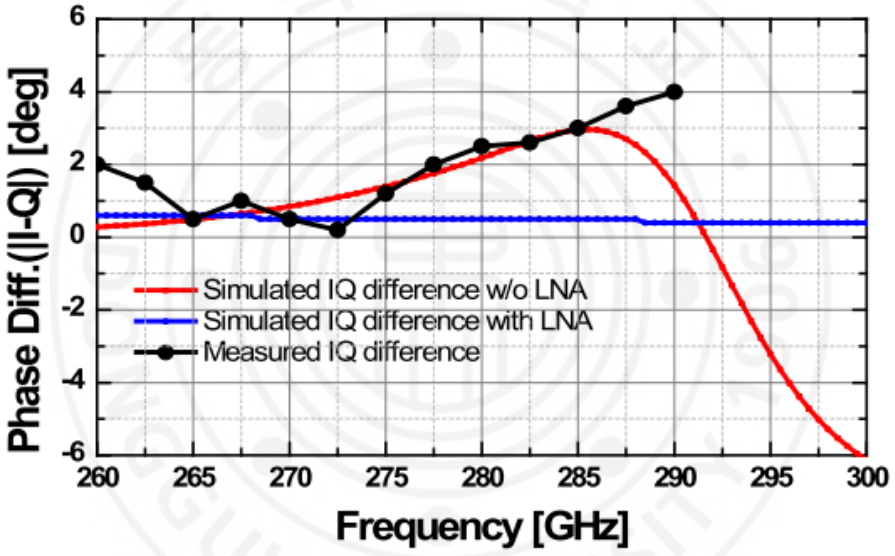


Figure 4.24 Comparison between measured and simulated I/Q phase mismatch.

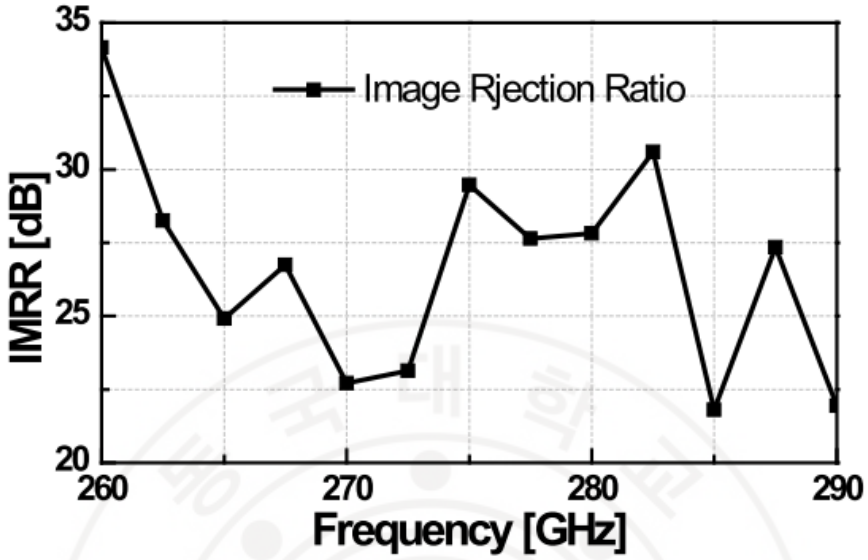


Figure 4.25 Calculated image rejection ratio of the mixer first receiver based on measured amplitude and phase mismatch.

4.4. Comparison With Previously Reported Sub-THz Receivers

Table 4.1 summarizes the performance of the proposed receivers and compares them with previously reported sub-THz receivers [4.3]-[4.6], [4.11]-[4.15]. The implemented receivers achieve peak conversion gains of 21.4 dB and 27.5 dB, IF bandwidth of 30 GHz, and minimum SSB noise figures of 22.3 dB and 20.1 dB, respectively. In addition, the proposed work integrates a complete 260 GHz quadrature LO chain and experimentally compares mixer first and LNA first receiver topologies within the same process and operating band.

Although some prior receivers report lower noise figure, the achieved 30 GHz IF bandwidth is particularly meaningful because it supports wideband quadrature demodulation and enables very-high-data-rate indoor sub-THz communication links. The measured quadrature balance and calculated image rejection ratio further indicate that the proposed receivers are suitable for high-order modulation formats in short-range 6G indoor network applications.

Table 4.1 Comparison with previously reported sub−THz Receivers

Ref.	This work		[4.3]	[4.4]	[4.5]	[4.6]	[4.18]	[4.19]
	(Rx1)	(Rx2)						
Modulation	16QAM/ 32QAM	16QAM/ 32QAM	QPSK	QPSK/16QAM/ 64QAM	16QAM	16QAM	QPSK/16QAM/ 32QAM	QPSK
Data rate (Gbps)	8/2.5	8/5	24	2.7 /0.7/1.0	80	100	28/32/20	16
Tech	130nm SiGe	130nm SiGe	130nm SiGe HBT	130nm SiGe bi−CMOS	40nm CMOS	130nm SiGe	40nm CMOS	65nm CMOS
Freq	265GHz	265GHz	240GHz	240GHz	265GHz	230GHz	290GHz	240GHz
Symbol rate (GBaud)	2/0.5	2/1	12	1.35/0.175/0.25	20	25	14/8/4	8
EVM	13.83%/ 7.44%	12.15%rms / 8.62%rms	24%	−	16.3%	17%	19%rms/ 12.2%rms/ 8.8%rms	−
Chip size	Rx : 1.418mm^2	Rx : 2.043mm^2	Rx : 1.522mm^2	Rx : 1.568mm^2	TRX : 11.05m m^2	−	RX : 3.15mm^2	RX : 2mm^2

4.5. Conclusion

This chapter has presented two 275 GHz quadrature receivers implemented in a 130−nm SiGe BiCMOS process for THz−band 6G indoor−network applications. The proposed receivers employ mixer first and LNA first front end organizations while sharing a common 260 GHz quadrature LO chain and broadband I/Q down conversion architecture.

To improve the down conversion performance in the sub−THz region, a modified Gilbert−cell mixer with swapped RF and LO ports was adopted, and a compact integrated LO chain consisting of an E−band driving amplifier, a frequency tripler, two 260 GHz driving amplifiers, and a differential hybrid coupler was codesigned. The measured results show that the mixer first and LNA first receivers achieve peak gains of 21.4 dB and 27.5 dB, minimum single−sideband noise figures of 22.3 dB and 20.1 dB, and 30 GHz IF bandwidth. The measured quadrature mismatch remains around 1 dB in amplitude and 4◦ in phase, and the calculated image rejection ratio reaches 34.2 dB at the best operating frequency.

The experimental comparison between the two receiver structures confirms that the LNA first architecture provides improved gain and sensitivity, whereas the mixer first architecture offers lower power dissipation and smaller area. Therefore, this work demonstrates not only a practical sub−THz quadrature receiver implementation, but

also an architecture level design trade-off relevant to future highly integrated broadband 6G frontends.

The circuit design of the 275-GHz quadrature receivers was primarily carried out by Van-Son Trinh, while the measurement, measured-data analysis, and performance comparison were conducted by the author. The results presented in this chapter have been published in IEEE Access and are detailed in [4.17].

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Chapter 5. A D-Band Transmitter

5.1. Introduction

Next-generation wireless communication systems require substantially higher data rates, lower latency, and wider RF bandwidths than existing millimeter-wave systems. To satisfy these requirements, the sub-terahertz spectrum has been actively explored as a key candidate for beyond-5G and 6G wireless links. In particular, the D-band around 130–150 GHz provides wide contiguous bandwidth and is attractive for high-capacity backhaul, fronthaul, and short-range point-to-point links. However, efficient and highly integrated D-band transmitters remain difficult to realize because the available transistor gain decreases rapidly and passive losses become severe as the operating frequency approaches the device fmax.

Bulk CMOS is attractive for large-scale integration because of its low cost, high digital compatibility, and mature manufacturing infrastructure. However, the limited maximum available gain and lossy on-chip passive components of bulk CMOS make it difficult to simultaneously achieve high output power and high power efficiency in the D-band. This limitation becomes more critical for spectrally efficient high-order modulation because high-PAPR signals such as 16-QAM typically require significant PA back-off in conventional linear transmitter architectures.

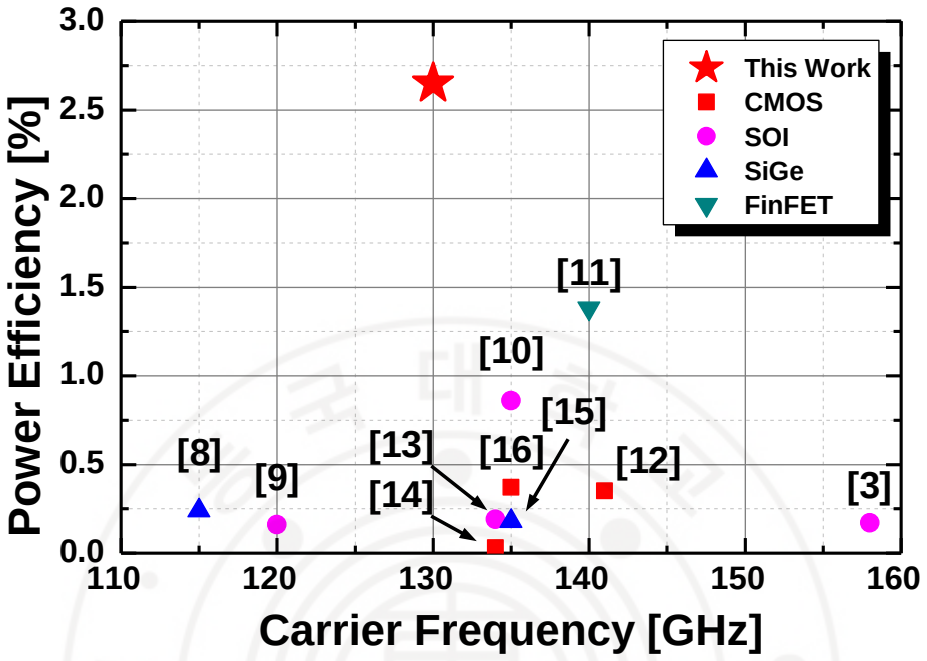


Figure 5.1 Power efficiency comparison with state-of-the-art transmitters versus carrier frequency.

RF-domain vector-synthesis and direct-modulation transmitter architectures address this system level limitation by synthesizing high-order constellations directly at RF from multiple phase- or amplitude-controlled vector components. Compared with a highly backed-off linear PA chain, this approach relaxes the linearity burden of each individual RF path and improves the effective modulated-output efficiency.

In this chapter, a 130-GHz 16-QAM transmitter implemented in 40-nm bulk CMOS is presented, with additional 16-QAM EVM

characterization at 140 GHz. The proposed transmitter employs an uneven-saturation dual-PA architecture in which two independent QPSK paths are designed to have a 6-dB saturated output power ratio. The two QPSK outputs are vector-combined in the RF domain to synthesize a 16-QAM constellation, while both PA paths operate close to saturation.

Figure 5.1 compares the modulated-output power efficiency of the proposed transmitter with previously reported D-band transmitters. The fabricated transmitter achieves a measured 16-QAM output power of 14 dBm with a power efficiency of 2.68% at 130 GHz. At 18 Gb/s, the measured EVMs are -21.62 dB at 130 GHz and -20.54 dB at 140 GHz. Owing to the uneven-saturation dual-PA architecture, this work achieves competitive modulated-output efficiency while maintaining high 16-QAM output power in a 40-nm bulk CMOS process.

The remainder of this chapter is organized as follows. Section 5.2 describes the proposed dual-QPSK-based 16-QAM transmitter architecture and analyzes the impact of inter-path group delay mismatch on wideband EVM. Section 5.3 presents the circuit implementation, including the power amplifiers, LO generation chain, quadrature coupler, mixers, intermediate pads, and output interface. Section 5.4 reports the measurement results of the fabricated transmitter. Finally, Section 5.5 concludes this chapter.

5.2. System Architecture and Wideband Phase error Analysis

5.2.1 Proposed dual-PA 16-QAM transmitter architecture

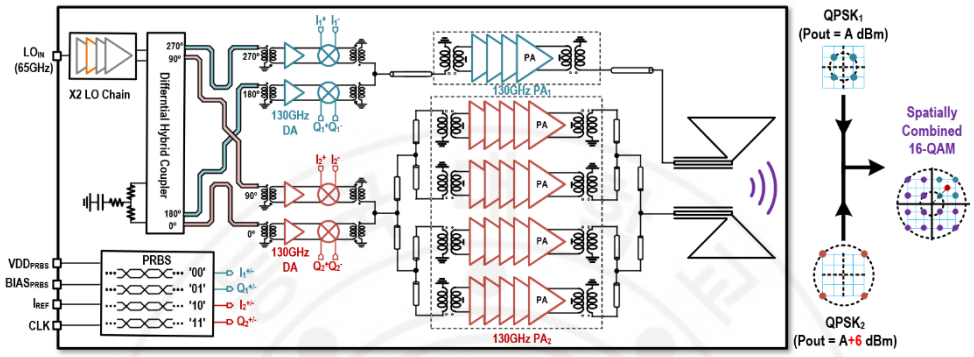


Figure 5.2 Block diagram of the proposed dual-PA transmitter architecture with 16-QAM modulation.

Figure 5.2 shows the block diagram of the proposed D-band transmitter. The architecture employs a frequency-multiplier-based LO generation stage, a quadrature distribution network, and two independent QPSK transmitter paths. A 65-GHz input signal is frequency-doubled to 130 GHz and then converted into differential I/Q LO signals through a quadrature coupler. These LO signals drive two separate up-conversion paths, and each path subsequently excites its own power amplifier. The two transmitter branches use similar unit-cell principles but are intentionally scaled in output power. Specifically, PA1 and PA2 are designed to exhibit a saturated output power difference of approximately 6 dB. The resulting QPSK outputs are then combined to realize a 16-QAM constellation.

The core idea is different from that of conventional single-PA transmitters and also from conventional RF-QAM transmitters using identical PA structures. In the proposed approach, the larger PA generates the dominant vector component and is allowed to operate close to saturation, whereas the smaller PA generates the lower-amplitude vector component needed to synthesize the multi-level amplitude states. Because the required amplitude ratio is built into the hardware itself, the transmitter can maintain high efficiency while still realizing 16-QAM modulation. This is the main architectural contribution of the chapter.

In the proposed implementation, PA2 is used as the high-power path and PA1 is used as the low-power path. To synthesize a square 16-QAM constellation, the two QPSK components require a 2:1 voltage-amplitude ratio, corresponding to a 6-dB output power ratio. Therefore, the proposed architecture requires not only the intended saturated output power ratio, but also accurate relative phase alignment between PA1 and PA2 over the occupied modulation bandwidth.

5.2.2 Group delay mismatch and wideband EVM model

In an ideal dual-QPSK-based 16-QAM transmitter, the final EVM is determined only by the individual QPSK EVMs when the two branches are perfectly phase-aligned. In practice, however, even when the two PA paths are aligned at the carrier frequency ω_0, each path exhibits its own frequency-dependent phase response because

of differences in gain, stage count, signal distribution, and embedding networks. As the signal bandwidth increases, the resulting phase dispersion produces residual phase error across the occupied RF spectrum, which degrades the combined 16-QAM EVM.

Let the phase response of the i^{th} PA path be $\phi_i(\omega)$. Its group delay is defined as

$$\tau_{g,i}(\omega) = -\frac{d\phi_i(\omega)}{d\omega} \tag{5.1}$$

The group delay mismatch between the two paths is then

$$\Delta\tau_g(\omega) = \tau_{g,2}(\omega) - \tau_{g,1}(\omega) \tag{5.2}$$

If the two paths are aligned at the carrier frequency, that is, $\phi_1(\omega_0) = \phi_2(\omega_0)$, then for a small offset $\Omega = \omega - \omega_0$, the phase of each path can be approximated by first-order Taylor expansion as

$$\phi_i(\omega_0 + \Omega) \approx \phi_1(\omega_0) - \tau_{g,i}(\omega_0)\Omega \tag{5.3}$$

Accordingly, the residual phase error between the two PA paths becomes

$$\Delta\phi(\omega_0 + \Omega) \approx -\Delta\tau_g(\omega_0)\Omega \tag{5.4}$$

This equation shows that even perfect center-frequency alignment does not guarantee wideband phase alignment. If a nonzero group

delay mismatch exists, the phase error grows linearly with frequency offset.

For a sufficiently small phase error, the instantaneous EVM is approximately proportional to the residual phase error,

$$EVM(\omega) \approx K_{\phi} \bullet \left| \Delta\phi(\omega) \right| \tag{5.5}$$

where K_{ϕ} is a normalization factor determined by the adopted EVM definition. In this dissertation, K_{ϕ} = 100%/(2π) is used for convenience. The RMS EVM over the occupied bandwidth can therefore be written as

$$EVM_{RMS} = K_{\phi} \sqrt{\frac{\int \left| \Delta\phi(f) \right|^2 S(f) df}{\int S(f) df}} \tag{5.6}$$

where S(f) denotes the RF spectrum of the transmitted 16-QAM signal. If $\Delta\tau_g$ is approximately constant across the occupied band, the RMS EVM becomes proportional to the product of group delay mismatch and signal bandwidth,

$$EVM_{RMS} \propto \left| \Delta\tau_g \right| \cdot B_{RMS} \tag{5.7}$$

This relation is the key design guideline of the chapter. It means that wideband 16-QAM performance is not determined only by

center–frequency phase matching; it is directly limited by the product of group delay mismatch and occupied bandwidth.

Behavioral simulations conducted in this study confirm this trend. For moderate values of $|\Delta \tau_g|$, the RMS EVM increases almost linearly with baud rate, and the deviation from linearity becomes noticeable only when the group delay mismatch becomes comparable to the symbol period. As shown in Figure 5.3, the RMS EVM increases almost linearly with baud rate as the group delay mismatch increases, which verifies that wideband EVM is directly limited by the product of group delay mismatch and signal bandwidth. Therefore, the dual–PA architecture requires not only amplitude scaling but also careful wideband phase equalization between PA1 and PA2.

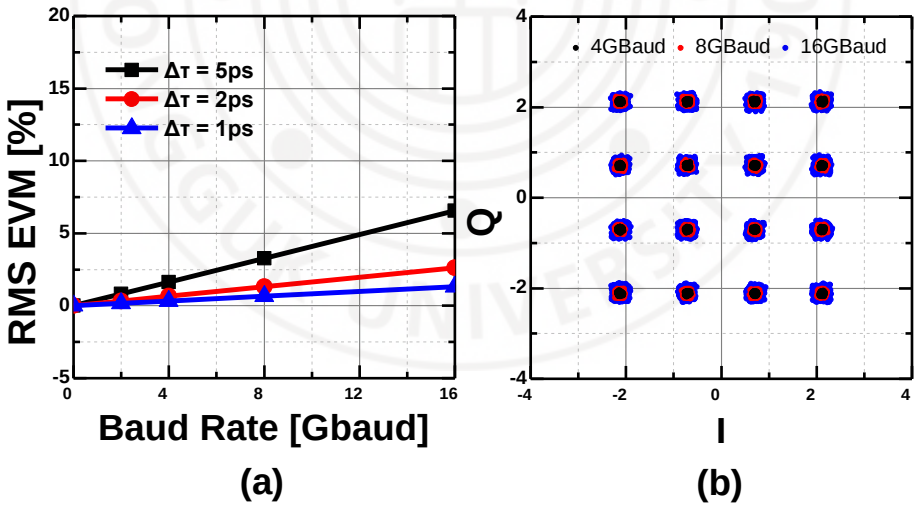


Figure 5.3 (a) Simulated RMS EVM versus baud rate for different constant group delay mismatches ($\Delta\tau_g$) (b) Constellation diagrams at various baud rates with $\Delta\tau_g$= 5 ps.

5.2.3 Design implication for dual-PA phase alignment

The practical meaning of the above analysis is straightforward. In a dual-PA 16-QAM transmitter, the two PA embedding networks and output combining paths must be co-designed so that the group delay mismatch remains sufficiently small over the occupied D-band spectrum. Otherwise, even if perfect phase alignment is achieved at the carrier frequency, the wideband EVM will degrade with increasing symbol rate. Therefore, the transmitter requires a phase-compensation mechanism that minimizes frequency dispersion rather than merely correcting the phase at a single frequency.

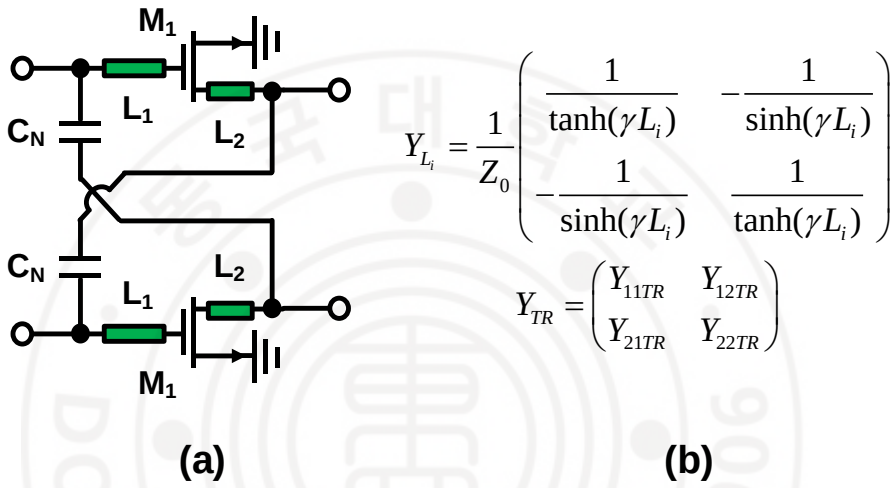
This requirement directly motivates the reversed-transformer phase-compensation method adopted in the proposed design, which is discussed in Section 5.3.2.

5.3. Circuit Design of the Proposed Transmitter

5.3.1 LLR-based wideband D-band power amplifier

At D-band frequencies, CMOS power-amplifier design is fundamentally limited by the rapidly falling available transistor gain near $f_{max}/2$ and by the significant loss of passive matching networks. In the proposed design, a wideband D-band PA is realized using an LLR-based embedding approach with dual-peaking G_{max} boosting. The primary design goal is to produce two gain peaks around 120 GHz and 160 GHz so that a wideband gain profile centered near 140

GHz can be obtained without sacrificing peak gain. A neutralization-based feedback network is used to implement this dual-peaking behavior, and the proposed G_{max} boosting structure together with its equivalent feedback-network model is shown in Figure 5.4.



$$Y_{L_i} = \frac{1}{Z_0}\begin{pmatrix} \frac{1}{\tanh(\gamma L_i)} & -\frac{1}{\sinh(\gamma L_i)} \\ -\frac{1}{\sinh(\gamma L_i)} & \frac{1}{\tanh(\gamma L_i)} \end{pmatrix}$$

$$Y_{TR} = \begin{pmatrix} Y_{11TR} & Y_{12TR} \\ Y_{21TR} & Y_{22TR} \end{pmatrix}$$

Figure 5.4 Proposed dual-peaking Gmax-boosting structure and equivalent feedback-network model.

With a properly designed feedback network represented by the LLR embedding network, the maximum achievable gain can be expressed as in [5.17]. When K = 1 and $\angle(Y_{21}/Y_{12}) = \pi$, G_{max} becomes 4U, where K denotes Rollett's stability factor and U denotes unilateral gain [5.17]. This G_{max} boosting technique can be achieved at two frequencies simultaneously by utilizing an appropriate embedding network. However, satisfying both conditions simultaneously is often not feasible, and the analysis in [5.18] shows

that G_{max} is more dependent on the K-factor than on the phase of the LLR structure. To achieve wideband performance, dual-peaking G_{max} boosting was targeted at 120 GHz and 160 GHz with a center frequency of 140 GHz. The proposed dual-peaking G_{max} boosting core and its equivalent Y-parameter can be modeled as in Figure 5.4 [5.19]. The Y-parameters of the LLR structure are derived using the coupled-line model and two-port formulation in [5.20], [5.21], which allows the calculation of G_{max} and the K-factor.

Theoretically, dual-peaking can be realized through various combinations of L_1, L_2, and C_n. However, in this design, L_2 was fixed because it is located on the drain side, where increasing its length would cause significant voltage drop and power loss, thereby degrading the overall PA performance. Keeping L_2 short minimizes these adverse effects and enables efficient power delivery to the output stage. Conversely, since C_n directly affects G_{max} and the K-factor, it requires dynamic adjustment rather than being fixed. Therefore, fixing L_2 rather than L_1 or C_n is the most reasonable choice for simplifying the design and optimizing power-transfer efficiency.

The intersection of the two contours shown in Figure 5.5 suggests the theoretical feasibility of dual-peaking boosting. However, practical implementation is challenging because when K equals unity, the real parts of the source and load admittances in the equivalent embedding network become zero, preventing effective power

transfer. Therefore, rather than strictly satisfying the theoretical condition, the design selects practical values of L_1 and C_n that maximize G_{max} at K values near unity.

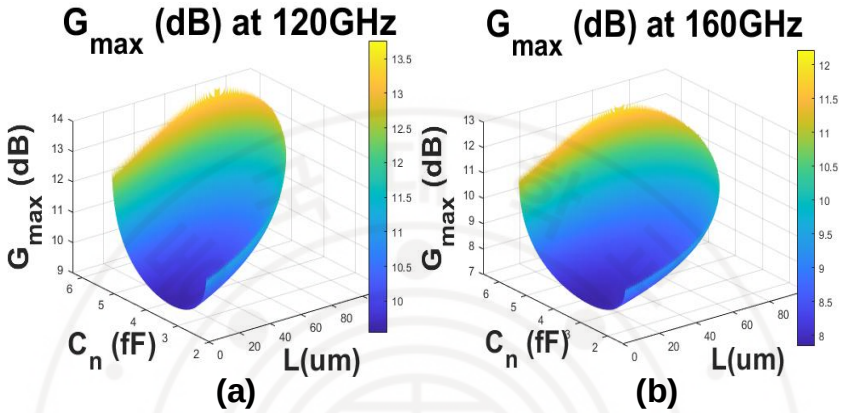


Figure 5.5 Simulated Gmax contours versus Cn and L1 at the two target frequencies.

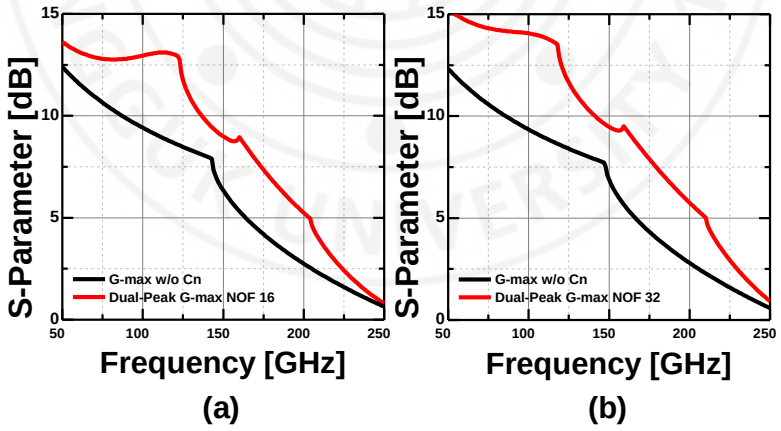


Figure 5.6 Simulated Gmax improvement using the dual-peaking technique for different transistor sizes.

Figure 5.6 presents the simulated G_{max} improvement for different transistor sizes using the selected component values. The proposed PA achieves approximately 2.5 dB higher small-signal gain at the center frequency compared with a conventional PA without neutralization capacitance. However, this technique is not applied to the output stage because excessive neutralization capacitance degrades the large-signal characteristics and consequently reduces output power and efficiency [5.22].

The output stage employs a cascaded balun exhibiting a flat intrinsic loss characteristic to overcome the narrowband limitation caused by the self-resonant frequency of conventional baluns in the 40-nm CMOS process, thereby ensuring broadband performance [5.23]. Figure 5.7 shows the schematic and layout of the proposed PA. To achieve high efficiency and broadband performance in the sub-THz band, the PA is designed using a transformer-coupled cascaded 2-way push-pull topology. PA1 and PA2 share the same unit-cell design principle to minimize phase and gain mismatches; however, PA1 targets approximately 6 dB lower saturated output power than PA2 and therefore employs one fewer gain stage to enhance power efficiency.

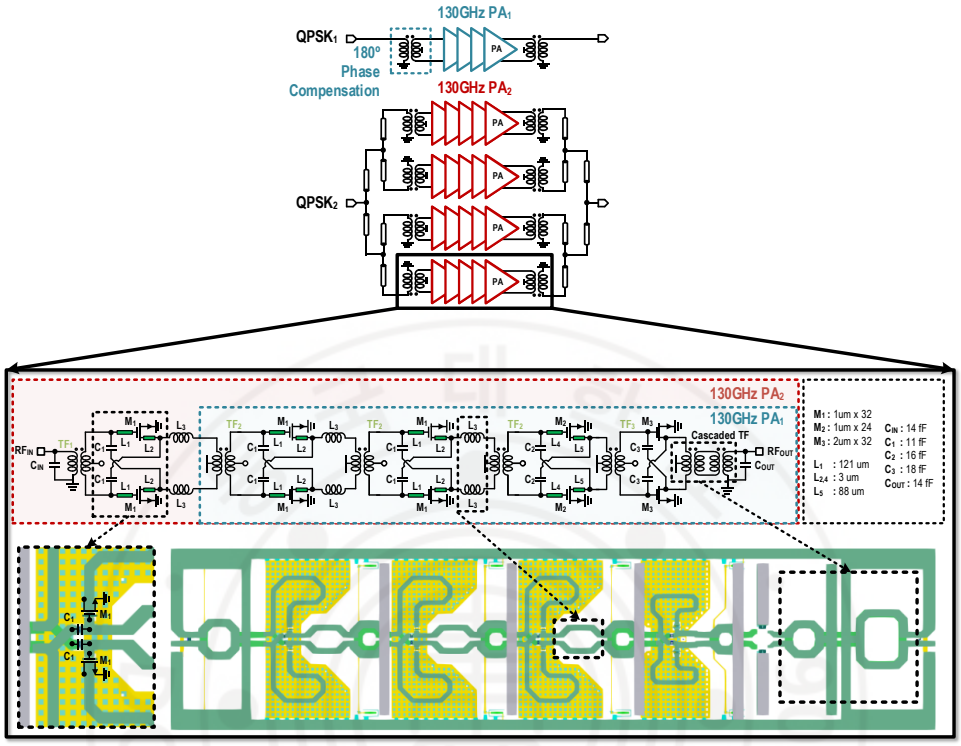


Figure 5.7 Schematic and layout of the proposed wideband D-band PA

5.3.2 Dual-PA amplitude scaling and phase equalization

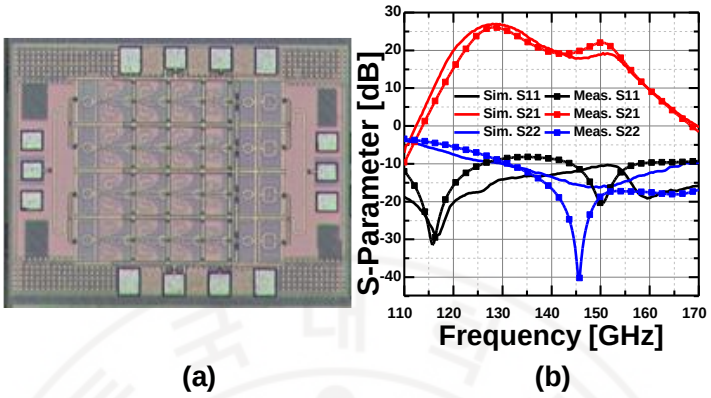


Figure 5.8 Fabricated standalone PA test structure and measured small-signal characteristics.

The proposed transmitter uses two amplifier paths with different output power capabilities. PA2 is the larger path and is designed for high saturated output power, whereas PA1 is designed to produce approximately 6 dB lower saturated output power. In this architecture, PA1 and PA2 share the same unit cell design principle, but PA1 uses one fewer gain stage to improve efficiency and realize the intended output power ratio. The fabricated standalone PA test structure and its measured small signal characteristics are shown in Figure 5.8, which verifies the gain behavior of the implemented PA before integration into the full transmitter.

The measured output power and power-added efficiency of the standalone PA are plotted in Figure 5.9. As shown in Figure 5.9, the implemented PA provides the output-power capability required for

the proposed dual-path transmitter architecture. However, the unequal stage count between PA1 and PA2 creates a phase-alignment problem. The larger PA path includes additional gain stages and signal-distribution structures, so a phase correction method is required to align PA1 and PA2 not only at the center frequency but also across the signal bandwidth.

A conventional transmission-line compensation method is not sufficient because a TL-based 180° phase shift is inherently dispersive. Even if it gives exact 180° correction at the center frequency, its phase deviation grows with frequency offset and therefore worsens the $|\Delta \tau_g| \cdot B$ limitation discussed in Section 5.2. The concept of the proposed 180° phase compensation is illustrated in Figure 5.10. Instead of using an electrically long transmission-line-based phase correction, the proposed design employs transformer reversal to suppress additional phase dispersion. Figure 5.11 shows the simulated output power and phase relations between PA1 and PA2 over frequency. The results confirm that the intended amplitude ratio is maintained while the residual phase mismatch remains sufficiently small over the operating band.

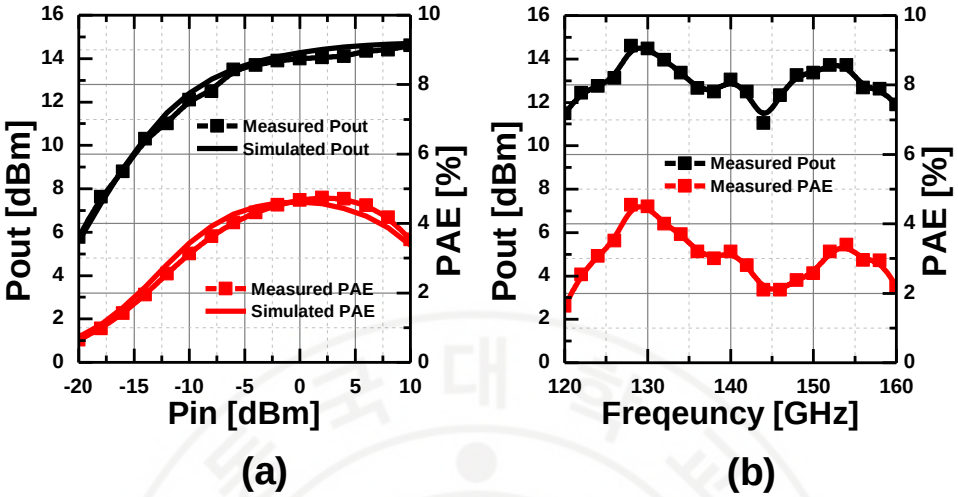


Figure 5.9 Measured output power and PAE of the standalone PA versus input power and frequency.

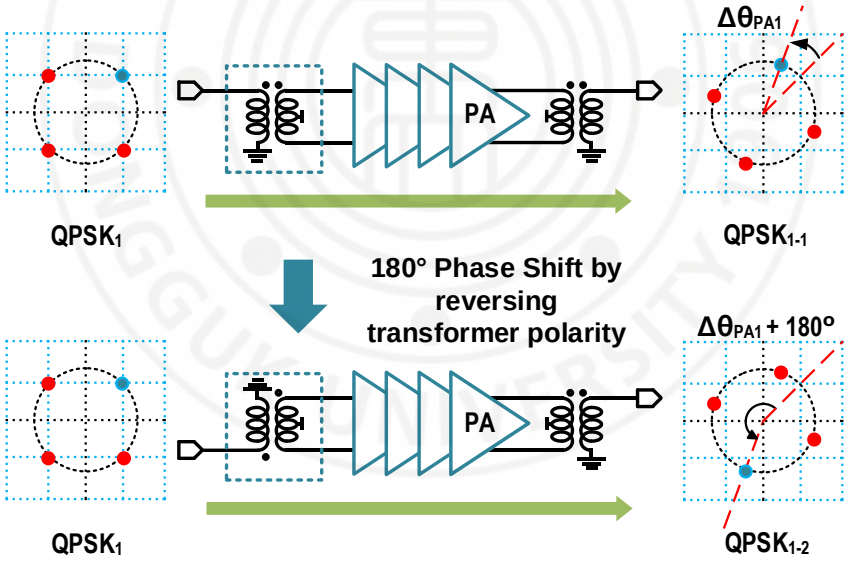


Figure 5.10 Conceptual illustration of 180° phase compensation using the reversed-transformer configuration.

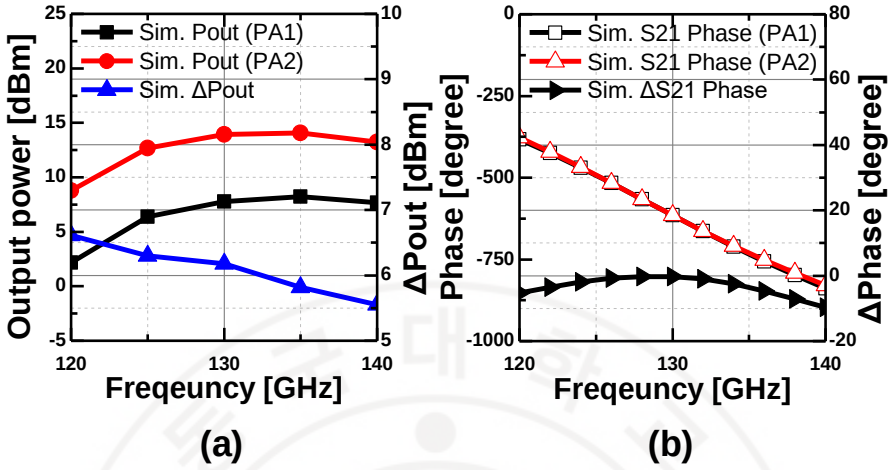


Figure 5.11 Simulated output-power and phase relations between PA1 and PA2 over frequency.

5.3.3 LO generator and driver amplifier

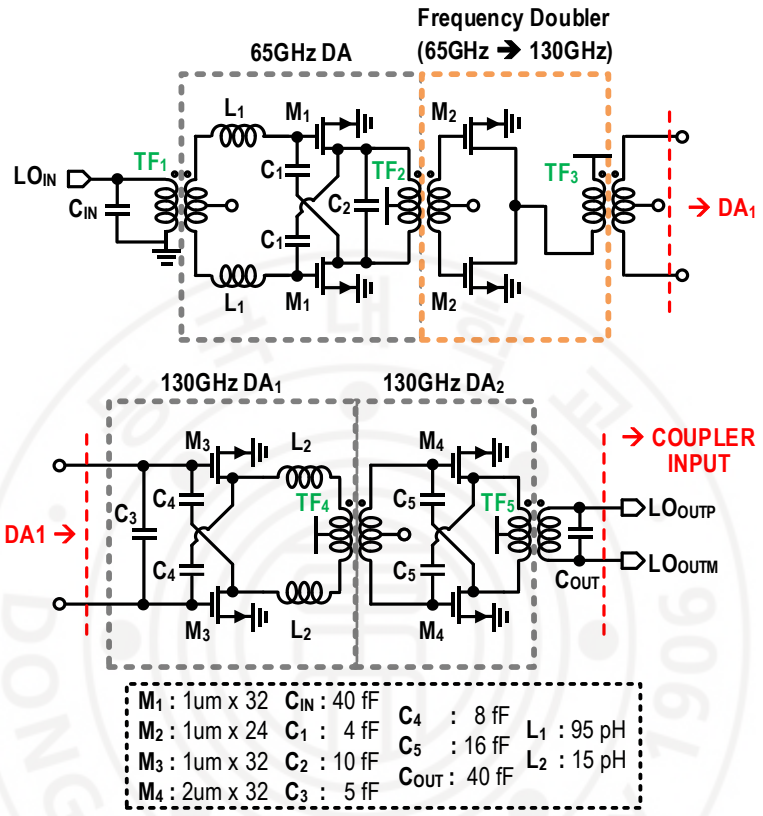


Figure 5.12 Schematic of the LO generator and driver-amplifier chain.

The LO path begins with a 65-GHz input signal and employs a frequency-doubling architecture to generate the 130-GHz LO required by the up-conversion mixers. Because the transmitter targets 16-QAM operation, LO phase error must be tightly controlled. For this reason, the design uses a push-push frequency doubler, whose differential structure suppresses fundamental-frequency

leakage and common-mode noise. The schematic of the LO generator and driver-amplifier chain is shown in Figure 5.12. The LO path further employs saturated driver stages to provide stable quadrature LO signals for the up-conversion mixers.

A notable point in the LO architecture is that the pre-coupler driver amplifier is intentionally driven into deep saturation and thus behaves as a limiter. This makes the LO envelope more constant before quadrature splitting and helps reduce AM-to-PM conversion in the post-coupler driver amplifiers. As a result, the final LO signals delivered to the mixers achieve improved phase consistency, which is important for high-order modulation accuracy. Figure 5.13 presents the simulated performance of the frequency doubler, including output power, efficiency, and harmonic suppression. These results confirm that the LO chain can provide sufficient drive level for the subsequent stages.

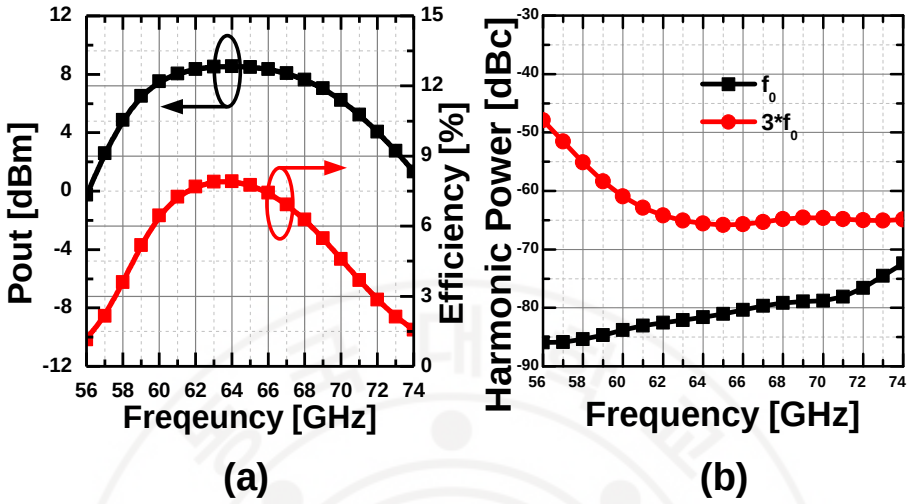


Figure 5.13 Simulated frequency-doubler performance, including output power, efficiency, and harmonic suppression.

5.3.4 Quadrature coupler

To divide the 130-GHz LO into accurate I and Q signals, the design employs a coupled-line-based differential hybrid coupler rather than a conventional quarter-wave branch-line coupler. The main advantage is reduced area and lower insertion loss, since the required coupled-line sections can be made relatively short at the target frequency. All line lengths are carefully matched to minimize amplitude imbalance and phase error between the I and Q LO paths. The layout and simulated amplitude/phase characteristics of the differential hybrid coupler are shown in Figure 5.14. The coupler is

designed to minimize amplitude imbalance and phase error between the I and Q LO paths over the target D-band range.

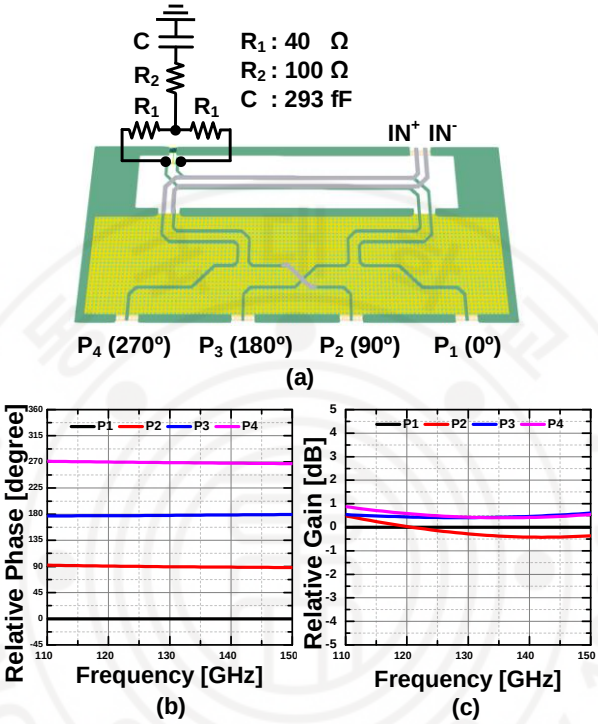


Figure 5.14 Layout and simulated amplitude/phase characteristics of the differential hybrid coupler.

5.3.5 Up-conversion mixer

The up-conversion mixer uses a double-balanced Gilbert-cell topology. This fully differential structure is chosen to suppress even-order distortion and LO leakage. An on-chip transformer is integrated at the mixer load to perform differential-to-single-ended conversion and impedance matching at the RF output. The transistor sizes and bias conditions are optimized to maximize conversion

performance in the D-band. Figure 5.15 shows the implemented D-band up-conversion mixer together with its simulated output power and LO leakage. The double-balanced structure suppresses even-order distortion and provides adequate LO isolation for high-order modulation.

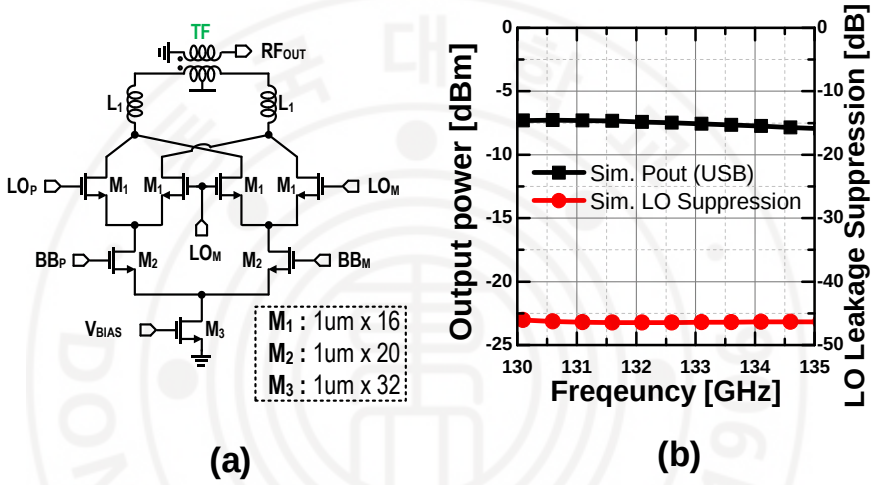


Figure 5.15 Implemented D-band up-conversion mixer: (a) circuit schematic and (b) simulated output power and LO leakage.

5.3.6 Intermediate pad structure for individual QPSK-path characterization

The transmitter was fabricated in two forms: one pad-based version for direct probing and verification of the individual-PA outputs, and one antenna-integrated version. In the probing version, the outputs of the two PA paths are combined by a Wilkinson combiner. Because the Wilkinson structure makes independent

measurement of one PA difficult when the other path is inactive, intermediate pads are introduced before the combiner so that the individual QPSK outputs of PA1 and PA2 can be separately characterized. The output combiner with intermediate pads and the corresponding simulated insertion loss comparison are shown in Figure 5.16. As shown in Figure 5.16, the intermediate-pad structure allows independent characterization of PA1 and PA2 while introducing only a limited insertion loss penalty.

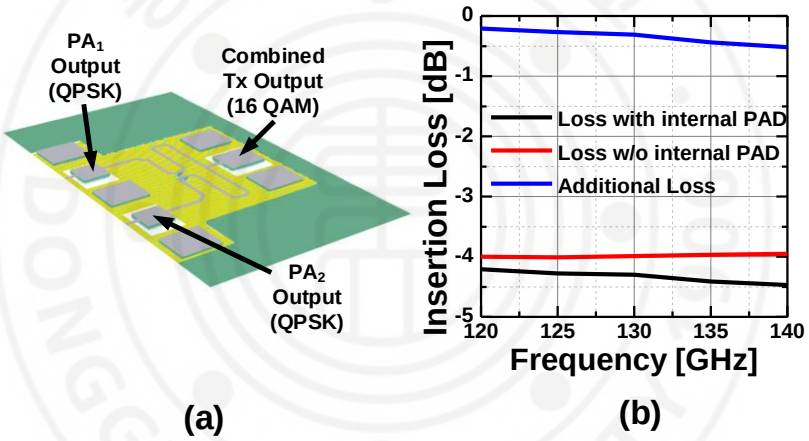


Figure 5.16 Output combiner with intermediate pads and simulated insertion loss comparison.

5.3.7 On-chip bowtie antenna

For the antenna-integrated version, the design adopts an on-chip bowtie antenna. At frequencies above 100 GHz, direct wire-bonded output interfaces suffer from severe insertion loss due to parasitic inductance and dielectric loss. Antenna-in-package solutions can

alleviate this problem but require more complex and costly packaging technology. Helical on-chip antennas provide an alternative, but they require vertical interconnect structures across many metal layers and are sensitive to parasitic capacitance and process variation. The bowtie antenna is chosen here because its planar geometry is simpler, more robust in CMOS, and more suitable for wideband operation.

Figure 5.17 shows the layout of the proposed on-chip bowtie antenna and the cross-sectional view with the silicon lens. The planar bowtie structure is adopted to achieve robust wideband radiation in a CMOS-compatible form. Because a shieldless on-chip antenna tends to radiate most of its power into the silicon substrate, a silicon lens is used to redirect radiation toward the backside and improve radiation efficiency. The simulated radiation characteristics of the proposed on-chip bowtie antenna are summarized in Figure 5.18, which verifies the suitability of the antenna for the intended D-band transmitter implementation.

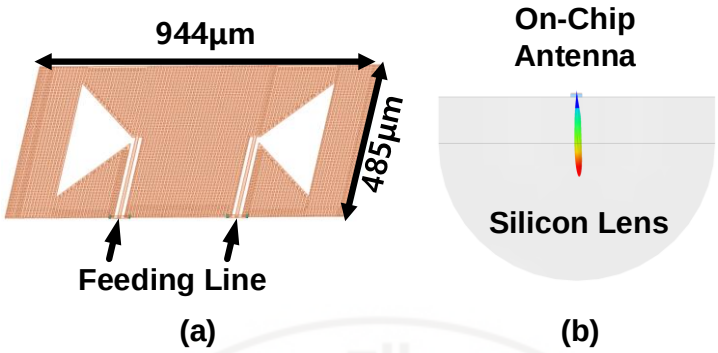


Figure 5.17 Layout of the proposed on-chip bowtie antenna and cross-sectional view with silicon lens.

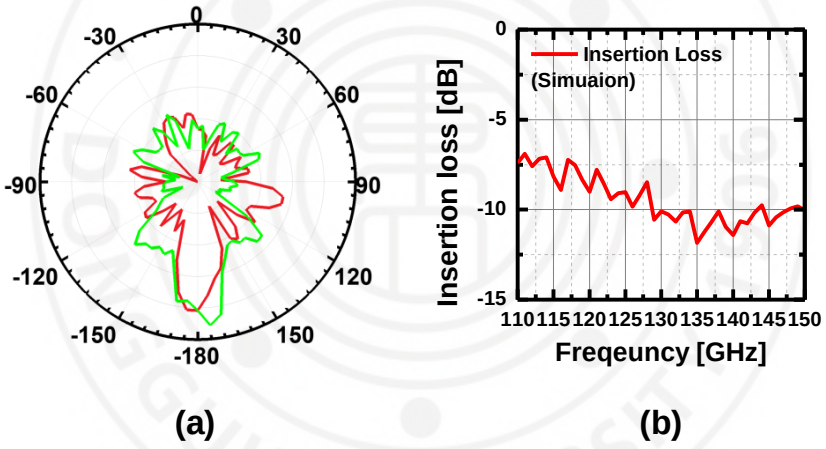


Figure 5.18 Simulated radiation patterns and insertion loss of the proposed on-chip bowtie antenna.

5.4. Measurement Results

5.4.1 Bare-chip measurement results

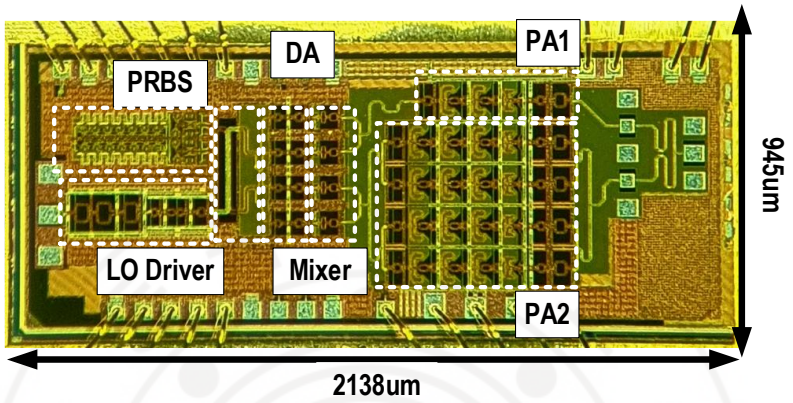


Figure 5.19 Chip micrograph of the fully integrated D-band transmitter.

The chip micrograph of the fabricated D-band transmitter is shown in Figure 5.19. The prototype includes RF/DC pads, a PRBS generator, and additional verification pads for individual-PA-path characterization. Bare-chip characterization was performed using on-chip probing, and Figure 5.20 shows the measurement setup used for bare-chip on-wafer characterization. The setup includes the probing environment and the instruments required for D-band modulated-signal verification.

The measured output powers of PA1 and PA2 versus frequency are plotted in Figure 5.21. As shown in Figure 5.21, the intended output-power difference between the two PA paths is successfully

realized in silicon. At 130 GHz, PA1 and PA2 achieve measured output powers of 7.96 dBm and 14.47 dBm, respectively, corresponding to a power difference of 6.51 dB. Figure 5.22 shows the measured QPSK constellation diagrams of the individual–PA1 and PA2 paths. The measured results confirm that both branches maintain sufficient modulation quality before vector combination.

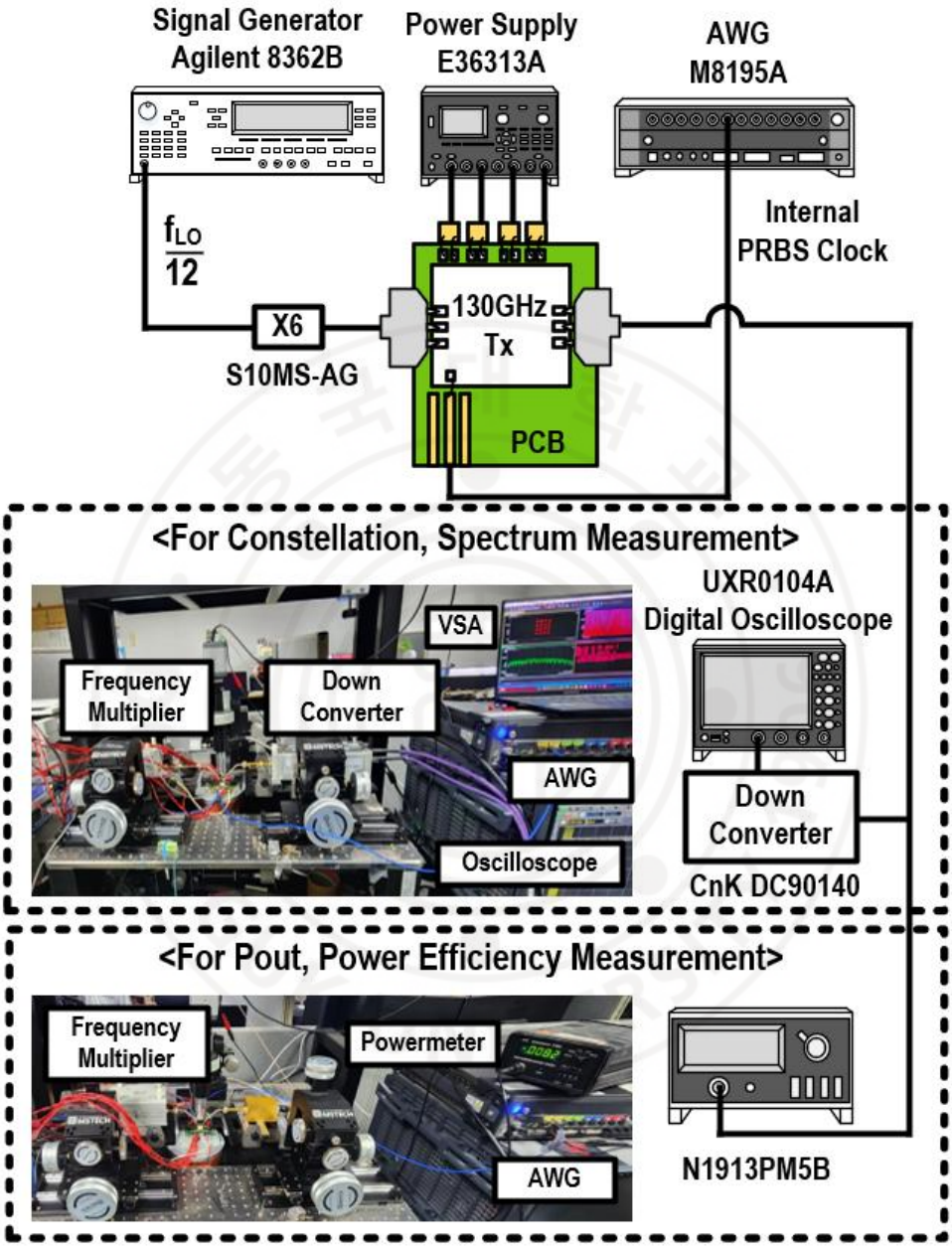


Figure 5.20 Measurement setup for bare-chip on-wafer characterization.

The measured output power, modulated power efficiency, and output return loss of the fully integrated transmitter are summarized in Figure 5.23. These results verify the effectiveness of the proposed architecture in improving transmitter efficiency at D-band. Under a 1-V supply with a total current consumption of 938 mA, the transmitter achieves an average output power of approximately 14 dBm and a modulated power efficiency of 2.68% when transmitting 16-QAM. The measured 16-QAM constellation diagrams at 130 GHz and 140 GHz are shown in Figure 5.24. The measured EVM results confirm that the proposed transmitter maintains acceptable modulation accuracy up to the highest tested symbol rate.

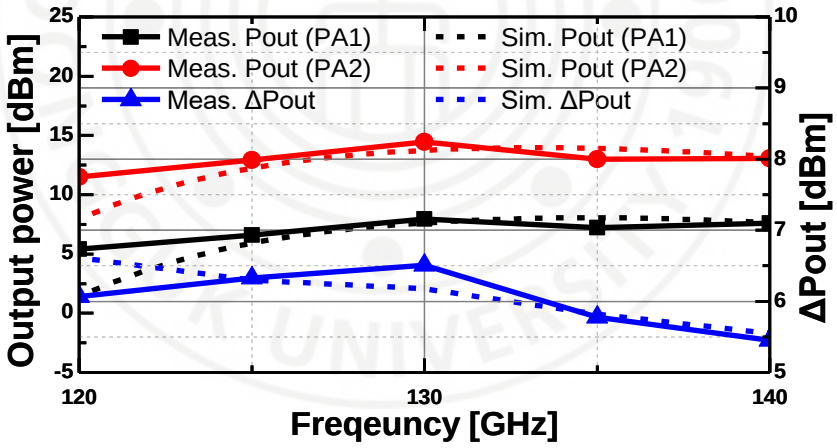


Figure 5.21 Measured output powers of individual-PA1 and PA2 versus frequency.

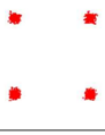
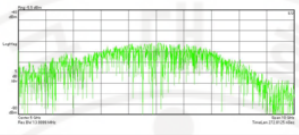
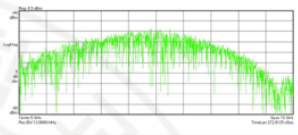
	Sub QPSK	
	PA1	PA2
Modulation	QPSK	QPSK
Data Rate	9Gb/s	9Gb/s
Constellation		
Spectrum		
EVM	-23.22 dB	-23.61 dB

Figure 5.22 Measured QPSK constellation diagrams of individual-PA1 and PA2.

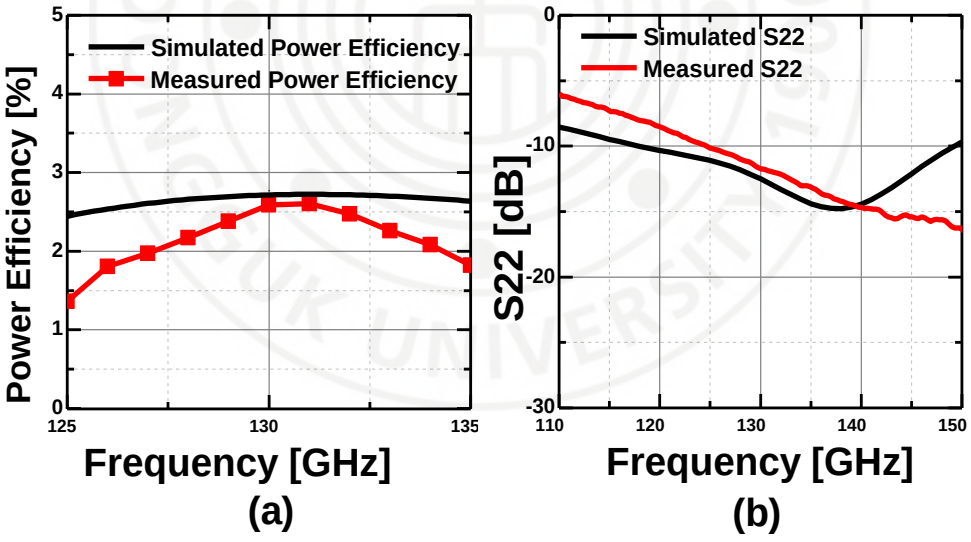
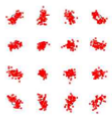
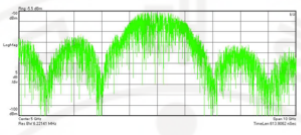
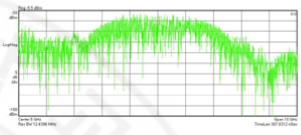


Figure 5.23 Measured output power, power efficiency, and output return loss of the fully integrated transmitter.

	RF Frequency	
	130GHz	130GHz
Modulation	16 QAM	16 QAM
Data Rate	4Gb/s	16Gb/s
Constellation		
Spectrum		
EVM	-28.11 dB	-22.59 dB

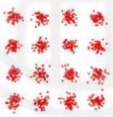
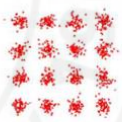
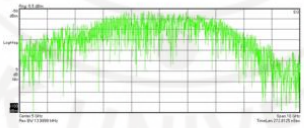
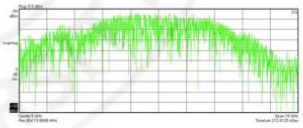
	RF Frequency	
	130GHz	140GHz
Modulation	16 QAM	16 QAM
Data Rate	18Gb/s	18Gb/s
Constellation		
Spectrum		
EVM	-21.62 dB	-20.54 dB

Figure 5.24 Measured 16-QAM constellation diagrams of the fully integrated transmitter at 130 GHz and 140 GHz.

5.4.2 Antenna measurement results

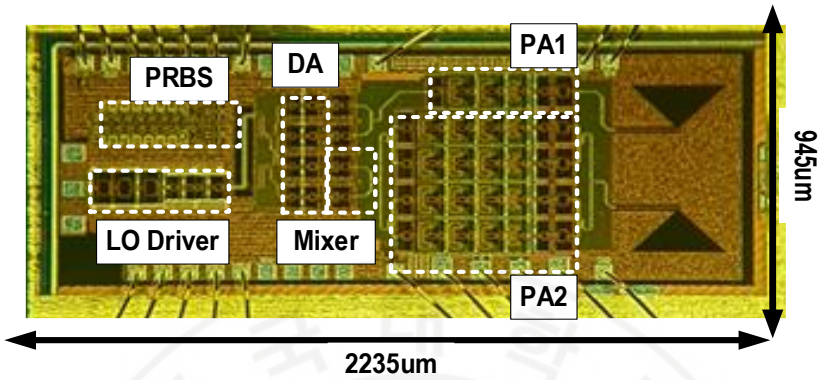


Figure 5.25 Chip micrograph of the antenna-integrated transmitter.

In addition to the pad-based transmitter version, an antenna-integrated version was fabricated to evaluate the radiation characteristics of the on-chip antenna and backside-radiation structure. The antenna-version chip micrograph is presented in Figure 5.25. Unlike the pad-based version, this chip does not provide a direct RF probing path for the antenna output. Therefore, the antenna-version measurement focuses on verifying the radiation interface rather than extracting the conducted transmitter output power and efficiency.

The transition and feeding structure used for the antenna-version measurement is shown in Figure 5.26, and the antenna measurement

setup is shown in Figure 5.27. In the antenna-integrated version, the LO signal is supplied through the WR-8 input transition, and the generated 130-GHz RF signal is radiated by the on-chip bowtie antenna through the backside silicon lens. The measured E- and H-plane radiation characteristics are shown in Figure 5.28. The measured patterns show directional backside radiation from the antenna-integrated version, which is consistent with the design intention of using a silicon lens to redirect the dominant substrate-side radiation.

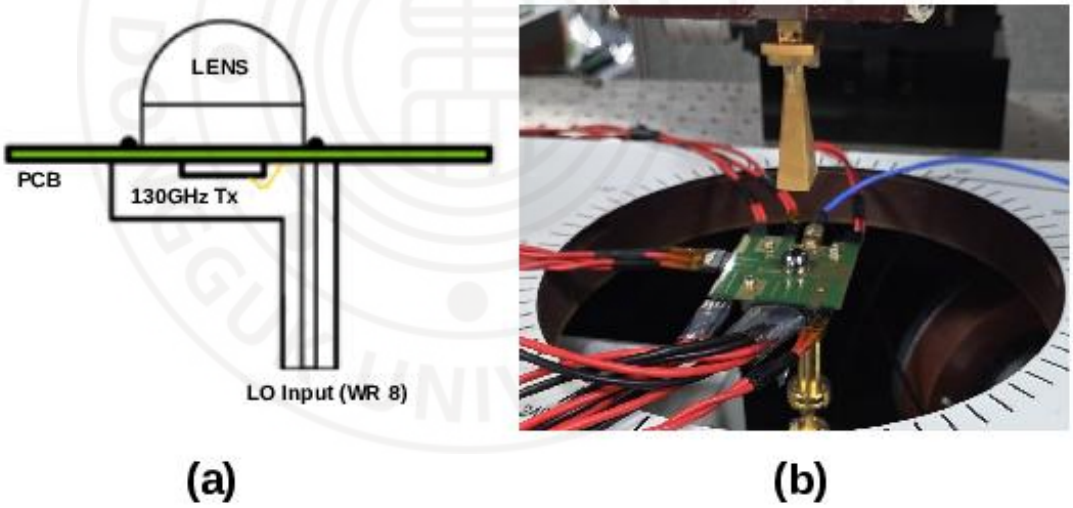


Figure 5.26 Transition and feeding structure for antenna-version measurement.

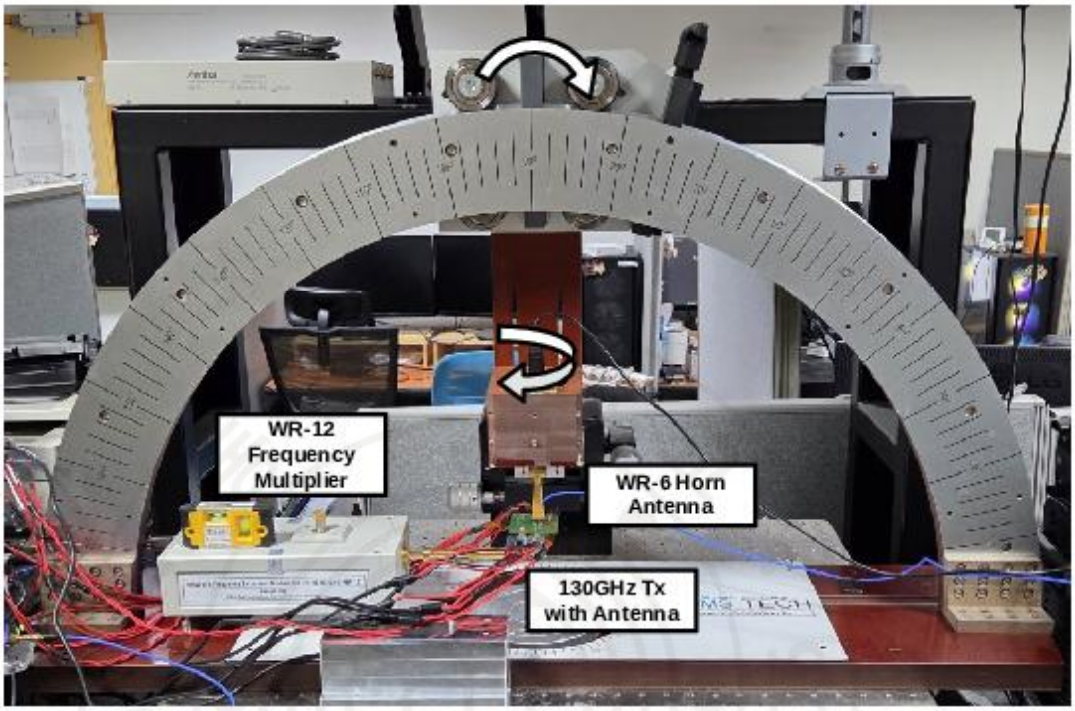


Figure 5.27 Measurement setup for antenna characterization.

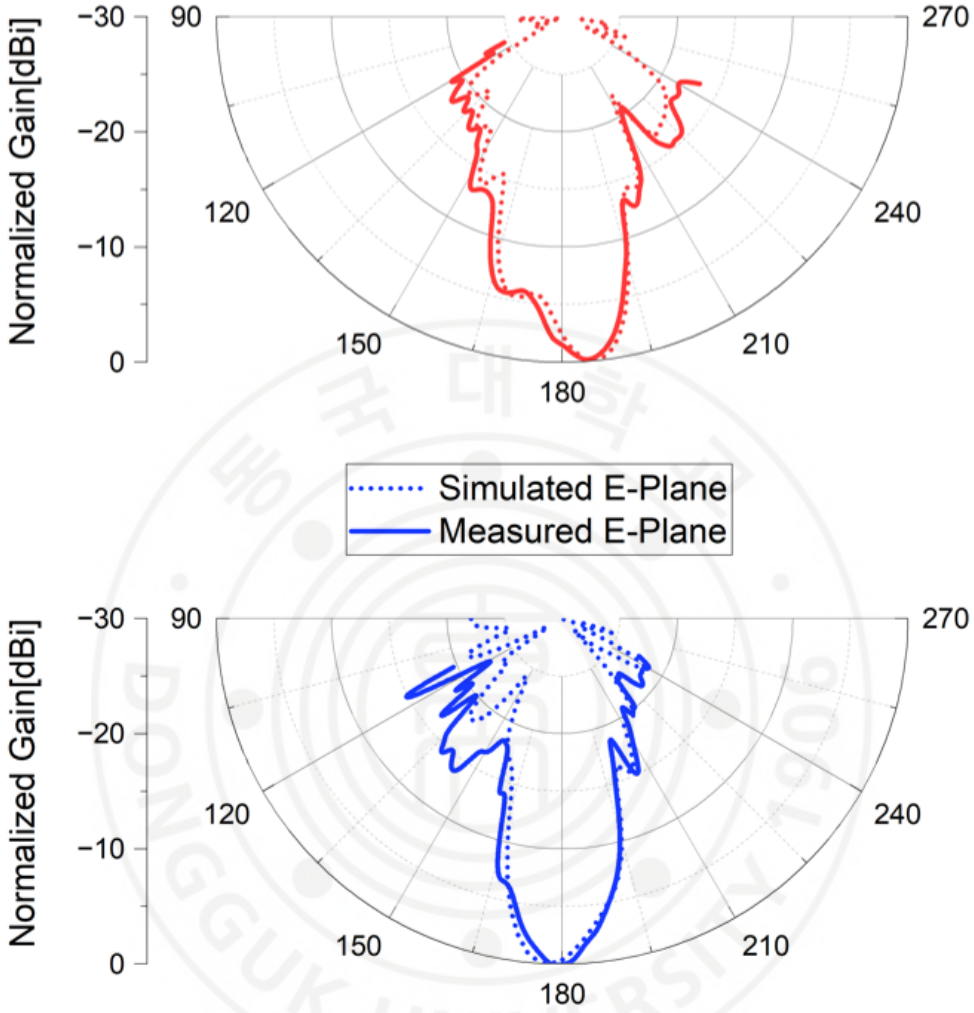


Figure 5.28 Measured E- and H-plane radiation characteristics of the antenna-integrated transmitter.

5.4.3 Comparison with previously reported D-band transmitters

Table 5.1 compares the proposed transmitter with previously reported D-band and nearby sub-THz transmitters. The proposed work achieves 14 dBm output power, an 18 Gb/s data rate, an EVM of −21.6 dB, 938 mW DC power consumption, and 2.68% modulated power efficiency. Compared with previously reported works in the cited comparison set, the proposed transmitter exhibits the highest modulated power efficiency while maintaining relatively high output power. These results confirm that the uneven-saturation dual-PA architecture is effective for realizing high-order modulation with improved efficiency in CMOS D-band transmitters.

Table 5.1 Comparison of State-of-the-Art Transmitter Around the D-band.

Ref.	This work COB/ Antenna	[5.3]	[5.8]	[5.9]	[5.12]	[5.13]	[5.14]	[5.15]	[5.16]	[5.24]	[5.25]
Tech	40nm CMOS	45nm RFSOI	180nm SiGe	45nm SOI	22nm FinFET	28nm CMOS	22nm FDSOI	22nm CMOS	130nm SiGe	22nm FDSOI	28nm CMOS
Carrier Frequency [GHz]	130	140-158	115	120	140	141	131-137	134	115-155/ 135-170	120-145	135
Output Power [dBm]	14	11-16*	1	1.4	0.8	13.1 7.5	1.95	-5	13dBm (Psat)	11/ 7.5	0
Modulation	16QAM	16QAM/ 64QAM	16QAM	64QAM	QPSK/ 16QAM	QPSK/ 16QAM	QPSK/ 16QAM/ 64QAM	QPSK/ 16QAM	512QAM/ 256 QAM/ 128QAM/ 64QAM	16QAM/ 64QAM	16QAM
Data Rate [Gbps]	18	56.32/ 48	20	120	80/ 160	24/ 48	4/ 4/ 2.5	28/ 56	36(64)/ 9(512)	56/ 30	32
EVM [dB]	-21.6	-14.0/ -20.0	-15.8	-18.6	-17.3/ -17.1	-15/ -15.5	-22.1/ -20.7/ -22.6	-16.5/ -18.4	-23.0/ -30.0	-17/ -25	-18
PDC [mW]	938	600	520	880	173	706/ 746	210	273	1350/ 2100	232	264
Modulated Output Power [dBm]	14	0††	1	1.4	3.8	4	-4.0 (16-QAM)	-11†††	4 (256 QAM)	3 (16-QAM)	0
Power Efficiency @ Modulation [%]	2.68	0.17	0.24	0.16	1.38	0.35	0.19	0.03	0.18	0.86	0.37

*with antenna gain(7.7 dB) and insertion loss
†Estimation from 6dB backoff
††Calculated from Tx input
†††Estimation from 6dB backoff

5.5. Conclusion

This chapter has presented a D-band 16-QAM transmitter implemented in 40-nm bulk CMOS using an uneven-saturation dual-PA architecture. The key idea is to synthesize 16-QAM by combining two phase aligned QPSK branches with an intentionally designed output power ratio of approximately 6 dB. Through this structure, the higher power PA can operate near saturation while the lower power PA provides the smaller vector component needed for higher order modulation, thereby improving modulated power efficiency in CMOS at D-band.

To support this architecture, the chapter also analyzed the effect of group delay mismatch on wideband EVM and showed that the EVM scales approximately with $|\Delta \tau_g| \cdot B$. Based on this understanding, a reversed-transformer phase-compensation method was adopted to correct the phase difference caused by unequal PA stage counts while avoiding the dispersive behavior of conventional transmission line based 180° correction. In addition, the transmitter incorporates an LLR based wideband D-band PA with dual-peaking Gmax boosting, a frequency doubled LO chain, a compact quadrature coupler, a double balanced up conversion mixer, and an optional on-chip bowtie antenna with silicon-lens-assisted backside radiation.

The PRBS block for testing was implemented with the assistance of Jun-Hee Lee, the QPSK coupler structure was revised with contributions from Sun-Hyeok Kwon, the PA2 block was designed

by Min-Gyun Kim, and the on-chip antenna and silicon-lens structure were developed by Tae-Hoon Kim. The block level modifications, overall transmitter integration, measurement, and data analysis were carried out by the author.

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Chapter 6. Conclusion

This dissertation has presented a systematic design framework for CMOS-based RF beamforming frontends spanning from X-band to sub-THz and D-band frequencies for next-generation 6G communication systems. Rather than focusing on a single circuit block, this work addressed the beamforming-frontend problem through a continuous progression of topics: accurate wideband signal alignment, multifunction frontend integration, high-frequency receiver architecture, and high-efficiency transmitter design. In this sense, the dissertation has organized the essential challenges of RF beamforming frontends along the three axes of signal control, frontend integration, and frequency scaling.

First, this work addressed the problem of beam squint and delay inaccuracy in wideband beamforming systems through the design of a passive true-time delay circuit. The proposed 5–11 GHz 8-bit precision passive TTD employed a hierarchical structure in which the lower bits used a precision delay architecture based on two LC delay networks in parallel, while the upper bits used conventional LC-based delay cells for coarse delay generation. Through this approach, the circuit achieved a minimum delay step of 1.56 ps and a maximum delay range of 400 ps without DC power consumption. The measured results verified better than 10 dB input and output return losses over 5–11 GHz, reduced insertion loss variation, an IP1dB of 11.2 dBm, RMS phase error below 5.2◦, and RMS delay error below 4.5 ps.

These results confirmed that accurate wideband delay alignment can be practically realized in CMOS and that true-time delay is an effective circuit level solution for broadband beamforming frontends.

Second, this dissertation extended the signal-alignment problem to the level of a practical RF frontend by presenting an X-band multifunction chip integrating phase shifting, attenuation control, amplification, and Tx/Rx switching in a single CMOS chip. The key idea of the proposed MFC was a hybrid passive phase shifter in which TTD cells were used for the lower bits and filter-based phase-shifter cells were used for the higher bits, thereby reducing mismatch-induced phase distortion while keeping the chip compact. The chip also integrated a 6-bit attenuator, transformer-based LNA and PA, SPI control, and path-preserving switching networks. The COB measurements verified an RMS phase error of 3.33°, RMS attenuation error of 0.31 dB, Tx OP1dB of 9.51 dBm, and receive noise figure below 16.2 dB over the 8–10 GHz band. After QFN packaging, the degradation remained minimal, with packaged RMS phase error of 3.5°, gain error below 0.39 dB, and receive noise figure below 16.8 dB. Compared with previously reported X-band MFCs of similar topology, the proposed design achieved very competitive integration density, low power consumption, and strong packaging robustness. Therefore, Chapter 3 demonstrated that accurate beamforming control can be extended from a standalone

delay element to a compact and practically deployable multifunction frontend.

Third, as the operating frequency was extended into the sub-THz region, this dissertation investigated how the dominant design criteria shift from phase control toward gain, noise figure, bandwidth, and LO generation. To this end, two 275 GHz quadrature receivers implemented in 130-nm SiGe BiCMOS were presented: a mixer first receiver and an LNA first receiver. Both architectures integrated a compact 260 GHz quadrature LO chain and achieved direct-conversion I/Q reception over a wide IF bandwidth. The measured results showed peak gains of 21.4 dB and 27.5 dB, minimum single-sideband noise figures of 22.3 dB and 20.1 dB, and IF bandwidths exceeding 30 GHz. In addition, the measured amplitude and phase mismatches were around 1 dB and 4°, and the calculated image rejection ratio reached 34.2 dB at the best operating point. The comparison between the two architectures clearly showed that the LNA first receiver improved sensitivity and gain, whereas the mixer first receiver offered lower power and smaller chip area. Thus, Chapter 4 demonstrated that in the sub-THz regime, receiver design must be understood not only as a device-limited problem but also as an architecture level trade-off among sensitivity, area, and power dissipation.

Finally, this dissertation addressed the efficiency bottleneck of CMOS transmitters in the D-band by proposing a 16-QAM

transmitter based on an uneven-saturation dual-PA architecture. Unlike conventional RF-QAM transmitters using identical amplifier structures, the proposed architecture employed two independent QPSK paths with an intentionally designed 6-dB saturated output-power difference. This allowed the higher-power PA to operate close to saturation while the lower-power PA generated the smaller-amplitude vector component needed to realize 16-QAM, thereby improving modulated power efficiency without sacrificing constellation quality. In addition, the dissertation analyzed the relationship between group delay mismatch and wideband EVM and showed that the EVM scales approximately with the product of group delay mismatch and signal bandwidth. Based on this analysis, a reversed-transformer phase-compensation method was adopted to suppress the 180° phase difference caused by stage-count asymmetry between the two PA paths. The fabricated 40-nm CMOS transmitter achieved approximately 14 dBm output power, 2.68% modulated power efficiency, and an EVM of −21.6 dB at 4.5 Gbaud. These results confirmed that even in CMOS, a D-band transmitter can simultaneously achieve meaningful output power, acceptable 16-QAM linearity, and state-of-the-art modulated efficiency when the architecture is optimized for saturation-mode vector synthesis rather than conventional backed-off linear amplification.

Taken together, the results of this dissertation lead to the following overall conclusion. In future 6G beamforming frontends, the key

design challenge is not the isolated optimization of a single RF block, but the consistent realization of signal alignment, amplitude/phase controllability, bandwidth preservation, and efficiency across a wide frequency span. The presented TTD, X-band MFC, sub-THz receiver, and D-band transmitter show that CMOS-based beamforming frontends can remain practical and scalable even as the operating frequency extends from microwave to sub-THz bands, provided that the circuit architecture is chosen according to the dominant limitation of each frequency range. At lower frequencies, accurate delay and multifunction integration are the primary concerns; at higher frequencies, receiver gain/noise and transmitter efficiency/phase alignment become dominant. This dissertation has shown that these apparently different problems can be understood within one continuous frontend-design framework.

Therefore, the main contribution of this dissertation is not simply the demonstration of several individual circuits, but the establishment of a coherent circuit level design direction for CMOS-based RF beamforming frontends from X-band to D-band. This work provides a practical foundation for future highly integrated multi-channel 6G transceivers, phased-array modules, and compact sub-THz wireless interfaces.

Chapter 7. Future Work

Several directions remain for future research. First, the proposed concepts should be extended from single-channel demonstrations to fully integrated multi-channel beamforming transceivers with shared LO generation, calibration, and digital control. Second, the delay, phase, and gain control concepts established in this dissertation should be combined with system level calibration methods so that channel-to-channel mismatch can be actively corrected in large-scale arrays. Third, as the operating frequency continues to increase, antenna integration, packaging, and chip-to-package co-design will become even more important, particularly for D-band and above. Finally, the dual-PA vector-synthesis concept proposed for 16-QAM transmitters may be further extended to higher-order modulation formats such as 64-QAM, provided that amplitude scaling, group-delay matching, and path-to-path phase alignment are more tightly controlled. In this sense, the work presented in this dissertation should be viewed not as an endpoint, but as a circuit foundation for the next stage of highly integrated, wideband, and energy-efficient 6G beamforming frontends.

논문초록

6G 무선 통신용 빔포밍 시스템을 위한 CMOS 기반 RF 프론트엔드 구현 연구

송정문
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본 학위논문은 차세대 6G 통신 시스템에서 요구되는 주파수 확장 전략에 대응하기 위해, 실리콘 기반 RF 빔포밍 프론트엔드의 체계적인 설계 프레임워크를 제시한다. 5G 밀리미터파 시스템의 실질적인 한계를 극복하기 위해, 본 연구에서는 광역 커버리지를 위한 '상위 중대역(Upper Mid-band, X-band)'과 초고속 데이터 전송을 위한 '서브 테라헤르츠(Sub-THz 및 D-band)'를 동시에 고려하는 이중 트랙 접근 방식을 채택하였다. 단일 회로 블록에 국한되지 않고, 각 주파수 대역에서의 지배적인 설계 제약 조건에 따라 CMOS 와 SiGe BiCMOS 공정을 전략적으로 선택하였다. 이를 통해 정확한 광대역 신호 정렬, 다기능 프론트엔드 집적, 초고주파 수신기 구조, 고효율 송신기 설계에 이르는 연속적인 연구 흐름을 구성하였다. 결과적으로 본 논문은 RF 빔포밍 프론트엔드의 핵심 문제를 신호 제어, 프론트엔드 집적, 주파수 확장이라는 세 가지 축을 중심으로 체계적으로 정리한다.

제 1 장은 광대역 빔포밍 시스템의 배경과 연구 동기를 소개하고, 동작 주파수가 X-band 에서 서브 테라헤르츠 및 D-band 로 확장됨에 따라 지연 정확도, 채널 간 일관성, 프론트엔드 집적의 중요성이 어떻게 증가하는지를 논의한다. 제 2 장에서는 65-nm CMOS 공정으로 구현된 5-11 GHz 대역의 8 비트 수동형 true-time-delay 회로를 제시한다. 하위 비트를 위한 정밀 미세 지연 구조와 상위 비트를 위한 기존 LC 기반 지연 셀을 결합함으로써, 제안된 회로는 1.56 ps 의 최소 지연 해상도와 400 ps 의 최대 지연을 달성하며, DC 전력 소모 없이 삽입 손실 변동을 최소화하였다. 제 3 장에서는 65-nm CMOS 기반 X-band 다기능 칩을 제안하며, 하이브리드 수동형 위상천이기, 감쇠기, 증폭기 블록, 그리고 송수신 스위칭 기능을 통합하였다. 제안된 칩은 낮은 RMS 위상 및 이득 오차와 함께 높은 집적도를 달성하였으며, 패키징에 따른 성능 저하를 설계 단계에서 분석하고 최소화하였다.

제 4 장에서는 130-nm SiGe BiCMOS 공정으로 구현된 275 GHz 대역의 두 가지 사분위 수신기 구조, 즉 mixer first 와 LNA first 토폴로지를 제시한다. 측정 결과를 통해 두 구조 모두 높은 이득과 넓은 IF 대역폭을 가지는 광대역 다운컨버전을 지원함을 확인하였으며, 감도, 칩 면적, 소비 전력 간의 명확한 트레이드오프를 보였다. 제 5 장에서는 40-nm CMOS 공정으로 구현된 D-band 송신기를 제안하며, 16-QAM 동작에서의 효율 향상을 목표로 한다. 비대칭 포화 특성을 갖는 듀얼 PA 구조와 광대역 위상 보정을 결합함으로써, 제안된 송신기는 높은 출력 전력과 최신 수준의 변조 효율을 달성하면서도 충분한 변조 정확도를 유지한다. 마지막으로 제 6 장에서는 본 논문의 전체적인

기여를 요약하고, 제 7 장에서는 다채널 빔포밍 송수신기 및 확장 가능한 서브 테라헤르츠 프론트엔드 시스템으로의 향후 확장 방향을 논의한다.

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