Master's Thesis

Study on FR3 and Sub-THz Beamformers for 6G Wireless Communications in CMOS Technology

Advisor: Professor Jung-Dong Park

Graduate School, Dongguk University
Department of Electronics and Electrical Engineering

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ABSTRACT

Beamforming concentrates electromagnetic energy toward a desired direction by precisely controlling the phase differences caused by propagation delays to each element in a multi-antenna array. This technique is fundamental to high-performance Integrated Sensing and Communication (ISAC) systems , which enables spatial multiplexing and interference suppression through multiple-input multiple-output (MIMO) processing, thereby allowing simultaneous handling of multiple independent channels and substantially improving capacity and coverage. Hardware implementations of beamforming primarily comprise phase shifters (PS) and true-time-delay (TTD) units: the former compensates phase offsets associated with element-dependent delays, whereas the latter provides frequency-independent delay compensation across element paths. This master's thesis investigates high-performance, compact TTD implementations for RF beamforming and presents beamformers designed in commercial CMOS processes for the FR3 and sub-terahertz (156 GHz) bands as key enablers of 6G hardware.

Chapter 1: This chapter provides an overview of the FR3 and sub-terahertz (sub-THz) bands as candidate spectra for 6G, and describes phased-array antennas and the key beamforming

hardware—phase shifters (PS) and true-time-delay (TTD) units.

Chapter 2: This chapter presents the design of an X-band, 6-bit hybrid true-time-delay (TTD) element operating from 9 to 11 GHz in a 28-nm CMOS FDSOI process[1]. While TTD fundamentally eliminates the beam-squint inherent to broadband transmission in phase-shifter-based beamforming, prior TTD implementations have typically suffered from short maximum delay, difficulty achieving linear code-to-delay characteristics, high insertion loss, and large area. The proposed hybrid TTD employs single-pole double-throw (SPDT) and double-pole double-throw (DPDT) switched-delay networks for the fine-delay stage (1.56, 3.125, 6.25, and 12.5 ps), and combines a single-pole N-throw (SPNT) selection network with a Gm-C all-pass filter for the coarse-delay stage (25, 50, and 75 ps), enabling precise, linear control over long delays. Measured results indicate a gain variation of 9 dB at 9 GHz across delay states, and an input return loss ≥ 10 dB ($S_{11,22} \leq -10$ dB) over the entire 9-11 GHz band. The total power consumption is 13.53 mW, and the silicon area is 0.54 mm². The delay resolution is 1.56% of the maximum delay, and the design achieves a state-of-the-art figure of merit compared with prior work.

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Chapter 3: This chapter presents a fully integrated four-channel X-band multifunction chip (MFC) fabricated in 65-nm bulk CMOS, occupying 2.85 mm² including pad-level ESD protection. To enable 3.3-V operation, the amplifier core adopts a three-stack device topology. A bi-directional gain amplifier with cross-coupled Rn-Cn feedback improves stability and bandwidth, while switchable shunt capacitors at the transformer interfaces realize resonant matching with minimal loss. The phase shifter employs transmission-line delays, achieving low insertion loss and effective cancellation of DPDT mismatch, enabling compact implementation with precise control. Measured small-signal performance confirms peak gain of 9.5 dB in transmit mode and 9 dB in receive mode, with 3-dB bandwidths of 8.5–9.7 GHz and 8.2–9.8 GHz, respectively. The receive-path noise figure (NF) is 6.2 dB at 9 GHz. The phase shifter attains an RMS phase error within 2.7° with DPDT tuning, and the attenuator achieves an RMS gain error within 0.55 dB using a trim bit, demonstrating high control accuracy. Linearity is validated with IP1dB better than −14.8 dBm over 8–10 GHz. The per-channel power consumption is 200 mW (Tx) and 135 mW (Rx).

Chapter 4: A high-efficiency 156-GHz transceiver was designed in a 28-nm CMOS FDSOI process, where beamforming is realized in the local-oscillator (LO) path by placing a 25-GHz true-time-delay (TTD) element ahead of a ×6 frequency multiplier in the LO chain. By situating the TTD in the lower-frequency section prior to

multiplication, the delay line's insertion loss is minimized, improving overall efficiency; the multiplied high-frequency LO is then applied to the mixer to align the per-channel RF phases and accomplish beamforming [4.2]. The architecture comprises a bidirectional gain amplifier (BDGA) in the IF chain; a TTD and a ×6 frequency multiplier in the LO chain; and, in the RF chain, a transmit/receive (T/R) switch (TRSW), power amplifier (PA), and low-noise amplifier (LNA). The frequency-conversion stage is implemented using a bidirectional mixer employing transformer-based VDD switching. Simulation results show an operating band of 150–160 GHz, a maximum delay of 53.7 ps, a TX saturated output power (Psat) of 5 dBm, an RX conversion gain of 27 dB, and an RX noise figure (NF) of 15 dB. The chip area is 2.47 mm^2, and the power consumption is 153 mW in transmit mode and 140 mW in receive mode.

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Sun-Hyeok Kwon

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Chapter 1. Introduction

1.1 Research Background

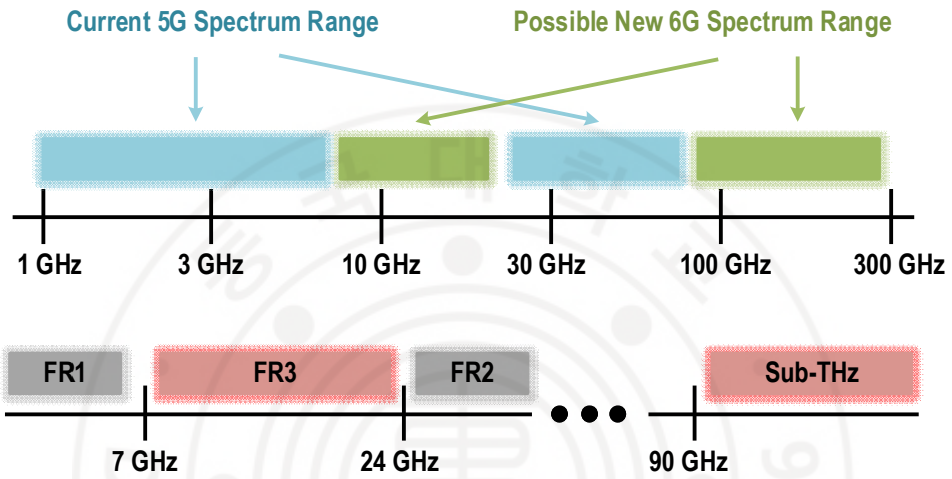

Figure 1-1 Frequency ranges for 5G (FR1, FR2) and new candidate bands for 6G (FR3, Sub-THz).

As illustrated in the mobile communication frequency spectrum in Figure 1-1, the next-generation technology, 6G, is considering new high-frequency bands such as FR3 (7-24 GHz) and sub-terahertz (sub-THz, above 90 GHz) to realize ultra-broadband services. 1[1.1] However, these frequency bands have significant physical limitations compared to conventional low-frequency bands, including severe free-space path loss and high susceptibility to signal blockage by obstacles like buildings or people.

The key technology to overcome these high-frequency

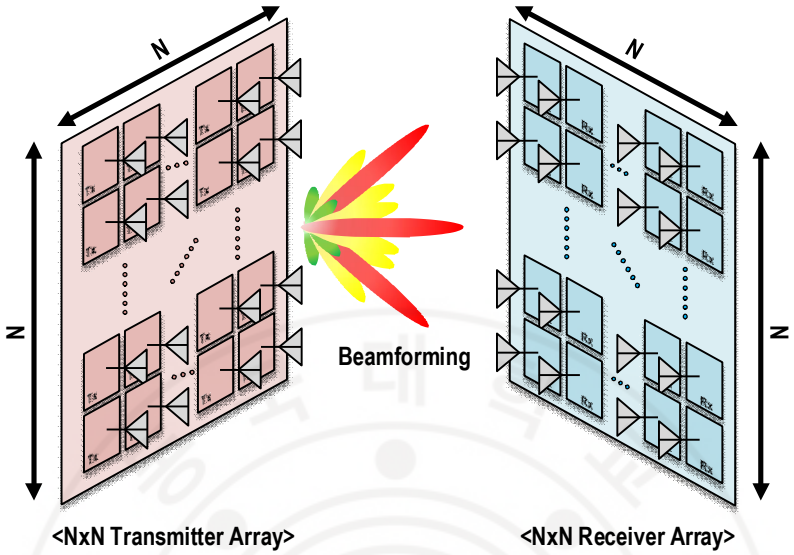

Figure 1-2 Conceptual illustration of beamforming in a Multiple-Input, Multiple-Output (MIMO) system.

limitations and establish a reliable communication link is the phased-array system, and its core operational principle is beamforming. Beamforming is a spatial filtering technique that applies precise amplitude and phase weights to the signals fed to each element of a multi-antenna array, thereby focusing the radiation pattern in a desired direction. This technique maximizes the array gain through in-phase combining of signals in the target direction, while suppressing interference in other directions through destructive interference.

From a communication system perspective, beamforming is combined with Massive MIMO (Multiple-Input, Multiple-Output) systems to maximize its performance [1.2-1.3]. As depicted in

Figure 1-2, MIMO technology uses multiple antennas at both the transmitter and receiver to create several independent data paths simultaneously within the same frequency band. Through spatial multiplexing, which utilizes these multiple paths, more data can be transmitted at the same time in limited frequency resources, dramatically increasing channel capacity. Beamforming plays the role of precisely steering these multiple data streams toward each user and suppressing interference between the streams, which ultimately results in a significant improvement in communication coverage and reliability.

In addition to communications, beamforming also plays a critical role in radar systems [1.4-1.5]. It serves as a key means to enhance detection range and angular resolution, and to enable high-speed spatial surveys, multi-target tracking, and low probability of intercept operations through electronic beam steering.

As such, in next-generation wireless systems for 6G ISAC (Integrated Sensing and Communication), beamforming has established itself as an indispensable technology for satisfying both a high link budget and overall system performance. This thesis deals with the design and measurement verification of a beamformer based on a commercial CMOS process, operating in the FR3 and sub-THz bands.

1.2 Phase Array System

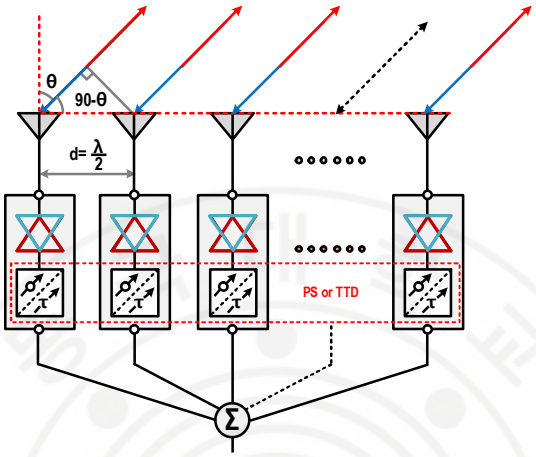

Figure 1-3 Block diagram of a phased-array antenna system for beamforming.

A phased-array system is a technology that precisely steers or shapes a radiation pattern by applying complex weights (i.e., amplitude and phase) to each element of a multi-antenna array. Figure 1-3 illustrates the block diagram of a typical phased-array antenna system designed for beamforming. For a linear array composed of N elements with a spacing of d, the Array Factor (AF) as a function of the angle θ is expressed as:

$$AF(\theta) = \sum_{m=1}^{N} \omega_m e^{j(m-1)kd\sin\theta} \tag{1.1}$$

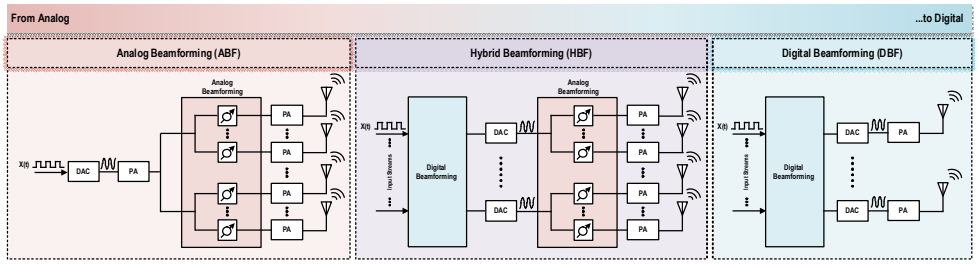

Figure 1-4 Conceptual illustration of beamforming in a Multiple-Input, Multiple-Output (MIMO) system.

In equation (1.1), ω_m represents the weight applied to each element, and k is the wavenumber ($2\pi/\lambda$). Through appropriate weighting (ω_m), signals are combined in-phase in the target direction to achieve high array gain, while destructive interference is induced in non-target directions to suppress interference and sidelobes.

Beamforming can be categorized by its implementation method—analog, digital, and hybrid—as conceptually illustrated in Figure 1-4. Analog beamforming is a method that applies phase and amplitude weights directly in the RF or Local Oscillator (LO) signal path using analog components such as phase shifters and attenuators [1.6-1.7]. This approach is cost-effective with low power consumption because it minimizes the number of high-speed data converters, but it generally supports only one data stream per beam and has limited flexibility as the weights are set in the analog domain.

Digital beamforming, in contrast, places a dedicated RF front-end and high-speed data converter (ADC/DAC) at each antenna element, applying the weights through digital signal processing in the baseband processor [1.8-1.9]. This architecture offers the highest flexibility and performance, enabling sophisticated signal processing such as the simultaneous generation of multiple beams and adaptive null steering. However, it demands a massive number of high-speed data converters, leading to significantly higher power consumption, a larger hardware footprint, and an immense data processing burden, especially for a large number of antenna elements.

Hybrid beamforming is a compromise between these two approaches, where a smaller number of digital chains each control a sub-array of antennas that perform analog beamforming [1.10-1.11]. This provides a practical balance, offering some of the flexibility of digital beamforming (such as supporting multiple beams, though fewer than a pure digital system) while managing the hardware and power overhead.

Particularly in high-frequency, wideband environments like FR3 and sub-terahertz (sub-THz), the high power consumption and massive data interface burden of digital beamforming become significant as the number of elements increases. Therefore, analog and hybrid beamforming, which allow for control at the element or sub-array level, are considered practical alternatives.

1.2.1 Phase Shifter (PS)

A phase shifter is a key component that electrically controls the phase of an input RF signal. In a phased-array antenna system, it plays a crucial role in implementing beamforming, which steers or shapes the antenna's radiation pattern by precisely adjusting the relative phases of the signals fed to each antenna element.

For the signal wavefront to be aligned in a specific direction, the signals radiated from each element must produce constructive interference in the target direction and destructive interference in other directions. Mathematically, the phase (ϕ_m) that must be applied to the m-th antenna element for a target steering angle (θ_0) is defined as follows:

$$f_m(f_0) = k_0 d_m \sin\theta_0 \quad \text{,where} \quad k_0 = \frac{2\pi f_0}{c} \tag{1.2}$$

In equation (1.2), $\phi_m(f_0)$ is the required phase shift for the m-th element at the center frequency f_0, k_0 is the wavenumber at that frequency, d is the element spacing, c is the speed of light, and m is the element index. The phase shifter is the key component that implements the desired beam steering by precisely applying this calculated phase (ϕ_m) to each antenna path.

Phase shifters can be implemented in various architectures based on their operating principle, as conceptually illustrated in Figure 1-5.

As shown in Figure 1-5(a), a reflective-type phase shifter consists of a 90° hybrid coupler and two identical, variable reflective loads [1.12]. The phase is controlled by varying the impedance of the loads, which alters the phase of the signal reflected from them after being split by the coupler. The main advantage of this method is its ability to achieve a wide phase-shift range with a relatively simple structure; however, its disadvantage is that the input/output return loss tends to degrade because the impedance of the loads changes during phase shifting.

The vector sum approach, depicted in Figure 1-5(b), splits the input signal into I/Q signals, adjusts their respective amplitudes with Variable Gain Amplifiers (VGAs), and then sums them back together [1.13]. This approach has the advantage of offering very high-precision control of phase and amplitude independently, and can even provide signal gain. However, it suffers from the disadvantages of high-power consumption, a complex circuit architecture, and potential degradation in noise performance due to the use of many active components.

Figure 1-5(c) illustrates a switched-type architecture, which is a representative digital controlled approach [1.14]. This structure works by using RF switches to select a signal path—either a reference path or various delay paths that introduce specific phase shifts. This switched-type architecture has the

advantages of simple control and high, predictable phase accuracy. On the other hand, its limitations include the insertion loss of the RF switches, which adds to the overall loss, and the fact that only discrete (non-continuous) phase control is possible.

While the previously described phase shifter is a fundamental method for implementing beamforming, it has an inherent limitation in systems that use wideband signals. A phase shifter provides a constant phase shift ($\Delta\phi$) regardless of frequency. This causes the beam's steering angle (θ_0) to become dependent on the signal's frequency (f), as shown in the beam steering equation:

$$\theta_0 = \sin^{-1}\left(\frac{c\Delta\phi}{2\pi fd}\right) \tag{1.3}$$

In equation (1.3), c is the speed of light and d is the element spacing. Since $\Delta\phi$ is constant, any change in frequency (f) across the signal's bandwidth will cause the steering angle (θ_0) to deviate. This unwanted deviation of the beam's direction with frequency is a phenomenon known as "beam squint".

To address this critical issue, the True Time Delay (TTD), which provides a constant time delay independent of frequency, is proposed as an alternative solution. The principles and advantages of TTD will be detailed in Section 1.2.2.

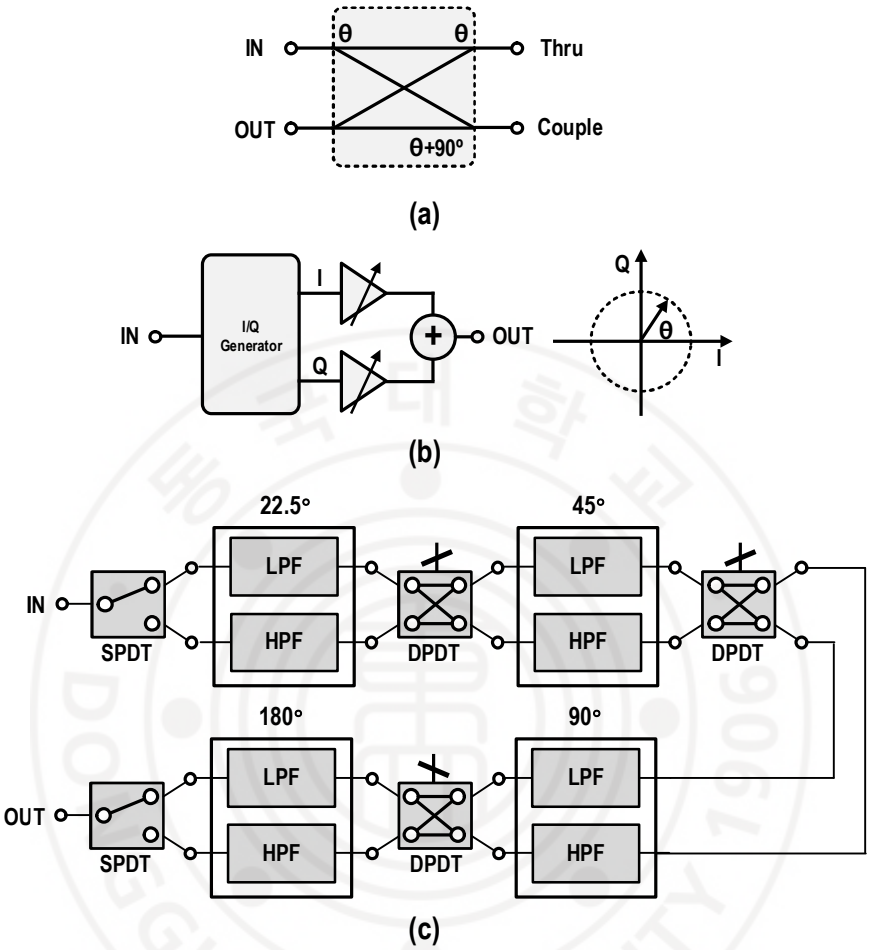

Figure 1-5 Block diagrams of various phase shifter architectures: (a) reflective-type, (b) vector sum type, and (c) digital switched-type.

1.2.2 True Time Delay (TTD)

True Time Delay (TTD) is a key beamforming implementation method designed to solve the beam squint phenomenon, which is a fundamental limitation of the phase shifters described in Section 1.2.1. While a phase shifter provides a constant phase shift regardless of frequency, a TTD, as its name implies, provides a constant time delay.

To steer a beam in a specific direction (θ_0), a TTD must apply a progressively increasing time delay to each antenna element in the array. The required time delay (t_m) for the m−th antenna element is calculated for a target steering angle (θ_0) as follows:

$$t_m = \frac{md\sin(\theta_0)}{c} \tag{1.4}$$

In equation (1.4), t_m is the required time delay for the m−th element, m is the index of the antenna element (0, 1, 2, ...), d is the element spacing, and c is the speed of light. This equation clearly shows that the time delay (t_m) required for beam steering is frequency−independent. Therefore, unlike with a phase shifter, all frequency components of a wideband signal are aligned in the same direction (θ_0), and the beam squint phenomenon does not occur. A practical TTD circuit operates by implementing these calculated time delay values, for example, by using switches to select transmission lines of different lengths.

The representative methods for implementing a True Time Delay (TTD) are the switched-line approach [1.15] and the all-pass filter (APF) approach [1.16], each with clear trade-offs in terms of area and bandwidth. The most intuitive switched-line method, which controls delay by selecting transmission lines of different lengths, has the significant advantage of providing nearly perfect true time delay over a wide bandwidth, but suffers from the drawback of large circuit area for long delays. In contrast, the all-pass filter approach utilizes the group delay characteristic of a filter and can be implemented with compact lumped elements, offering the benefit of a much smaller area. However, it is limited by a narrower operating bandwidth compared to the switched-line method, as the group delay remains constant only over a restricted frequency range. To address these trade-offs, this work proposes a Hybrid TTD structure that combines the advantages of both approaches to simultaneously achieve wide bandwidth and a compact area, which will be detailed in Chapter 2.

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Chapter 2. An X-Band 6-Bit Hybrid True Time Delay in 28nm FDSOI

2.1 Introduction

A critical consideration when employing True Time Delay (TTD) for beamforming is that the required maximum delay increases proportionally with the number of elements in the phased array. This necessitates longer delay times, and as the maximum delay increases, the chip size correspondingly grows. Figure 2.1-1 (a) illustrates various previously reported TTD circuit designs, which can be categorized into conventional structures [2.7-2.8], Trombone structures [2.9-2.18], filter-based structures [2.19-2.25], and Gm-C structures employing active components [2.26-2.32]. Trombone and filter-based structures typically require larger areas as the maximum delay grows. In contrast, Gm-C structures offer the advantage of achieving significant delays within a smaller area but face limitations such as lower resolution and increased power consumption. Figure 2.1-1-(b) illustrates the delay variation of previously reported TTD circuits with center frequencies below 25 GHz, excluding continuous-tuning type designs. Most circuits exhibit a delay variation exceeding 6%, while [2.19] and [2.24] achieve excellent delay variation. However, these designs suffer from the limitation of large chip areas due to their filter-type structures.

To address these challenges, this paper introduces a TTD circuit implemented using the 28nm FD-SOI CMOS process, featuring a 6-bit control mechanism for enhanced precision. For short delays (1.56 ps, 3.125 ps, 6.25 ps, 12.5 ps), the design employs a conventional approach, while for longer delays (25 ps, 50 ps, 75 ps), it integrates a Gm-C-based all-pass filter circuit with an SPTT (Single-Pole Triple-Throw) switch in a thermostat-based linear delay configuration. This design achieves a maximum delay of 100 ps with a resolution of 1.56 ps, enabling precise delay control. These characteristics make the proposed TTD circuit particularly suitable for applications requiring efficient and accurate beam steering across a broad frequency range.

The key feature of the proposed work lies in the integration of a Single-Pole N-Throw (SPNT) switch with an active element-based all-pass filter (APF), enabling highly flexible and space-efficient delay control. This combination enables precise management of diverse delay values while improving performance and significantly reducing both power consumption and circuit area. These features make the approach particularly suitable for systems prioritizing low power consumption and compact designs. A linear delay control mechanism is realized through the SPNT switch, while the Gm-C-based all-pass filter functions as a coarse delay cell, effectively handling larger delay increments.

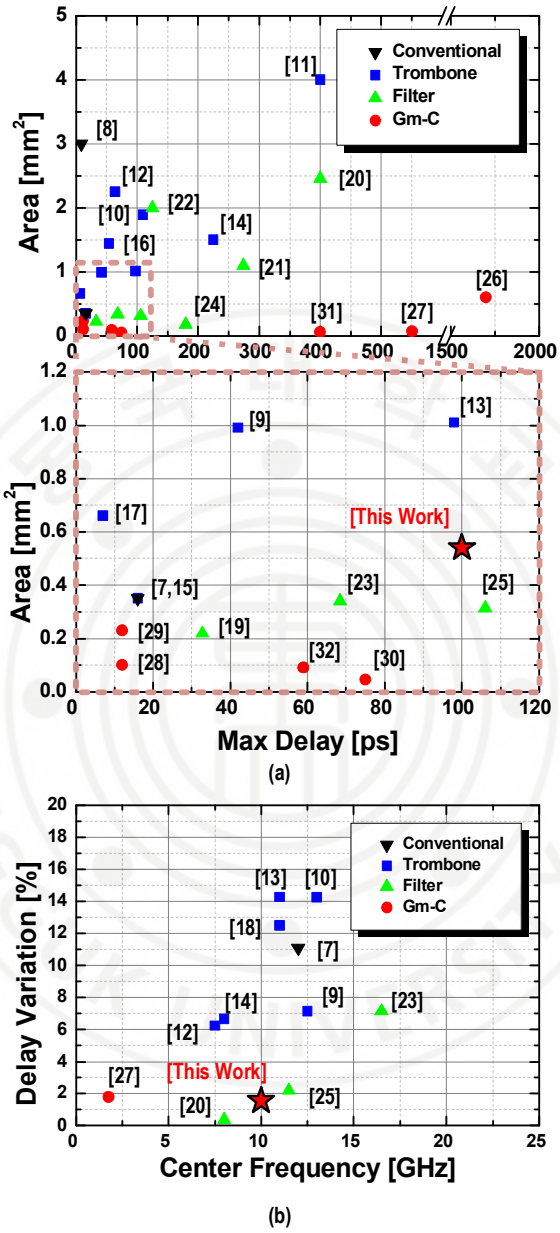


Figure 2.1-1 Comparison of previously reported time delay circuits: (a) Area vs. Maximum Delay (b) Delay Variation vs. center frequency

2.2 Proposed Linearly Controlled Delay Cell with SPNT

In this design, a Single-Pole N-Throw (SPNT) switch is utilized to select among various delay paths. Specifically, this work employs a Single-Pole Triple-Throw (SPTT) configuration, supporting up to three paths, as illustrated in Fig. 2.2-1(a). However, the SPNT structure can be expanded to accommodate additional paths, thereby enhancing flexibility and enabling the implementation of a broader range of delay values. This scalability allows for the realization of longer delays without necessitating circuit redesign, making it particularly advantageous in systems where miniaturization is critical. The proposed approach is especially effective for managing the large delays required in massive timed-array antenna systems.

As illustrated in Fig. 2-(b), the SPTT switch in this design is implemented utilizing a transmission gate structure composed of RF components, with the detailed circuit schematics presented in Fig. 2-(c). The transmission gate offers numerous benefits, including miniaturization, low power consumption, and reduced insertion loss, making it particularly suitable for high-frequency applications. Its simple device structure contributes to the compactness of the circuit, which is critical in systems requiring small form factors. Moreover, the transmission gate demonstrates excellent power efficiency, consuming minimal power during switching operations and negligible power when active. This feature is essential for

maintaining stable performance in high-frequency environments. The low switch resistance also minimizes signal insertion loss and distortion, even at high frequencies, ensuring precise signal transmission and reducing high-frequency signal degradation, which make the transmission gate as an optimal choice for the SPTT switch of the proposed TTD design. The primary advantage of this architecture lies in the excellent isolation achieved between switch paths. This is facilitated by the Gm-C-based all-pass filter, which connects the input to the gate of the MOSFET. This configuration effectively minimizes signal interference between paths, thereby ensuring robust isolation.

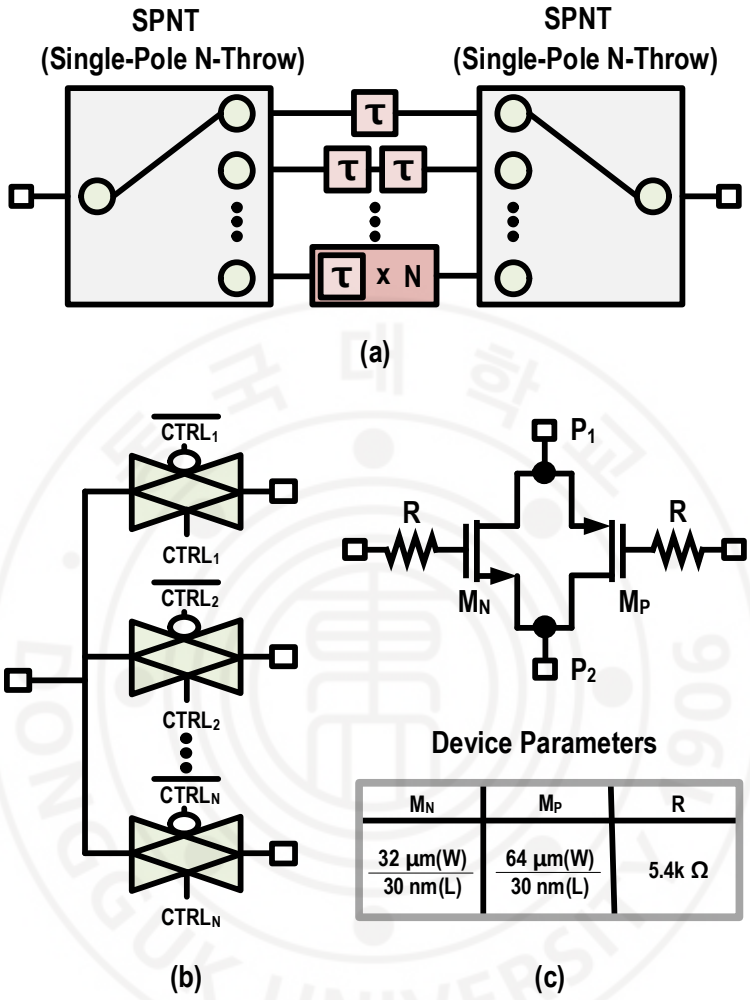


Figure 2.2-1 (a) Proposed linearly controlled delay cell with SPNT (b) Block diagram of SPNT (c) Schematic of transmission gate switch

2.3 Proposed Hybrid TTD Architecture

This proposed TTD circuit is implemented using the 28nm FD-SOI CMOS process, featuring a 6-bit control mechanism for enhanced precision. Figure 2.3-1 illustrates the overall block diagram of the TTD system proposed in this work. For the short delay sections (1.56 ps, 3.125 ps, 6.25 ps, and 12.5 ps), the delays are implemented using SPDT and DPDT switches in combination with transmission lines (T-line) as short delay elements. It will be depicted in section 2.3.1. For the long delay cells (25 ps, 50 ps, and 75 ps), the design employs a combination of the SPTT and all-pass filter (APF) structures, enabling linear delay control using the thermostat method. It will be depicted in section 2.3.2.

SPDT or DPDT switches are similarly utilized to select between the reference and delay lines, ensuring that the delay

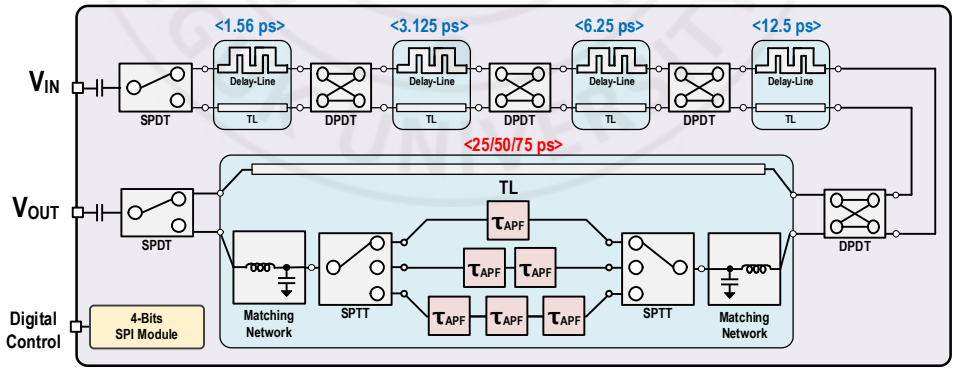


Figure 2.3-1 Block diagram of proposed hybrid true time delay (TTD) utilizing transmission-lines and cascased Gm-C-based all pass filters

characteristics of the APF align with those of the TL in the shorter sections. This alignment reduces the overall root mean square (RMS) error. Moreover, since the APF exhibits higher loss than the T-line, additional design optimizations were implemented to minimize losses when realizing delays in the range of 1.56 ps to 23.44 ps.

To implement long delay cells, the input of the SPTT is connected to a DPDT switch, while its output is connected to an SPDT switch. To minimize losses, 50-ohm matching networks are placed between the DPDT and SPTT, as well as between the SPTT and SPDT. Additionally, a 16-bit Serial Peripheral Interface (SPI) circuit is incorporated into the design to control the switches digitally.

Table 2.3-1 presents the logic mapping table used to control the proposed hybrid TTD circuit. The table is organized into four distinct delay regions, each corresponding to a specific range of delay values. For each delay range, the appropriate logic states are applied to the associated All-Pass Filter (APF) path, facilitating the accurate output of the desired delay. By dynamically assigning signals to the correct APF path based on the logic states specified in the table, the circuit ensures precise delay control of the hybrid TTD over a wide range of operating conditions.

Table 2.3-1 Logic mapping table for hybrid true time delay (TTD) control

Range [ps]	Main Delay State [ps]							
	1.56	3.125	6.25	12.5	APF Path	25	50	75
1.56 ~ 23.435	±	±	±	±	−	×	×	×
26.56~ 48.435	±	±	±	±	+	+	−	−
51.56~ 73.435	±	±	±	±	+	−	+	−
76.56~ 98.435	±	±	±	±	+	−	−	+

+ = HIGH, - = LOW, ± = HIGH or LOW, × = Don't Care

2.3.1 Transmission-Line based TTD for Fine Cell

For the short delay sections (1.56 ps, 3.125 ps, 6.25 ps, and 12.5 ps), the delays are implemented using SPDT and DPDT switches in combination with transmission lines (T-line) as short delay elements. Each switch toggles between the reference line and the delay line, with the T-line providing a fixed delay time for each path. The SPDT and DPDT switches are designed using a transmission gate structure as depicted in section 2.2. Figure 2.3-2 presents the symbols and block diagrams of the SPDT and DPDT. Similar to the SPNT structure shown in Fig. 2.2-1(b), it is

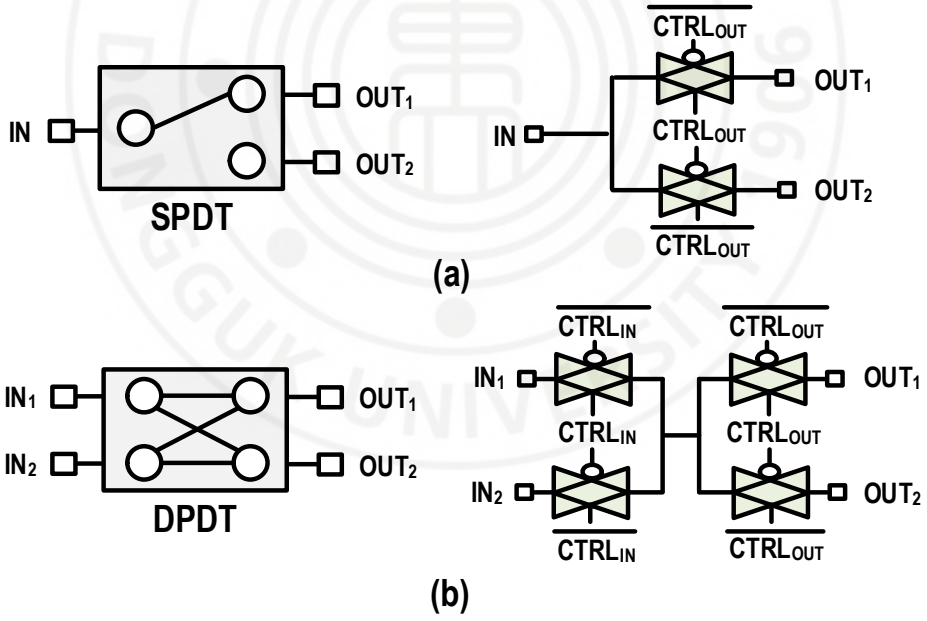


Figure 2.3-2 Switch implementation using CMOS transmission gates: (a) SPDT, (b) DPDT

designed based on the transmission gate circuit presented in Fig. 2.2-1(c).

The 28 nm FD-SOI CMOS process utilized in the implementation mandates strict density rules in its design guidelines, requiring dummy fills for the precision delay design of the T-line delay cell. These dummy structures, however, can substantially affect RF characteristics. To address this, a high-density custom dummy fill was meticulously designed and integrated into the simulation, enabling precise design adjustments to mitigate its negative impact on RF performance and achieve optimal circuit functionality, as shown in Fig. 2.3-3(a). Simulations were performed to evaluate and compare delay variations with and without the dummy fill as illustrated in Fig. 2.3-3(c).

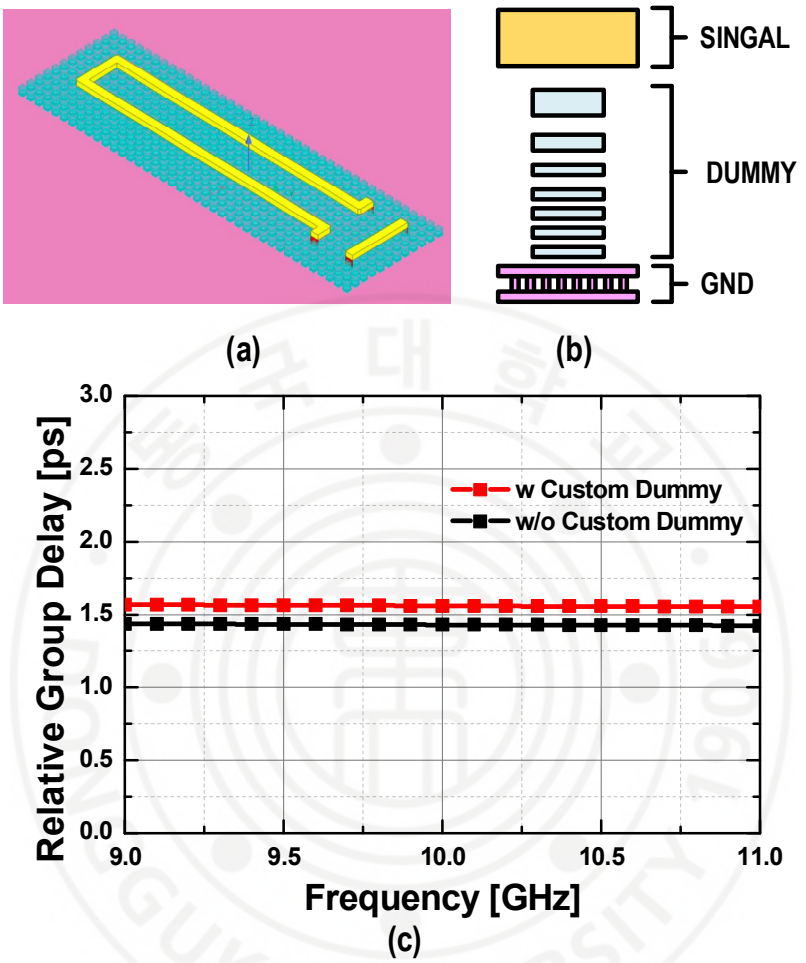
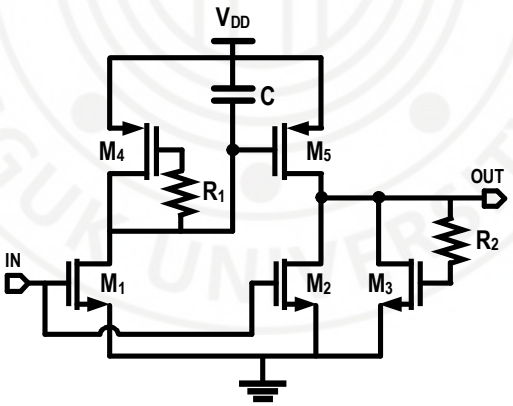


Figure 2.3-3 (a) 3-D view on HFSS of 1.56ps delay line with custom dummy (b) side view of metal layers (c) simulated relative group delay with custom dummy and without custom dummy

2.3.2 Gm-C All-Pass Filter based TTD for Coarse Cell

The Gm-C all pass filter (APF) was chosen for its ability to provide coarse time delays while maintaining excellent area efficiency. Its key advantage lies in the properties of an ideal all-pass filter, which adjusts the phase of the input signal without altering its amplitude. Additionally, its phase response changes linearly with frequency, making it highly suitable for TTD circuit design. However, this structure has notable limitations, that is operating frequency is restricted by the RF performance of the active device. As the operating frequency increases, the transconductance (gm) decreases, resulting in longer delays, complicating the design of high-resolution TTD circuits. We utilized



Device Parameters

M_{1-3}	M_4	M_5	R_1	R_2
20 μm(W) / 30 nm(L)	25 μm(W) / 30 nm(L)	50 μm(W) / 30 nm(L)	600 Ω	1k Ω

Figure 2.3-4 Gm-C based all-pass filter for coarse cell [2.26]

the Gm-C APF structure reported in [2.26], implemented in 28nm FDSOI CMOS process, as illustrated in Fig. 2.3-4. This architecture provides a delay characterized by $\tau = 2C/g_m$. In our design, a single delay cell achieves a 25 ps delay. By connecting multiple delay cells in series, delay cells of 50 ps (two cells) and 75 ps (three cells) can be realized correspondingly. It is noted that the DC voltage of Vout is equal to the DC voltage of Vin, making the structure easily cascadable. The simulation results, combined with the SPTT structure, are presented in Fig. 2.3-5. The circuit operates within a frequency range of 9-11 GHz, with an insertion loss variation of approximately 2 dB.

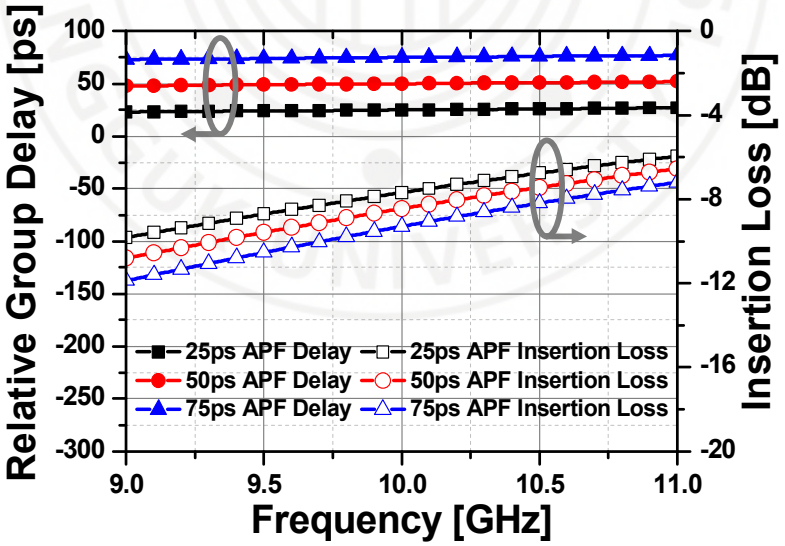


Figure 2.3-5 Simulation results of proposed delay cell with SPTT

2.3.3 Chip Photograph

The 6-bit TTD, designed using a combination of transmission-line delay and an all-pass filter (APF), was fabricated in Samsung 28nm FDSOI CMOS process, with the chip layout and photo presented in Fig. 2.3-6. Excluding the pad area, the chip dimensions are 600 μm × 900 μm, yielding a total area of 0.54 mm2.

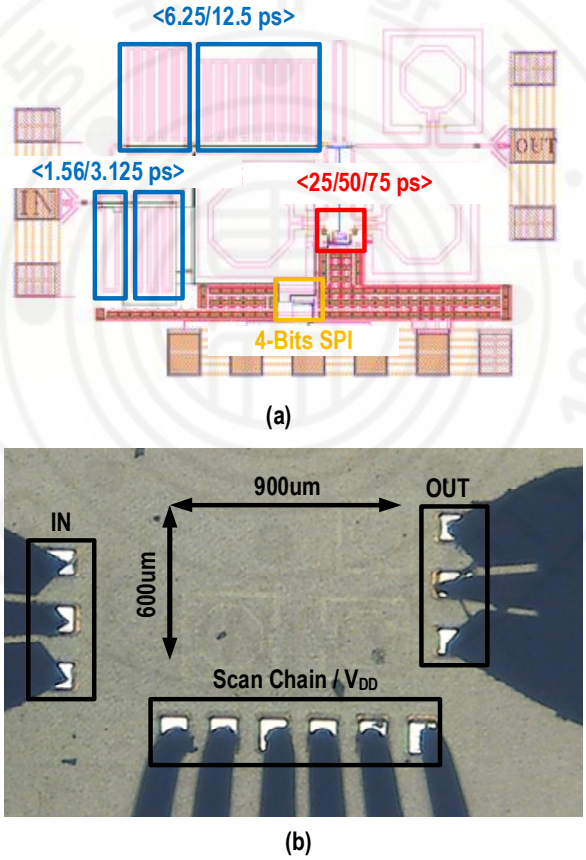


Figure 2.3-6 (a) Layout of designed TTD (b) Chip-photograph of the fabricated TTD in Samsung 28nm FDSOI.

2.4 Measurement

2.4.1 Measurement Setup

On-chip measurement with in-situ probing was performed to verify the performance of the implemented TTD chip. The digitally controlled time delay and S-parameters were evaluated using a Keysight N5224A network analyzer as illustrated in Fig. 2.4-1(a). In measuring the large-signal performance, we used Agilent 83623B signal generator and Agilent E4407B spectrum analyzer in Fig. 2.4-1(b). The implemented TTD operates under a 1.1V power supply (Keysight E36313A power supply) with the current consumption of 12.3mA.

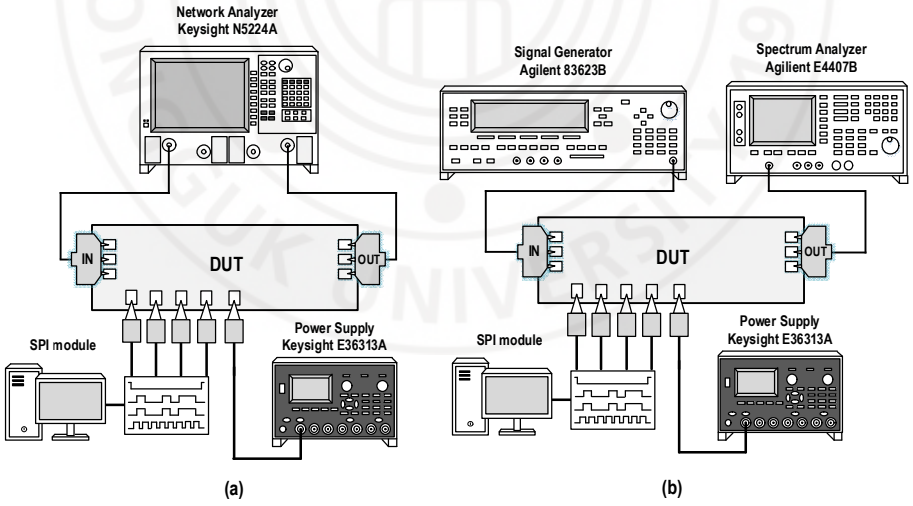


Figure 2.4-1 The measurement setup for (a) S-parameters, time delay over the frequency (b) large-signal performance

2.4.2 Group Delay at Small Signal

Figure 2.4-2 presents the measured relative group delay for all states, along with a comparison of measured RMS error and simulation results in the 9-11GHz range. The measured RMS error is less than the target resolution of 1.56ps, confirming precise system operation and accurate time delay implementation.

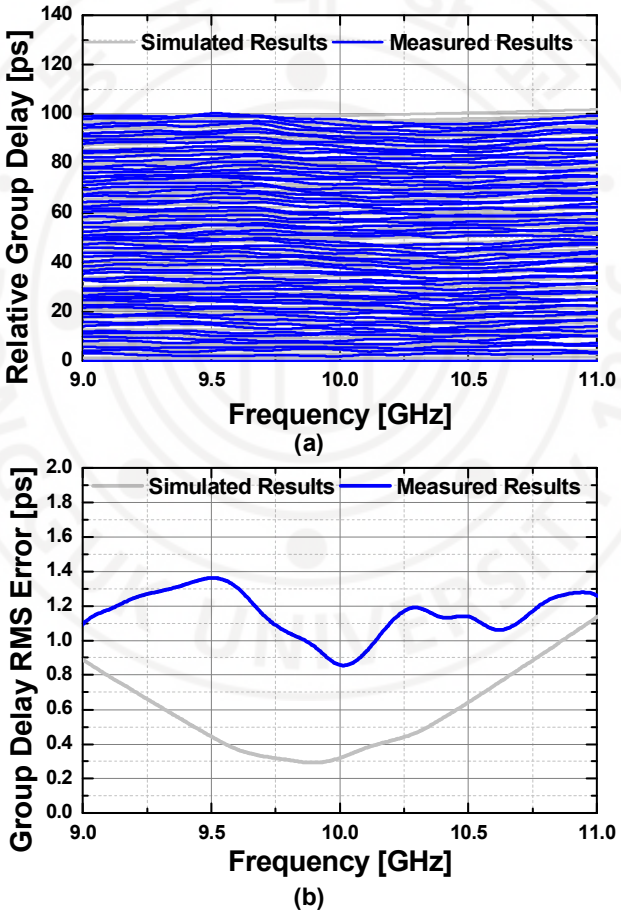


Figure 2.4-2 (a) Measured group delay of the all states (b) Simulated and measured rms error of group delay to 9-11GHz

Figure 2.4-3 presents the phase measurement results, illustrating a linear increase with respect to the frequency of the time delay circuit.

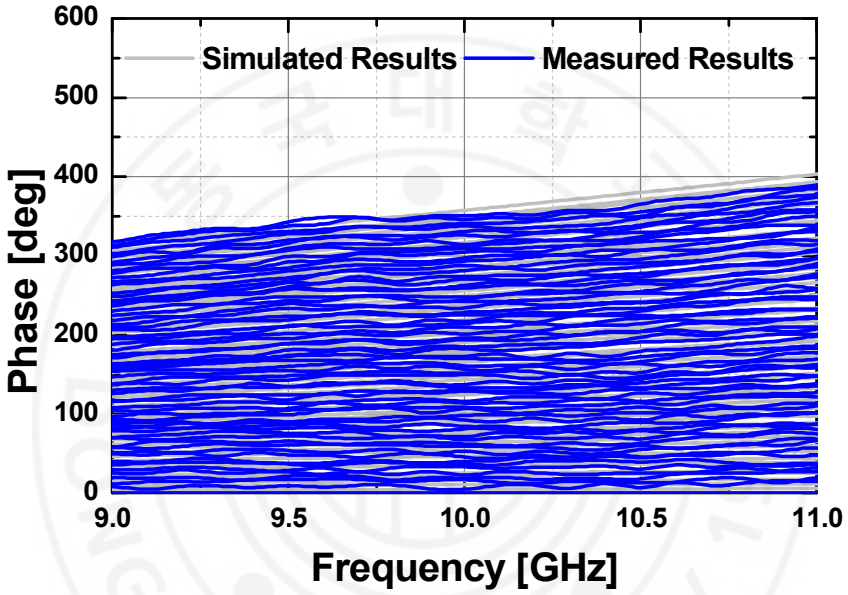


Figure 2.4-3 Measured relative phase of the all states to 9-11GHz range

The measured S-parameters for all states are shown in Figure 2.4-4(a). The return loss for both input and output exceed 10dB, indicating effective impedance matching. Figure 2.4-4(b) shows gain variations of ±4dB at 11GHz and ±7dB at 9GHz, demonstrating stable signal transmission across the frequency range.

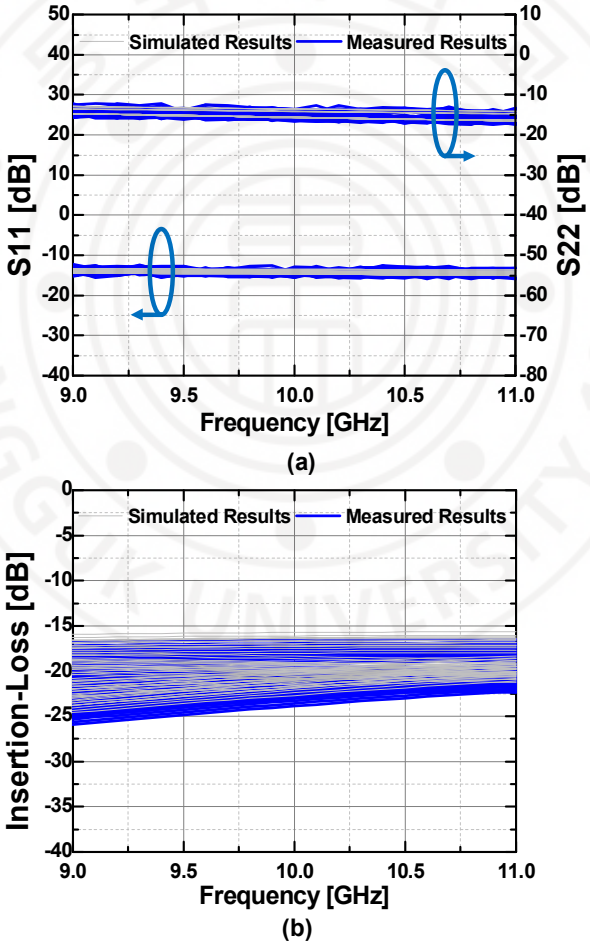


Figure 2.4-4 Measured (a) input and output return loss (b) insertion loss of the all states between 9G and11GHz range.

2.4.3 Group Delay at Large Signal

Figure 2.4-5 depicts the output power (Pout) and gain compression at 10 GHz at the reference state. The measured input 1-dB compression point (IP1dB) was determined to be 12 dBm.

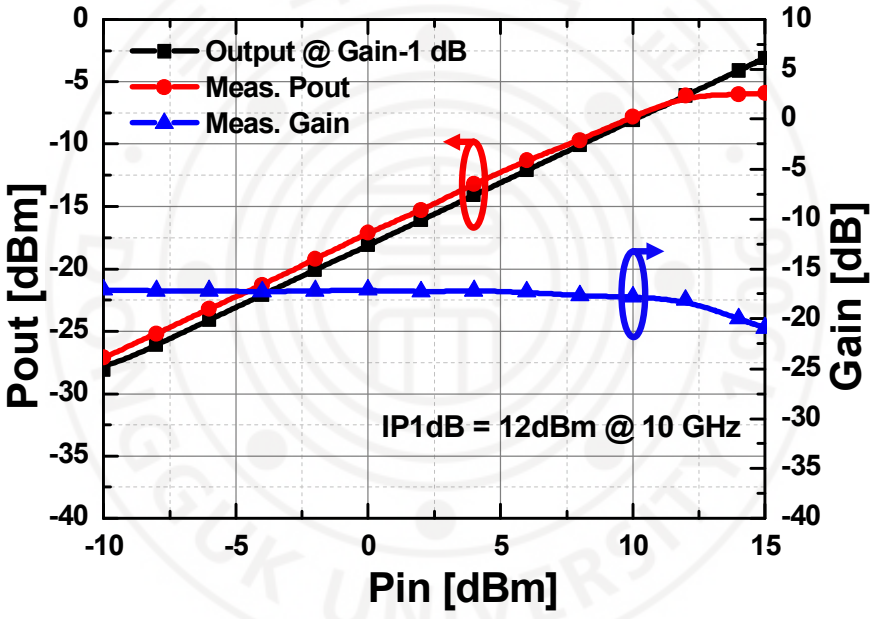


Figure 2.4-5 Measured output power and gain compression curve with the reference delay state at 10 GHz

Figure 2.4-6 illustrates the relative group delay of APF-based cells (25 ps, 50 ps, 75 ps) as a function of input power (Pin). The group delay remains nearly constant up to the onset of gain compression. Beyond this threshold, increasing gain compression results in more pronounced nonlinearity of the active components, leading to greater delay errors. Nonetheless, the circuit demonstrates robust performance under varying input power conditions, ensuring reliable operation across a broad range of input power level

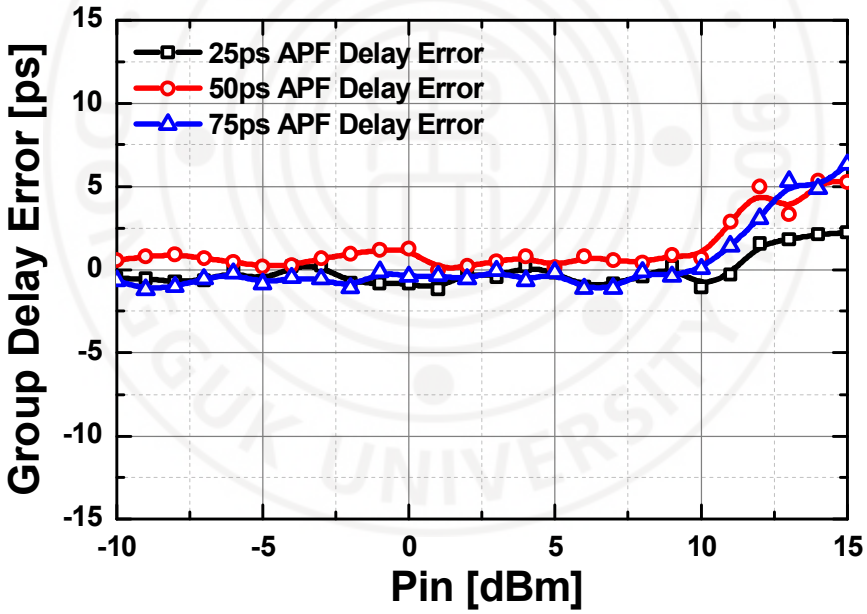


Figure 2.4-6 Measured Pin versus relative group delay error of APF-based delay cells (25ps, 50ps, 75ps) with the reference delay state at 10 GHz

2.4.4 Comparison with other TTDs

Table 2.4-1 provides a comparative assessment of previously published true time delay circuits against the design presented here. Within similar frequency ranges, the proposed circuit achieves a notably smaller chip footprint, the highest resolution, and minimal delay variation. Despite employing active components, it also maintains exceptionally low power consumption. The FoM listed in Table 2.4-1 accounts for maximum delay, resolution, bandwidth, power usage, and area. Excluding passive [18] and continuous [19] designs, the proposed TTD circuit demonstrates the best overall performance.

Table 2.4-1 Comparison table of true time delay

Ref	**This Work**	[2.25] JSSC 2015	[2.9] MWCL 2013	[2.18] Access 2022	[2.10] TMTT 2020	[2.11] MTT-S 2015
Tech	**28nm SOI**	140nm CMOS	130nm CMOS	65nm CMOS	180nm CMOS	130nm CMOS
Structure	**TL + APF**	APF	Trombone	Low Pass LC	Passive 2nd/4th order APN	Passive APN + Trombone
Freq [GHz]	**9-11**	1-2.5	15-40	5-11	8-18	1-20
Maximum Delay [ps]	**100**	550	42	400	109.3	400
Resolution [ps] / Bit	**1.56 / 6**	13 / 6	5.2 / 4	1.54 / 8	15.6 / 3	Continuous
Gain Variation [dB]	**±9**	±1.4†	±2†	±30*	±1†	±16*,†
Delay Variation [%]	**1.56**	1.8	12.5	0.39	19	Continuous
RMS Delay Error [ps]	**≤ 1.39**	N/A	N/A	≤4.5	≤ 4	N/A
Pdc / CH [mW]	**13.53**	90	8.6-24.6	Passive	44.2	2.6-6
Chip Area [mm^2]	**0.54**	0.07	0.99	2.46	1.89	4.0
FoM [GHz/mW·mm^2]	**17.5**	10.07	16.1	-	0.178	-

*** Estimated from measured plots.**
† With calibration gain amplifier.

$$\textbf{FoM} = \frac{\left(\frac{Max\ Delay}{Resolution}\right) \times Bandwidth}{Power\ Consumption \times Area}.$$

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Chapter 3. An X-Band 3.3-V Four-Channel Phased-Array T/R Module Chip in 65-nm CMOS

3.1 Introduction

Modern phased array T/R modules demand high-density integration for beamforming gain, along with precise per-channel phase and amplitude control and on-chip calibration. While compound semiconductors like GaN and GaAs are advantageous for achieving high power and excellent linearity due to their wide bandgap and high carrier mobility, they pose significant challenges, including high integration costs and difficulties in integrating large-scale digital control and calibration circuitry on-chip [3.1-2].

In contrast, CMOS technology allows for the seamless integration of RF, analog, and digital blocks on a single die, substantially reducing system complexity and cost in large-channel array systems [3.3-4]. However, the low core supply voltage of standard CMOS processes (approximately 1V) presents fundamental limitations. This low voltage restricts the output swing and linearity of power amplifiers (PAs), the on-resistance and overdrive margin of switch networks (e.g., phase shifters and attenuators), and the driving capability of channel interfaces [3.4].

This work addresses these limitations by designing an amplifier with a three-stack structure in a 1V-class process, enabling a T/R

module to operate at 3.3V. The core hypothesis is that the system-level benefits—improved output power, linearity, and control precision—gained by extending the voltage headroom outweigh the drawbacks of increased parasitics and complexity introduced by the stacked structure.

3.2 Three-Stacked Device Structure for 3.3-V Operation

A three-stack device is a circuit architecture designed to safely utilize a high supply voltage (e.g., 3.3 V) in a CMOS process that uses low-voltage core devices (around the 1 V level). It is typically implemented by stacking two Common-Gate (CG) stages on top of a single Common-Source (CS) stage, as depicted in the schematic

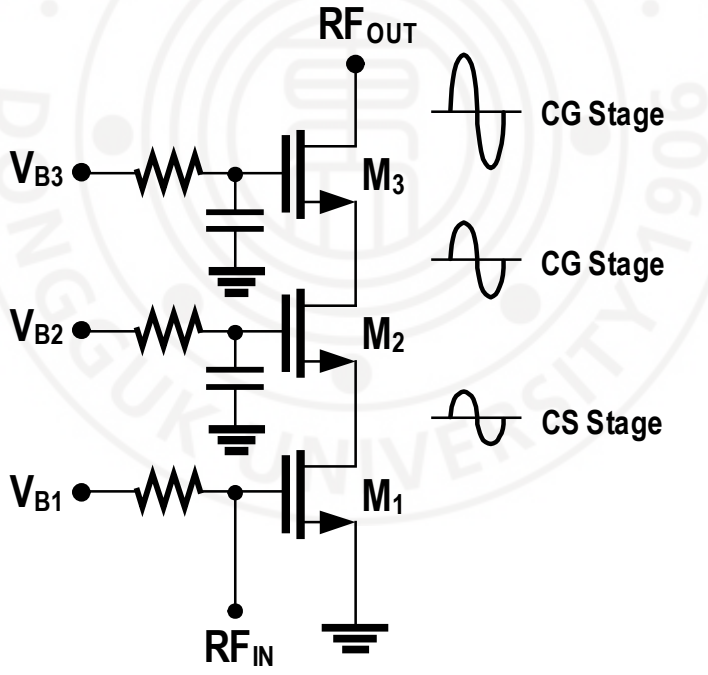


Figure 3.2-1 Schematic of three-stacked device Structure

in figure 3.2-1 [3.5].

The key to the stable operation of this stacked structure lies in precisely setting the biasing conditions for each transistor. The DC bias voltage of each gate must be carefully adjusted to ensure all three transistors operate in the saturation region, functioning as amplifiers. This effectively distributes the voltage stress so that the drain-to-source voltage (V_{DS}) across each device does not exceed its maximum rating, ultimately achieving the core objective of ensuring the oxide reliability of individual devices.

This successful voltage distribution leads to the significant outcome of greatly expanding the overall circuit's voltage headroom. The expanded headroom translates to various advantages at the system level. For instance, in Power Amplifiers (PAs) or Broadband Distributed Amplifiers (BDGAs), it allows for a larger output voltage swing, which improves maximum output power and linearity. In the case of Low-Noise Amplifiers (LNAs), the high headroom prevents the circuit from easily saturating even with strong input signals, thereby enhancing IIP3 and P1dB characteristics to secure excellent linearity.

3.3 Proposed 3.3V 4-Channel T/R Module

3.3.1 Overall Architecture

Figure 3.3-1 shows the overall block diagram of the proposed 4-channel T/R module. This module is a fully integrated front-end designed in a 65nm CMOS Bulk process, targeting high integration and performance for beamforming systems. The overall architecture consists of a common path shared by all channels and four individual T/R channels that include identical RF blocks to

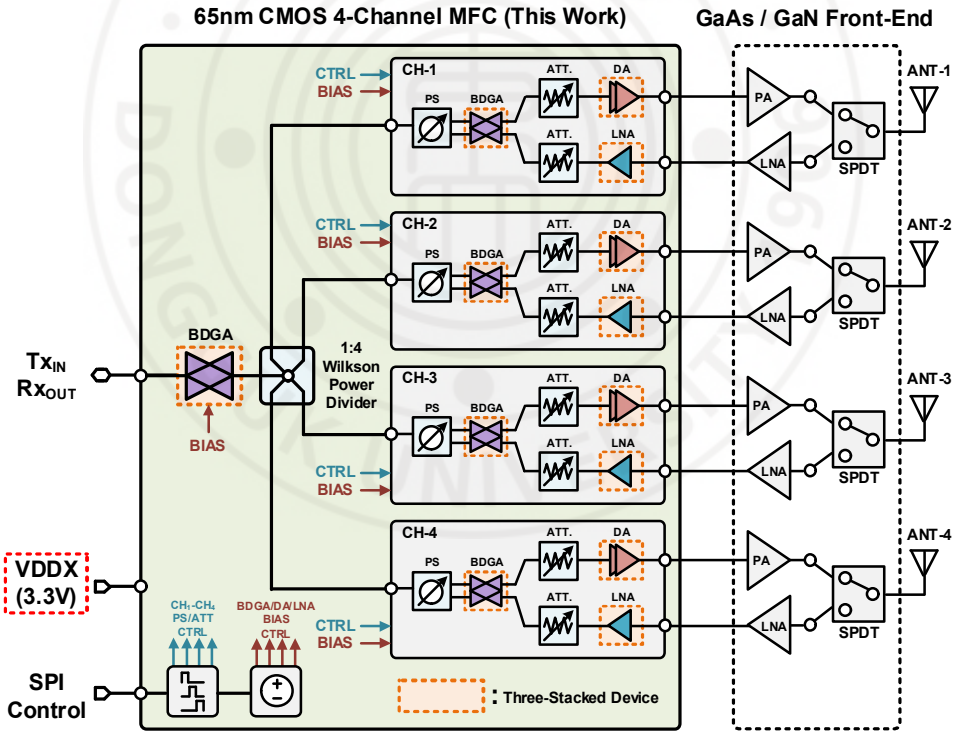


Figure 3.3-1 Total block diagram of proposed four channel T/R module

ensure channel-to-channel uniformity. A 1:4 Wilkinson power divider is placed in the module's common I/O path, which serves to divide the input RF signal equally into four channels in transmit (TX) mode and to combine the signals from each channel with low loss in receive (RX) mode.

Each of the four channels is composed of a bidirectional path that includes a Broadband Distributed Gate Amplifier (BDGA), a phase shifter (PS), an attenuator (ATT), a Power Amplifier (PA), and a Low-Noise Amplifier (LNA). One of the key features of this module's design is the common application of a 3-stack structure to all amplifier blocks: the BDGA, PA, and LNA. This structure overcomes the low breakdown voltage limitation of the 65nm process devices, enabling stable operation with a high 3.3V supply voltage. The resulting expanded voltage headroom has led to significant improvements in the amplifiers' linearity, maximum output power, and overall reliability.

Furthermore, the core beamforming blocks, the PS and ATT, were designed with the following characteristics. The PS adopts a hybrid approach combining a True-Time Delay (TTD) and a filter-type structure. Notably, the 180° phase shift is implemented using a transformer inside the BDGA, which enhances the circuit's integration level. The ATT combines T-type and π-type structures and applies impedance matching using an inductor between them to minimize insertion loss and ensure reliability.

The detailed designs of each key block are described in the following sections. The PA, LNA, and Wilkinson power divider are covered in Sections 3.3.2, 3.3.3, and 3.3.4, respectively, while the BDGA, PS, and ATT are detailed in Sections 3.3.5, 3.3.6, and 3.3.7.

3.3.2 Bi-Directional Driving Amplifier (BDGA)

A bidirectional amplifier is a circuit designed to amplify signals in both directions by sharing a single amplifier core, eliminating the need for separate transmit (TX) and receive (RX) amplifier chains. The primary advantage of this architecture is that it dramatically reduces the overall circuit size and complexity in systems like T/R modules by integrating two amplifiers into one. This plays a crucial role in minimizing chip area and power consumption in multi-channel beamformer systems.

Conventional bidirectional amplifiers, as shown in Figure 3.3-2(a), typically use a method where RF switches, such as Single-Pole Double-Throw (SPDT) switches, are placed at the input and output

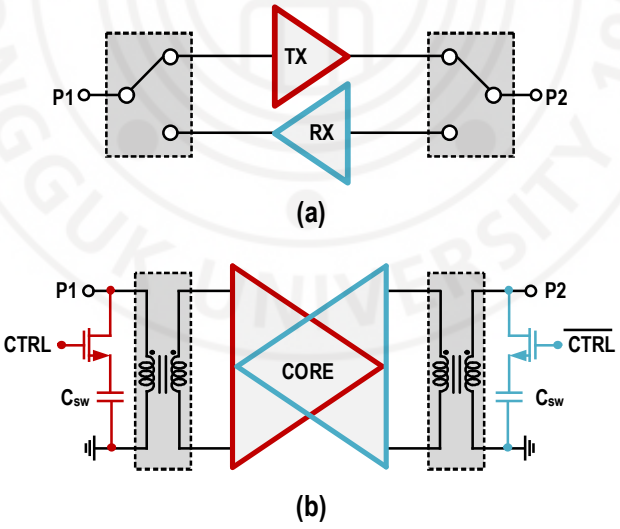


Figure 3.3-2 Block diagram of (a) conventional SPDT-based BDGA (b) proposed transformer-based BDGA with switched capacitor

of the amplifier to physically reconfigure the signal path [3.6]. While this structure has the advantage of being intuitive to design, it suffers from a fundamental limitation: the insertion loss inherent to the switch components themselves. This loss acts as a critical drawback, directly degrading the receiver's noise figure and reducing the transmitter's final output power. Furthermore, the non-linearity of the switches can also degrade the overall system linearity. To fundamentally solve the drawbacks of these switched BDGAs, a method was proposed in [3.7] that implements a bidirectional amplifier using transformers instead of external switches. However, this transformer-based approach faces its own critical matching challenge; its symmetrical topology struggles to simultaneously optimize for differing input and output impedances, leading to a degradation in matching performance.

To address this new limitation, this work proposes an improved bidirectional amplifier that reconfigures the amplifier core itself, as depicted in Figure 3.3-2 (b). The key innovation is the introduction of switched capacitors within the transformer-based resonant network. By switching these capacitors, the input and output matching can be precisely tuned for the target operating frequency in both transmit and receive modes, solving the impedance mismatch problem of previous transformer-based designs. This approach, combined with the inherent advantages of a transformer-based topology—such as high gain for a given power consumption

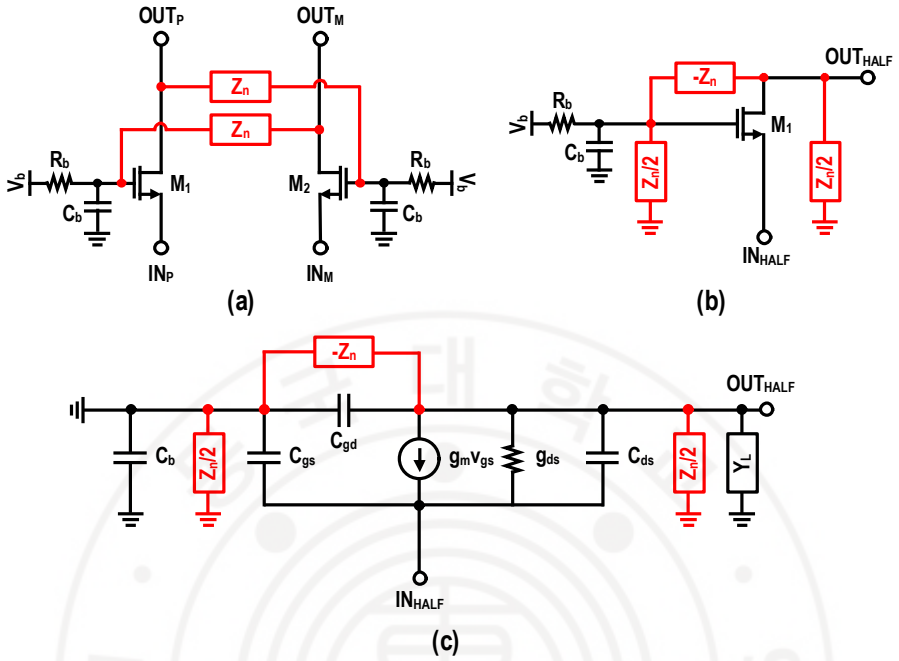


Figure 3.3-3 Differential common-gate amplifier with cross-coupled Zn feedback (a) full schematic (b) odd-mode half-circuit, and (c) small-signal equivalent model

through resonant matching and a compact chip area—enables a highly efficient bidirectional amplifier.

A bi-directional gain amplifier (BDGA) amplifies signals in both transmit and receive directions using a shared core. So, we designed and implemented BDGA with three-stacked device core to improve the integration density of the chip. However, the three-stacked topology inherently suffers from limited stability margin because parasitic components such as C_{gd},C_{gs} and bias networks are superimposed at the internal nodes between stacked devices,

making it easy to form resonant loops. In addition, due to the bi-directional amplifier operation, the reverse-direction signal path can act as an additional feedback loop, further increasing the loop gain and phase delay inside the stacked core and degrading stability. To address this issue, matching inductors can be inserted between stacked devices to stabilize the internal stack network; however, this approach inevitably increases the chip area and limits integration density.

To mitigate these intrinsic instability sources of the three-stack structure and the bidirectional feedback path within the core itself, this work adopts a cross-coupled R_n-C_n feedback network in the middle common-gate stage, depicted in Figure 3.3-3 (a). By shifting the drain and gate node admittances into a more stable region and improving the stability metrics μ, the proposed structure secures the stability of the stacked core.

Figure. 3.3-3 (b) shows the odd-mode half-circuit of the differential common-gate stage with the cross-coupled R_n-C_n feedback network. In Figure 3.3-3 (a), the two feedback branches are implemented as cross-coupled series R_n-C_n elements between the drain of one transistor and the gate of the other. For compact notation, each branch is represented by a single impedance

$$Z_n(s) = R_n + \frac{1}{sC_n} \tag{3.1}$$

Under odd-mode excitation ($V_{INP}=-V_{INM}$), the differential pair can be decomposed into two identical half-circuits referenced to a virtual ground at the common-mode plane. In this transformation, the cross-coupled network is converted into the red network shown in Figure 3.3-3 (b): each drain node sees a shunt impedance $Z_n/2$ to AC ground, while the differential coupling between the two drains appears as an effective series impedance $-Z_n$ between the drain and gate in the odd-mode half-circuit. Figure 3.3-3 (c) then augments this half-circuit with the small-signal model of the common-gate transistor(g_m,g_{ds},C_{gs},C_{gd}) and the bias decoupling capacitor, yielding the final equivalent circuit used to derive the Y-parameters and to analyze the stability factors μ of the proposed feedback structure.

Labeling the source, drain, and gate nodes as 1, 2, and 3, respectively, the 3×3 nodal admittance matrix of the half-circuit in Figure 3.3-3 (c) becomes

$$\mathbf{Y_{ij}} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} = \begin{bmatrix} Y_{gs}+Y_{ds}+g_m & -Y_{ds} & -Y_{gs}-g_m \\ -Y_{ds}-g_m & Y_{gd}+Y_n+Y_{ds} & -Y_{gd}+Y_n+g_m \\ -Y_{gs} & -Y_{gd}+Y_n & Y_{gs}+Y_{gd}+Y_n+Y_b \end{bmatrix} \quad (3.2)$$

Since the gate node is not externally accessible, it can be eliminated

using the Schur complement to obtain an equivalent 2-port with ports at the source (port 1) and drain (port 2). The reduced 2x2 Y-matrix

$$\mathbf{Y}_2 = \begin{bmatrix} y'_{11} & y'_{12} \\ y'_{21} & y'_{22} \end{bmatrix} \tag{3.3}$$

is given by

$$\begin{aligned} y'_{11} &= Y_{11} - \frac{Y_{13}Y_{31}}{Y_{33}} \quad y'_{12} = Y_{12} - \frac{Y_{13}Y_{32}}{Y_{33}} \\ y'_{21} &= Y_{21} - \frac{Y_{23}Y_{31}}{Y_{33}} \quad y'_{22} = Y_{22} - \frac{Y_{23}Y_{32}}{Y_{33}} \end{aligned} \tag{3.4}$$

Using a reference impedance Z_0, the port admittance $\mathbf{Y_2}$ is converted to S-parameters via

$$\mathbf{S} = (Y_0\mathbf{I} - \mathbf{Y_2})(Y_0\mathbf{I} - \mathbf{Y_2})^{-1}, \quad Y_0 = \frac{1}{Z_0} \tag{3.5}$$

Where I is the 2x2 identify matrix and

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}, \quad \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.6}$$

Finally, the unconditional stability of the proposed CG stage with cross-coupled feedback is evaluated using the well-known Rollet stability factors. The stability factors are defined as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S^*_{11}| + |S_{12}S_{21}|} \tag{3.7}$$

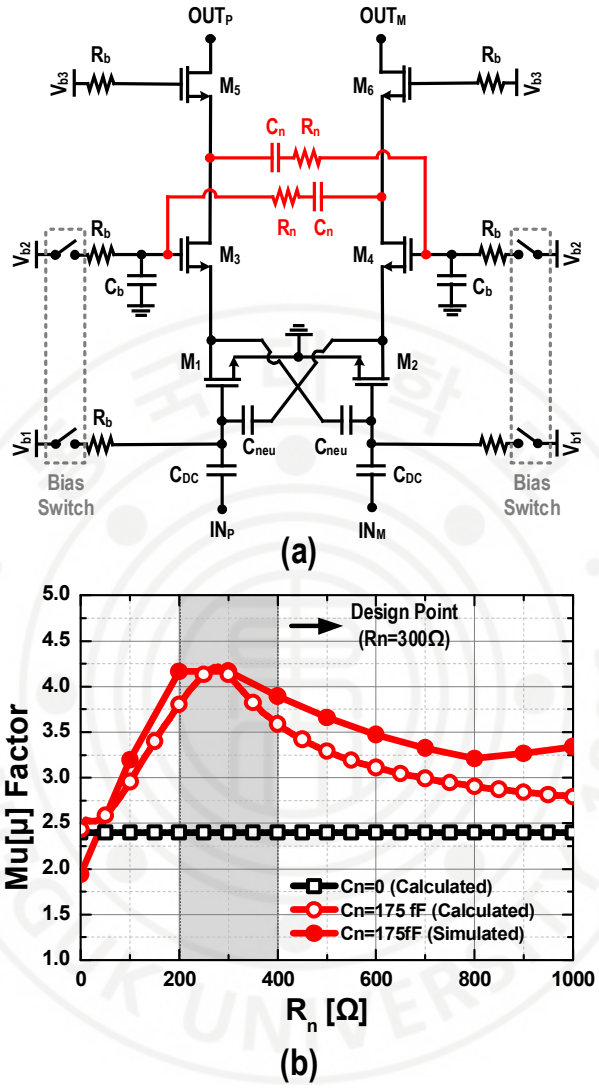


Figure 3.3-4 Schematic of three stacked device with R_n-C_n cross-coupled feedback and (b) calculated and simulated μ -factor

where *denotes complex conjugation. A two-port is unconditionally stable for all passive source and load impedances if and only if μ is larger than unity.

Figure 3.3-4 (a) shows the three-stacked device implemented with the proposed R_n-C_n cross-coupled feedback structure. The first-stage devices (M_1-M_2) form a common-source (CS) amplifier, to which a neutralization capacitor is applied. This cancels the effective C_{gd}, suppressing Miller feedback, thereby improving stability and enhancing high-frequency gain. In this design, the capacitor C_n was set to 175 fF to achieve optimal matching at the center frequency of 9 GHz. Using this value as the baseline, R_n was swept and the corresponding stability factor μ was calculated from (3.4)-(3.7) and compared with circuit-level simulations, showing very good agreement, as summarized in Figure 3.3-3 (b). It can be observed that when $R_n \approx 300\ \Omega$, the resulting μ is clearly improved compared with the case without the proposed feedback, so C_n=175 fF and R_n=300 Ω were chosen as the design point.

we adopt a transformer-based BDGA implemented with this three-stacked device topology, depicted in Figure 3.3-5 Conventional BDGAs rely on RF switches to select the path, which adds insertion loss and degrades noise figure and efficiency. A transformer-based BDGA avoids series switches: by bias-reconfiguring the core and exploiting magnetic coupling, the signal path is reversed with minimal loss [3.7]. Identical differential transformers are placed symmetrically at the input and output; each primary is center-tapped to V_{DD} to provide bias while maintaining symmetry. The core employs a push-pull amplifier topology. The

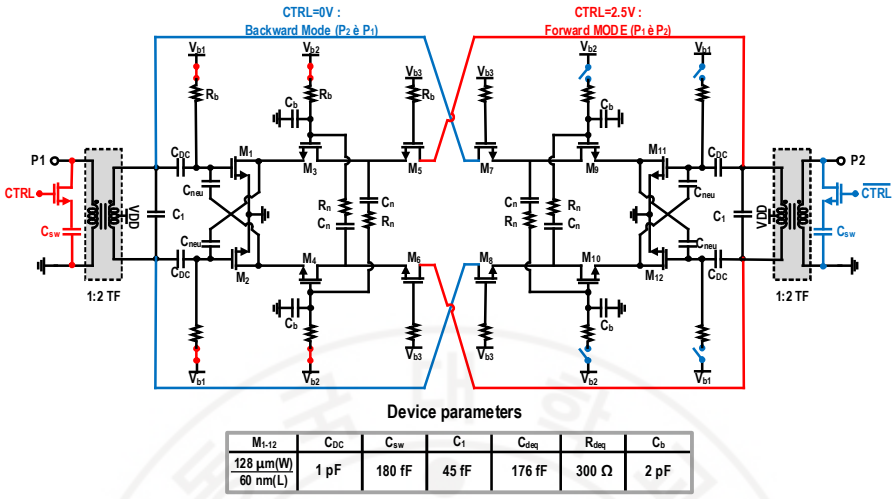


Figure 3.3-5 Proposed transformer-based BDGA employing a three-stacked device.

V_{DD} connected to the input gate is isolated by a DC-blocking capacitor. The gate biases of the first and second transistors in the three-stack (M_1-M_4) are selectively disabled via switches along the inactive path. Disabling only the first device is insufficient—large output swing can couple through parasitics and partially turn on the opposite branch—so both the first and second devices are gated off to ensure isolation.

As noted earlier, the BDGA employs identical transformers at the input and output to realize symmetric forward/reverse operation. Because the port impedances differ, achieving resonance at the same frequency requires different shunt capacitances on the two sides. To accommodate this, Figure 3.3-6 (a) adopts a switched-capacitor shunt across each transformer. When the switch is ON, the branch behaves as a R_{on}-C_{sw} series to ground; when the switch

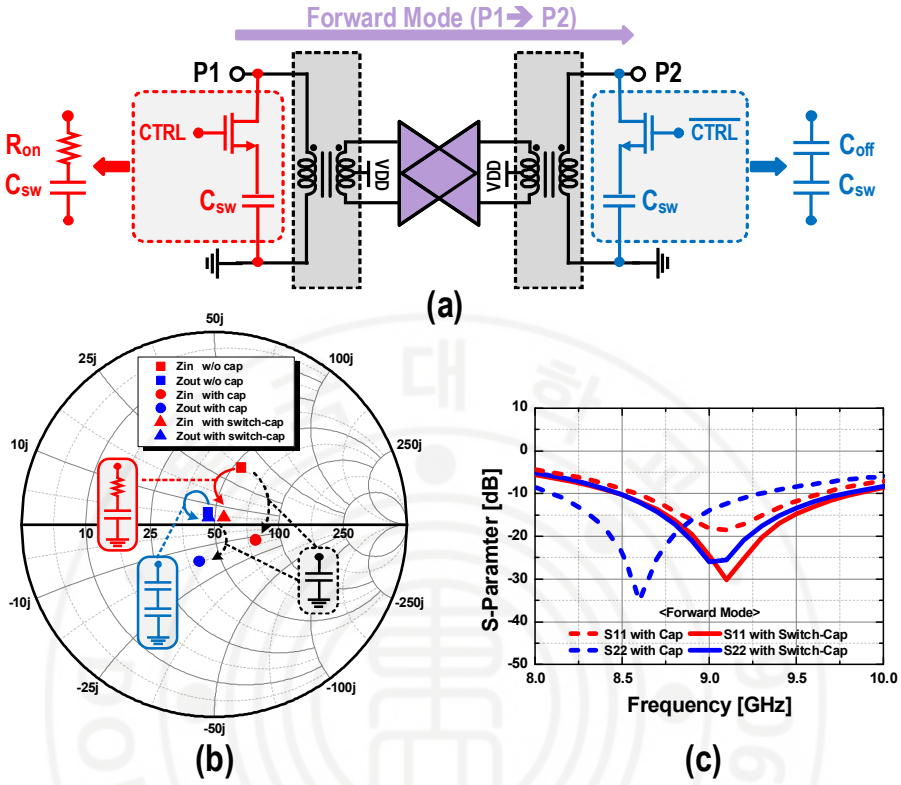


Figure 3.3-6 Forward-mode operation of the proposed BDGA: (a) block diagram and I/O matching schematic; (b) Smith-chart of input/output impedances with the 9-GHz (c) simulated S_{11} and S_{22} comparing capacitor and switched-capacitor configurations

is OFF, the device presents a small series capacitance so the effective shunt C decreases. This allows each port to be tuned to the same resonant frequency despite unequal impedances. Figure 3.3-6 (b) plots Smith-chart loci at 9 GHz for three cases: before matching, with a fixed shunt capacitor, and with the proposed switched capacitor. With a fixed capacitor, matching Z_{in} over-pulls Z_{out}, detuning S_{22} at the center frequency, as seen in Figure 3.3-6

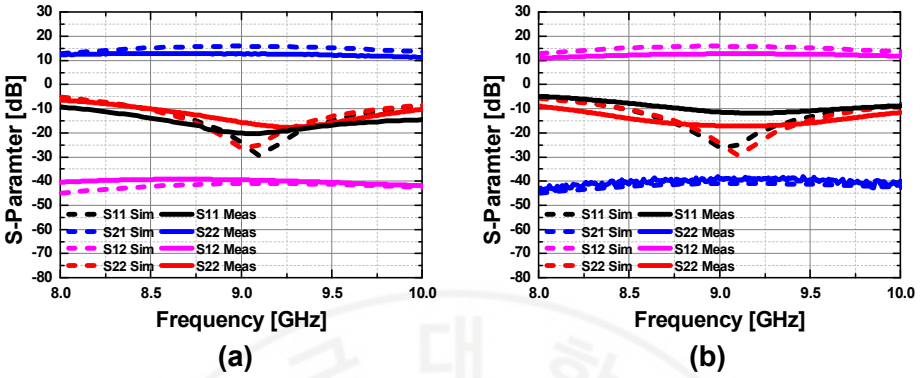


Figure 3.3-7 Simulation and measured results of proposed BDGA (a) forward mode (b) backward mode

(c). In contrast, the switched-capacitor keeps Z_{in} near 50-Ω while the already near-matched Z_{out}, so both ports resonate at 9GHz simultaneously, which is confirmed by the aligned minima of S_{11} and S_{22} in Figure 3.3-6 (c).

Figure 3.3-7 presents the simulation and measurement results of the proposed BDGA. The data confirm that the forward and reverse modes exhibit nearly identical performance, and that the input and output matching are formed as intended around 9 GHz, achieving closely aligned resonance on both ports

3.3.3 Power Amplifier (PA)

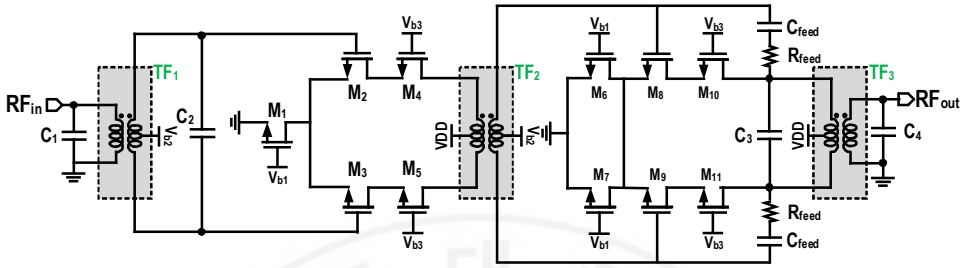


Figure 3.3-8 Schematic of the proposed 2-stage, 3-stack transformer-matched power amplifier.

A Power Amplifier (PA) is a key component in a transmitter's signal chain, designed to boost the power of a radio frequency (RF) signal to a sufficient level for transmission through an antenna. The primary goals for a PA are to deliver high output power with maximum efficiency and minimal distortion (high linearity)

Figure 3.3-8 shows the complete schematic of the proposed 2-stage power amplifier. Each stage of this power amplifier is implemented with a 3-stack structure in a push-pull topology to secure high breakdown voltage and gain, and it adopts a transformer matching technique for inter-stage and output matching. Notably, a tail current source was added to the 3-stack structure. This ensures a stable bias current against process, voltage, and temperature (PVT) variations and significantly improves the Common-Mode Rejection Ratio (CMRR), which enhances the amplifier's immunity to common-mode noise and improves overall

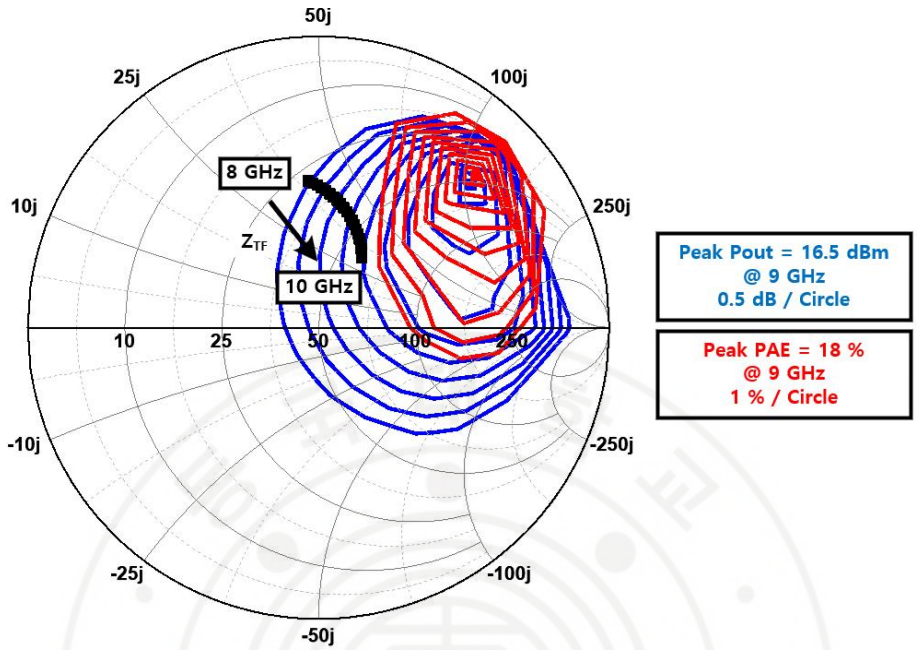


Figure 3.3-9 Load-pull simulation results for the power amplifier at 9.5 GHz, showing contours for output power (Pout, in blue) and PAE (in red)

system efficiency. Furthermore, an RC feedback structure was applied to the second stage, the final output stage, to adjust the output impedance and lower the Q-factor, through which broadband output matching characteristics were achieved [3.8].

Figure 3.3-9 shows the load-pull simulation results for the power amplifier (PA) at 9.5 GHz. This Smith Chart displays the optimal impedance regions for maximum output power (Pout, blue contours) and maximum power-added efficiency (PAE, red contours). As can be seen, the points for peak Pout and peak PAE are located away from the 50-ohm matching point. Since a stable

50-ohm match was also a critical consideration for this design, the output matching network was designed to find an optimal trade-off by simultaneously considering all three factors: maximum Pout, maximum PAE, and the 50-ohm match.

3.3.4 Low Noise Amplifier (LNA)

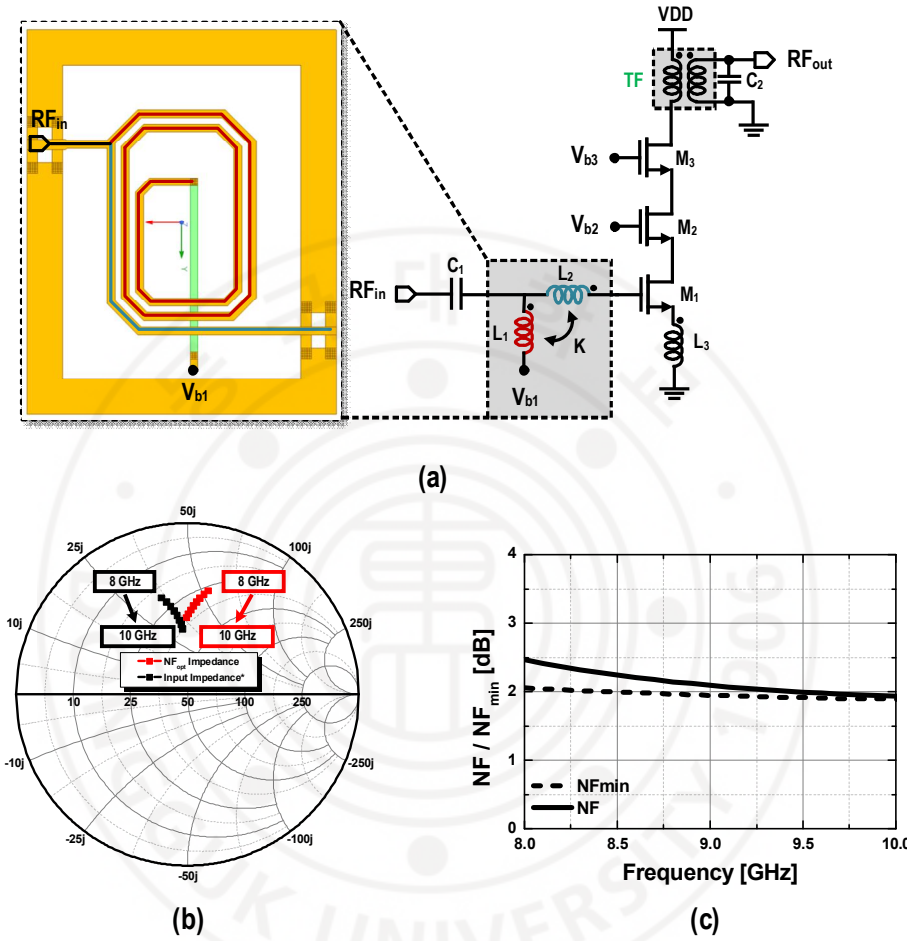


Figure 3.3-10 (a) Schematic of low noise amplifier employing a three-stacked device (b) smith-chart of Z_{opt}, NF and input conjugate impedance; (c) simulated noise figure and NF_{min}

A Low-Noise Amplifier (LNA) is the first active block in a receiver front-end, designed to amplify a very weak incoming

signal from an antenna while adding as little noise as possible. The noise performance of the LNA is critical as it effectively sets the sensitivity for the entire receiver system.

Figure 3.3-10 (a) shows the detailed schematic of the proposed LNA. This LNA is designed based on a 3-stack device structure to achieve high gain and linearity, and to ensure stable operation at high voltages.

A key feature of this LNA design is the broadband matching technique applied to the input and output stages. For the input stage, a T-coil matching network was applied to significantly extend the LNA's operating bandwidth [3.9]. Unlike a conventional LC matching circuit, which shows optimal performance only at a single frequency, the T-coil structure effectively cancels the transistor's input capacitance over a wide range of frequencies. In conjunction with this, a source degeneration inductor was used to simultaneously optimize the noise figure and stability.

A transformer-based matching technique was adopted for the output stage. This efficiently matches the amplifier's output impedance to the load impedance (50 Ω), minimizing the power loss of the amplified signal and maximizing transfer efficiency. Through this input and output matching strategies, the proposed LNA can achieve excellent performance across the entire target X-Band

Figure 3.3-10 (b) is the NF_{opt} trace (red) on the Smith Chart from 8 GHz to 11 GHz, which represents the optimal source impedance NF_{opt} that the LNA must see at its input to achieve its minimum noise figure (NF). Since the primary goal of an LNA is to optimize noise performance, the input matching network applied in this design—consisting of the T-coil and the source degeneration inductor—was designed with the key objective of matching the 50-ohm source impedance as closely as possible to this NF_{opt} trace. Figure 3.3-10 (c) shows the simulated noise figure.

3.3.5 1:4 Wilkinson Power Divider

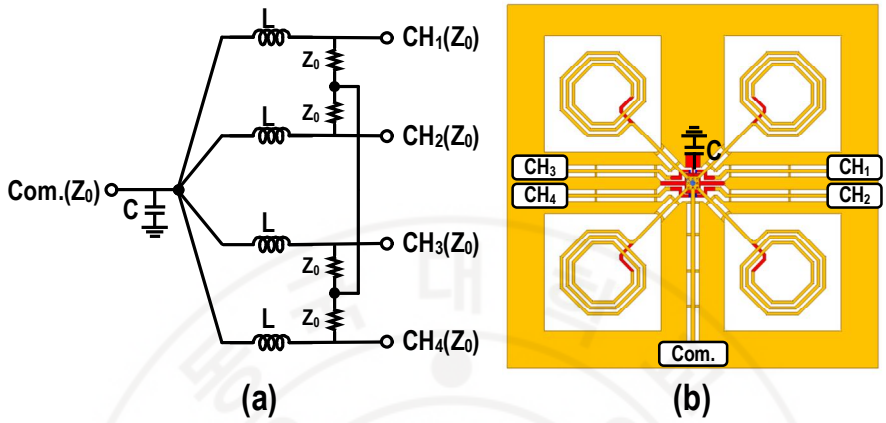


Figure 3.3-11 (a) schematic of 1:4 Wilkinson power divider (b) Top View of Full 3-D electromagnetic (EM) model in HFSS

The Wilkinson power divider is a key passive component widely used in RF systems to equally divide a single signal into multiple channels or to combine signals from multiple channels with low loss. The reason this divider is essential, especially in multi-channel systems, is because of its high isolation characteristic between each output port. This high isolation prevents a reflected signal from one channel from affecting the other channels, playing a crucial role in ensuring the stability and signal integrity of the entire system.

Figure 3.3-11 shows the schematic and HFSS 3D model of the 1:4 Wilkinson power divider used in the common path of the proposed 4-channel T/R module. Typically, a 1:4 divider is implemented by cascading three 1:2 dividers, but this approach has

the drawbacks of a complex structure and accumulated loss [3.10] In this design, we actively leverage the advantage of the multi-layer metal interconnects in the CMOS process, which allow for a high degree of freedom in designing complex 3D transmission line structures. This enables a new architecture that divides the power directly from 1-to-4 in a single stage. This structure reduces the overall circuit size and minimizes the additional loss that occurs in a multi-stage design [3.11].

Furthermore, with the primary goal of minimizing insertion loss, we intentionally omitted the typically used output matching capacitors in this design. While this choice carries a trade-off of potentially degrading the output return loss characteristics, simulation results confirmed that an excellent return loss of less than -10 dB was maintained across the entire target band even without the capacitors. Since this is a fully acceptable level from an overall system perspective, we adopted a design that improves insertion loss by sacrificing some matching performance, thereby enhancing the overall system efficiency.

3.3.6 Phase Shifter (PS)

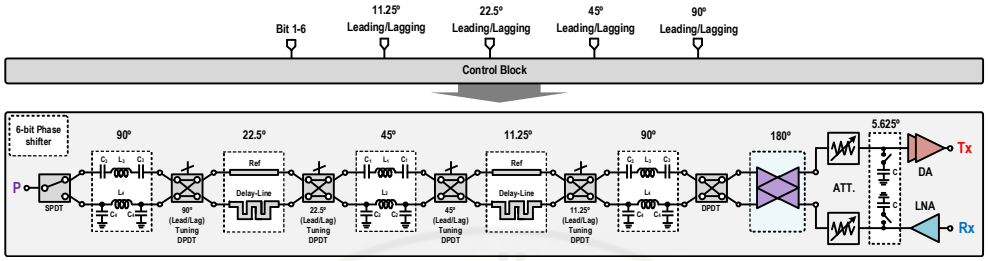


Figure 3.3-12 Block diagram of the designed 6-bit, 360° phase shifter.

A phase shifter is a key block in a multi-channel T/R module that enables beamforming by precisely controlling the phase of each channel's signal. The phase shifter proposed in this work, as shown in the block diagram in Figure 3.3-12, is designed with a 6-bit control structure to cover a full 360° range with a least significant bit (LSB) of 5.625°.

The smaller phase bits, 11.25° and 22.5°, adopt the delay line method. This approach creates a phase difference using the time-of-flight difference between a reference line and a physically longer delay line. This relationship is defined in Equation (3.1):

$$\Delta\phi = \omega\Delta\tau \tag{3.1}$$

where $\Delta\phi$ is the resulting phase difference in radians, ω is the angular frequency of the signal ($2\pi f$), and $\Delta\tau$ is the difference in propagation time between the two lines in seconds. Compared to

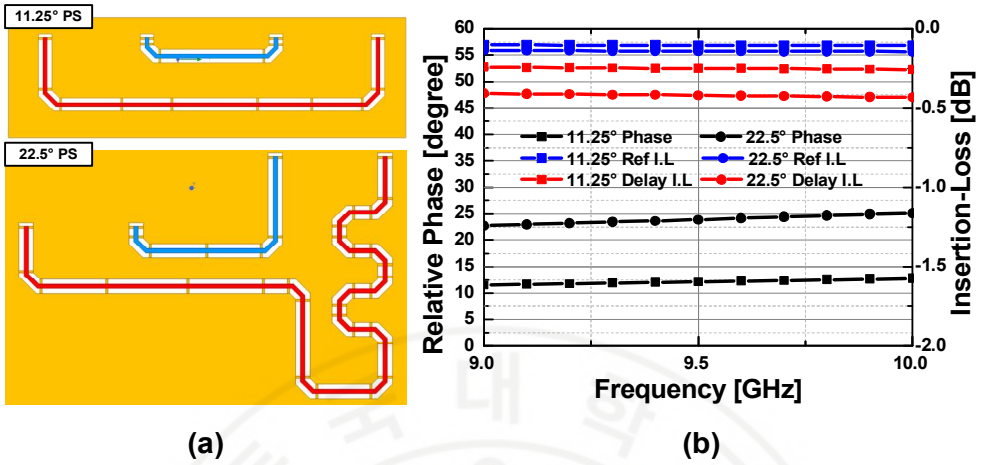


Figure 3.3-13 Phase shifter of 11.25° and 22.5°: (a) HFSS 3-D top view and (b) simulated relative phase and insertion loss.

filter-based structures, the delay-line method's simple transmission-line architecture offers advantages like lower insertion loss, simpler design, and flexible layout area through meandering. Here is the updated sentence. Figure 3.3-13 shows the HFSS 3D model and simulation results of the delay-line structure. (In the 3D model, the reference line is shown in blue, and the delay line is in red). Within the target 9-10 GHz band, the phase error is less than 2.5°, and the maximum insertion loss for the 22.5° bit is below 0.4 dB, confirming excellent performance.

A drawback of the delay-line method is that its frequency-dependent phase error increases with larger phase shifts. To compensate for this, the larger phase bits, 45° and 90°, are

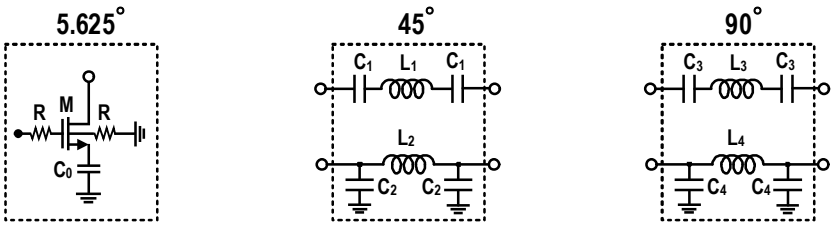
implemented using a method that combines a π-type C-L-C Band-Pass Filter with a Low-Pass Filter. Notably, the 90° bit is realized by cascading two 45° cells. This avoids the problems of a single C-L-C HPF design for 90°, which would be vulnerable to ground inductance and could suffer from a low Self-Resonant Frequency (SRF) due to the large required inductor. The proposed two-stage 45° structure effectively resolves these issues.

Furthermore, a tuning circuit has been added to the DPDT switch itself to correct for phase errors that may arise from process variations or EM modeling inaccuracies. This circuit adds switched capacitors to both the leading and lagging paths within the switch. If the actual phase difference is smaller than the designed value, the capacitor on the lagging path is turned on to increase the total phase difference. Conversely, if the phase difference is too large, the capacitor on the leading path is turned on to reduce the total phase difference. This error correction technique is applied to the 11.25°, 22.5°, 45°, and 90° bits, significantly improving the phase shifter's overall accuracy.

The LSB of 5.625° is implemented using a switched capacitor. Located between the ATT and the amplifier, this cell uses the principle of signal lagging caused by a parallel capacitor when its switch is activated. The 180° MSB is realized using the 180°

phase-inverting function of the multi-functional BDGA's transformer which increases integration by eliminating a separate circuit. Figure 3.3-14 shows the detailed schematics of the 5.625°, 45°, and 90° cells.

Figure 3.3-15 depicts the differential BDGA configured to provide a 180° phase inversion together with TX/RX path reconfiguration. Matching switched capacitors are connected to the differential transformers so that, by enabling a single side, the network behaves effectively as a balun. Controlling the DPDT thus yields the required 180° inversion while simultaneously switching between transmit and receive paths.



Device parameters

M	C_0	R	L_1	L_2	C_1	C_2	L_3	L_4	C_3	C_4
32um/60nm	80 fF	5 kΩ	590 pH	550 pH	800 fF	145 fF	510 pH	510 pH	800 fF	155 fF

Figure 3.3-14 Schematics of the phase shifter cells: (a) 5.625° switched-capacitor type, (b) 45° filter-type, and (c) 90° stage using two cascaded 45° cells.

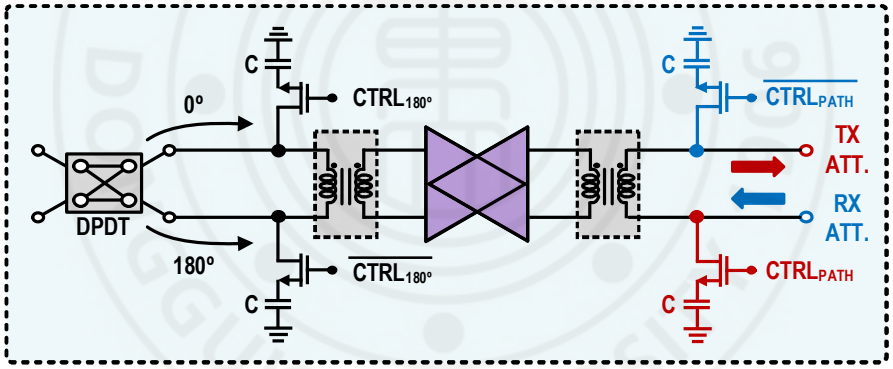


Figure 3.3-15 Block diagram of differential BDGA performing 180º phase shifting and Tx/Rx path switching

3.3.7 Attenuator (ATT)

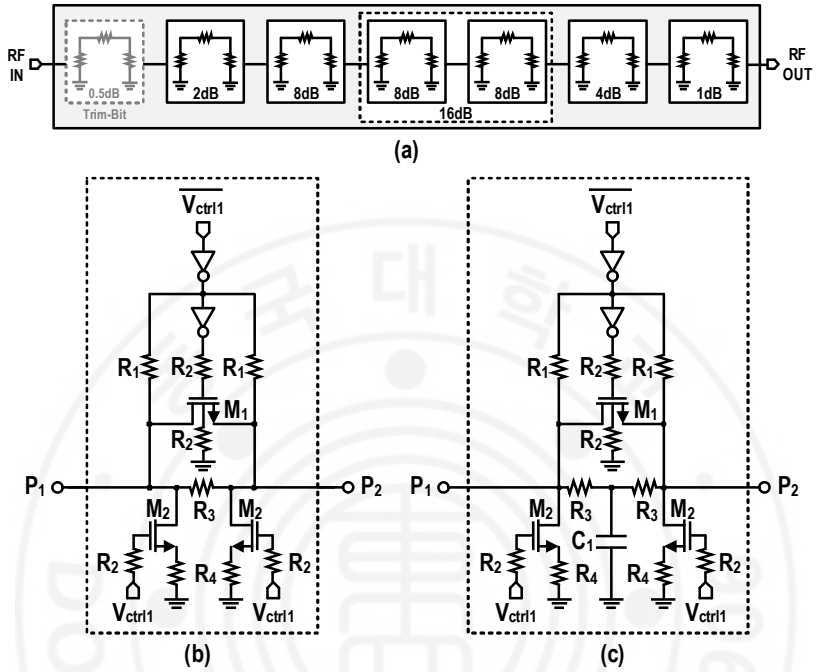


Figure 3.3-16 (a) Block diagram of the 5-bit attenuator with one trim bit and the schematic of a π-type cell; (b) 0.5, 1, 2, and 4 dB cells; (c) 8 dB cell.

The attenuator is designed to provide a 0–31 dB range in 1 dB steps, with an additional 0.5 dB trim bit, as depicted in Figure 3.3-16 (a), and employs a resistive π-type network to guarantee accurate impedance matching. Figure 3.3-16 (b) and (c) shows the schematics of the attenuator cells (including the trim bit). Each 8 dB cell includes an auxiliary capacitor to suppress the phase error introduced by signal attenuation, and the 16 dB step is realized by cascading two 8 dB cells.

3.3.8 Chip Photograph

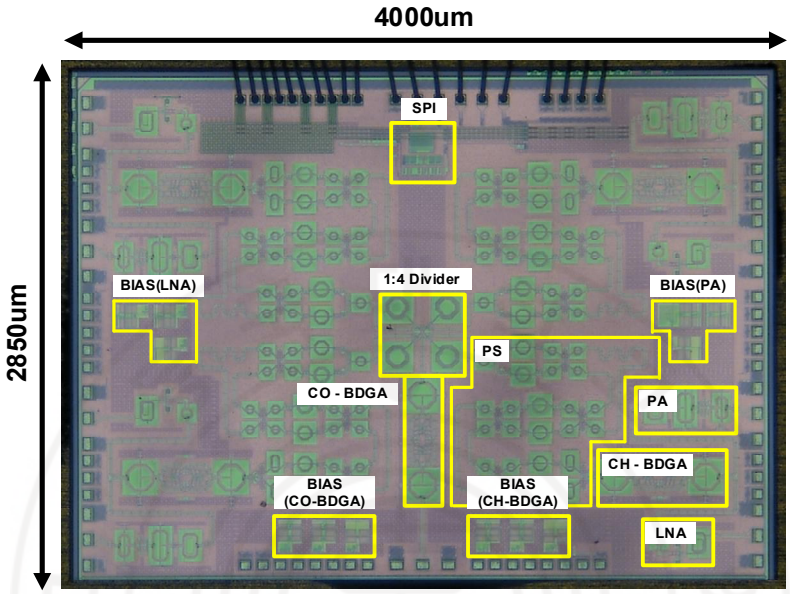


Figure 3.3-17 Chip photograph of the proposed 4-channel T/R module (4000 μm × 2850 μm).

Figure 3.3-17 shows the chip photograph of the proposed 4-channel transmit/receive (T/R) module. The chip was fabricated using the 65nm CMOS process, and its total size, including the pads, is 4000 μm × 2850 μm. Integrated within the chip for each channel are the previously described 1:4 Wilkinson divider, a 3-stack BDGA, a PA, an LNA, and a 6-bit phase shifter and attenuator. Furthermore, it can be seen that the bias circuits (designed by Jun Kwon) and a 128-bit SPI circuit (developed by Jeong-Moon Song) for controlling the operation of these blocks are also integrated together.

3.4 Measurement Result

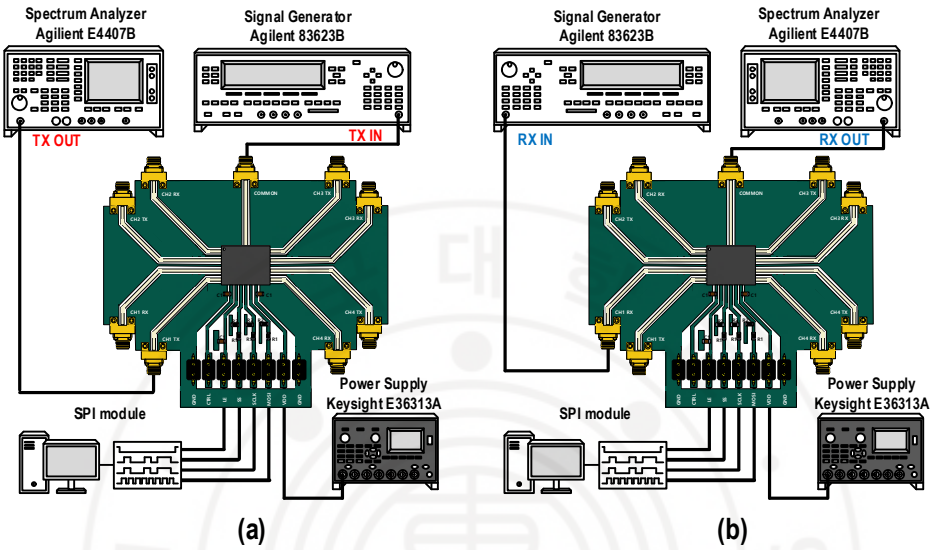


Figure 3.4-1 Measurement setup for the 4-channel T/R module: (a) Small-signal S-parameter measurement, (b) Large-signal measurement

Figure 3.4-1 illustrates the measurement setup for verifying the performance of the fabricated 4-channel transmit/receive module. The fabricated chip was mounted on a test PCB in a custom LGA (Land Grid Array) package, as described in [3.16], for characterization.

Figure 3.4-1 (a) shows the setup for small-signal S-parameter measurements. A Keysight N5224A Network Analyzer was used to measure the gain and return loss characteristics of each channel. Figure 3.4-1 (b) depicts the setup for large-signal measurements, where an Agilent 83623B Signal Generator provides

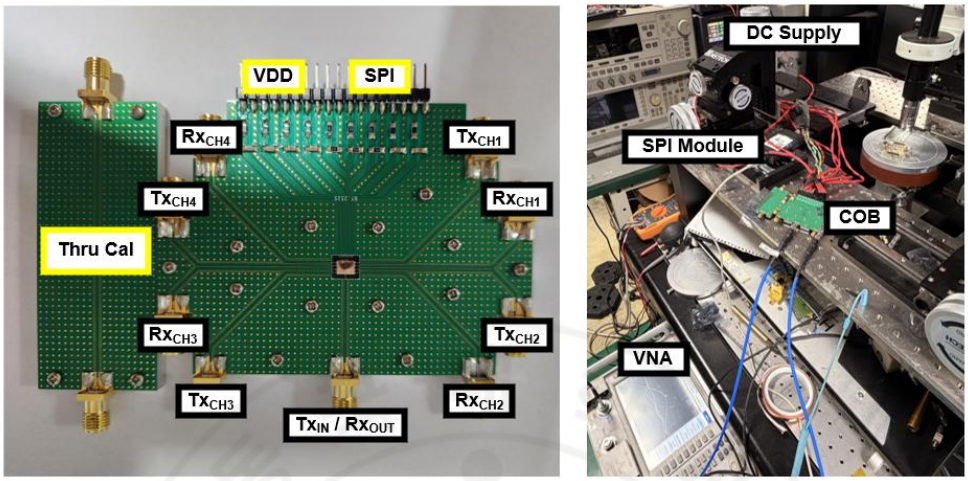


Figure 3.4-2 Photograph of (a) the fabricated 4-channel LGA T/R module evaluation board and (b) its small-signal measurement setup

the input signal, and an Agilent E4407B Spectrum Analyzer is used to analyze the output power and spectral characteristics. In both setups, a Keysight E36313A Power Supply provided the DC power, and an SPI module connected to a PC was used to digitally control the internal states of the chip, such as phase and attenuation.

Figure 3.4-2 shows the fabricated 4-channel Land Grid Array (LGA) module and the small-signal measurement setup

3.4.1 Small Signal Measurements

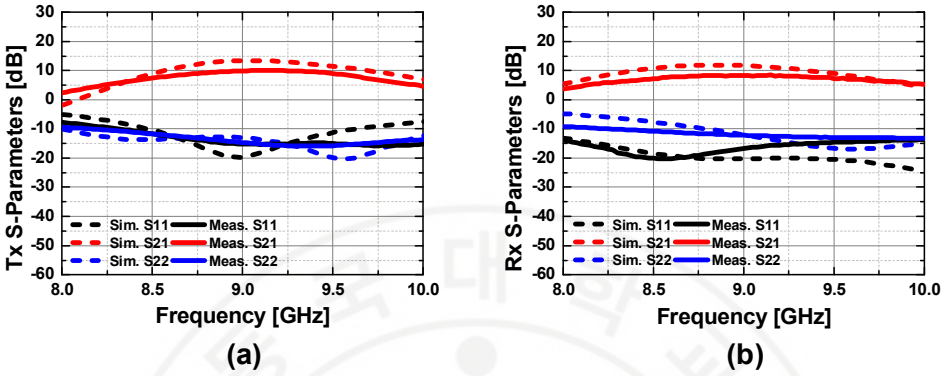


Figure 3.4-3 Comparison of Measured and Simulated S-Parameters: (a) Transmit (Tx) Mode, (b) Receive (Rx) Mode

Figure 3.4-3 shows a comparison between the measured and simulated small-signal S-parameters of the fabricated 4-channel transmit/receive module. Figure 3.4-3 (a) presents the performance in transmit (Tx) mode. The measured peak gain is 9.5 dB, with a 3-dB bandwidth from 8.7 GHz to 9.5 GHz. The power consumption in this mode is 200 mA from a 3.3V supply. Figure 3.4-3 (b) shows the performance in receive (Rx) mode, where the measured peak gain is 9 dB and the 3-dB bandwidth is from 8.5 GHz to 9.7 GHz. The power consumption in receive mode is 135mA from a 3.3V supply.

Figure 3.4-4 shows the measured phase performance of the integrated 6-bit phase shifter. Figure 3.4-4 (a) and 3.4-4 (b) present the results for the transmit (Tx) and receive (Rx) modes,

respectively. Both plots demonstrate that all 64 discrete phase states (black solid lines), corresponding to the 6-bit control, are stably implemented across the entire X-Band (8.0-10.0 GHz). The RMS phase error (red dotted line) shown at the bottom remains low, below 5.625° , across the entire band for both Tx and Rx modes, proving that the designed phase shifter operates with high accuracy.

Figure 3.4-5 shows the measured attenuation performance of the integrated 5-bit attenuator. Figure 3.4-5 (a) and 3.4-5 (b) present the results for the transmit (Tx) and receive (Rx) modes, respectively. Both plots demonstrate that all 32 discrete attenuation states (black solid lines), corresponding to the 5-bit control, are stably implemented across the entire X-Band (8.0-10.0 GHz). The RMS gain error (red dotted line) shown at the bottom is within 0.6 dB across the entire band for both Tx and Rx modes.

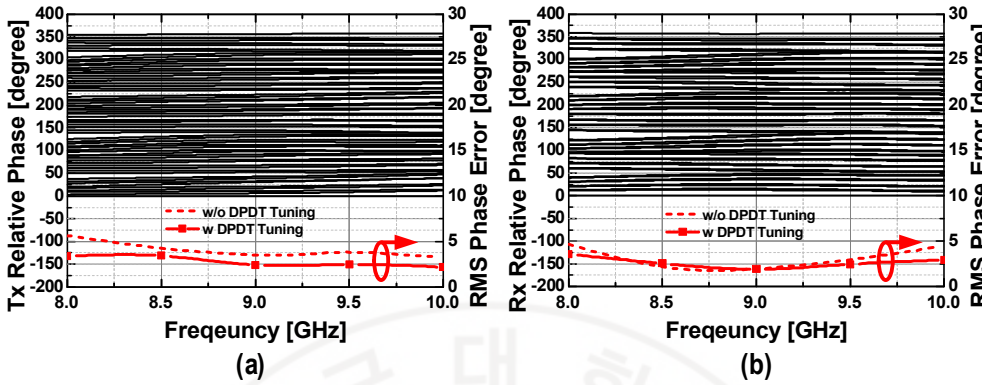


Figure 3.4-4 Measured Relative Phase and RMS Phase Error: (a) Transmit (Tx)

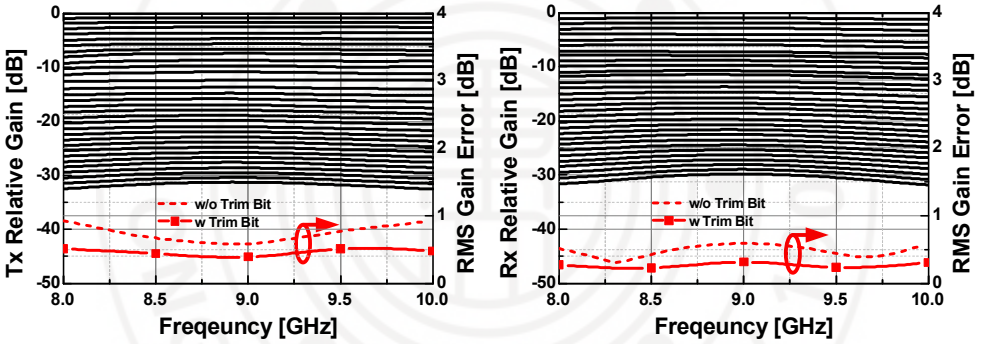


Figure 3.4-5 Measured Relative Gain and RMS Gain Error: (a) Transmit (Tx) Mode, (b) Receive (Rx) Mode

3.4.2 Large Signal Measurements

Figure 3.4-6 presents the transmitter Psat and OP1dB, where at the center frequency of 9 GHz the measured Psat and OP1dB are 7.9 dBm and 5.3 dBm, respectively. Figure 3.4-7 shows the input 1-dB compression point (IP1dB) for the receive path, which is better than -14.8 dBm across 8–10 GHz, demonstrating adequate linearity of the RX chain.

The noise figure (NF) was measured using the Y-factor method with an Agilent 346C-K01 noise source. In Figure 3.4-8, The minimum NF is 6.2 dB at 9 GHz, and within the 3-dB bandwidth (8.5–9.8 GHz) the NF remains below 7.8 dB.

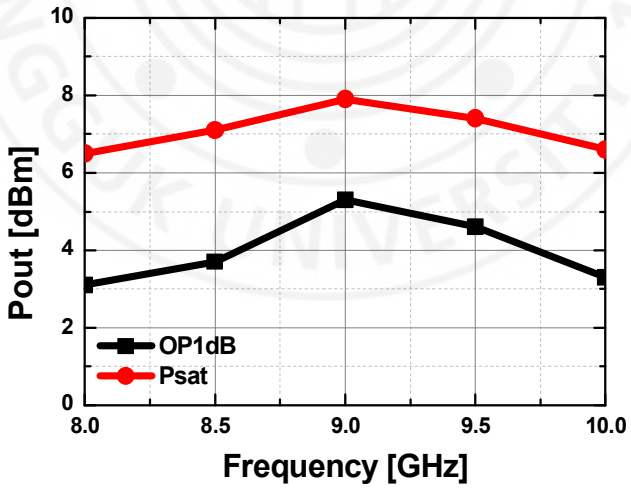


Figure 3.4-6 Measured Saturated power and OP1dB in Tx mode

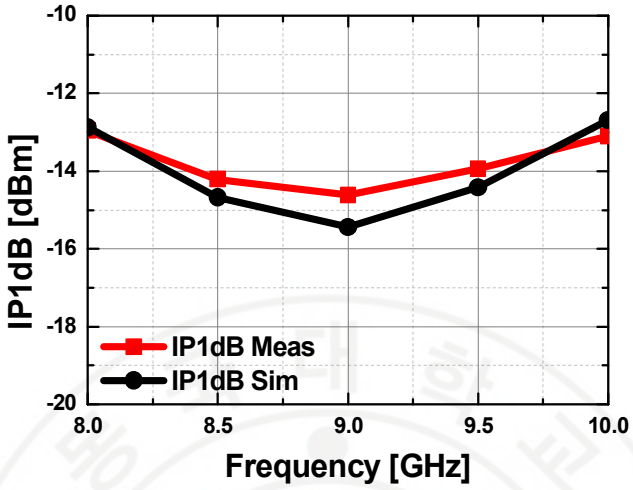


Figure 3.4-7 Measured and simulated IP1dB in Rx mode

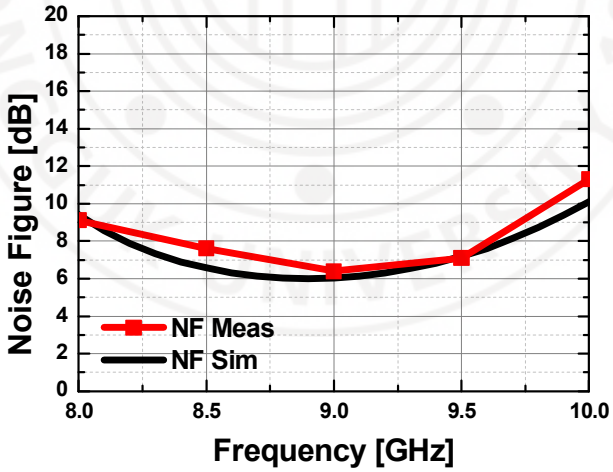


Figure 3.4-8 Measured and simulated noise figure in Rx mode

3.4.3 Comparison with other T/R Modules

Table 3.4-1 presents a comparison of the key performance metrics of the beamformer chip designed in this work against other recent studies. The circuit of this work, fabricated in a 65nm CMOS process, features a complete transceiver architecture by integrating four transmit (Tx) and four receive (Rx) channels onto a single chip. This is a distinct advantage that differentiates it from the works in [3.4], [3.12], and [3.14], which implement only a transmitter or a receiver. In terms of performance, the proposed circuit achieves high resolution in phase and gain control, which are essential for beam steering. The phase can be controlled with a fine step of 5.625° and the gain with a 0.5 dB step, making it highly suitable for precise beam pattern shaping. Furthermore, it secures a decent and stable gain of 10 dB for both the transmitter and the receiver. Particularly noteworthy are its power consumption and chip area efficiency. The power consumption of 289 mW per Tx channel and 182 mW per Rx channel is significantly lower compared to the chips with a similar 4Tx/4Rx architecture, such as [3.13] and [3.15]. Moreover, the chip area of 11.4 mm^2 is considerably smaller than that of the chip in [3.13], which occupies a much larger area (49 mm^2) despite using a more advanced technology node (45nm SOI). This confirms the excellent competitiveness of our design in terms of integration density and power efficiency.

Table 3.4-1 Comparison table of X-Band 4-channel T/R module

TABLE I. COMPARISON OF STATE-OF-THE-ART MFC AROUND THE X-BAND

Ref.		This work	[3.3]	[3.4]	[3.13]	[3.15]	[3.17]	[3.18]	[3.19]
Tech		65nm CMOS	130nm CMOS	130nm CMOS	45nm SOI	130nm CMOS	65nm CMOS	130nm CMOS	130nm CMOS
Topology		4Tx / 4Rx	1Tx / 1Rx	4Tx	4Tx / 4Rx	4Tx / 4Rx	1Tx / 1Rx	1Tx / 1Rx	1Tx / 1Rx
Frequency [GHz]		8.5-9.7	8.5-10.5	7.9-9.6	8-12	9-10	8-10.5	9-10.5	8.5-10
Gain [dB]	Tx	9.5†	3.5	11.5	N/A	12	3.7	20	11
	Rx	9†	3.5	-	21	9	3.7	12	12
Rx NF [dB]		7.8	8.5	-	3.4	N/A	10	8.5	8.2
Gain Tuning Range/bit [dB]		31 / 5 (+1 trim)	31 / 1	5 / 3	N/A / 6	31 / 5	31.5 / 0.5	31.5 / 0.5	31.5 /0.5
RMS Gain Error [dB]		0.6 / 0.55*	0.3	0.5	N/A	0.4	0.5	0.44	0.25
Phase Step [°]		5.625	5.625	22.5	5.625	5.625	5.625	5.625	5.625
RMS Phase Error [°]		5.5 / 2.7**	4.3	6	3.5	2.3	4	4.3	2
RX IP1dB [dBm]		-14.8†	N/A	-	N/A	N/A	N/A	N/A	0
Pdc/ CH [mW]	Tx	200	150	217.5	1625	800	170	250	640
	Rx	135	150	-	188	800	170	120	670
Chip Area/CH [mm²]		2.85 (with ESD)	1.19	2.18	12.25	2.8	9.56	17.2	12.8

* with Trim Bit
** with DPDT Tuning
† LGA Packaging
‡ QFN Packaging

3.5 Reference

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Chapter 4. A D-Band Beamforming Transceiver Using LO-Path Time Delaying for RF Phase Alignment in 28nm FDSOI

4.1 Idea of LO-Path Time Delaying for RF Phase Alignment

Beamforming systems can be broadly classified into RF, IF, and LO beamformers, depending on the location where phase control is performed. These architectures are typically implemented using either Phase Shifters (PS) or True Time Delay (TTD) units. However, when these methods are applied to the wideband signals in the Sub-THz band, a candidate for 6G, they face distinct technical limitations. The most common PS-based beamformer causes a phenomenon known as "beam squint," where the beam's direction changes with frequency in wideband signals. This is a critical issue that severely degrades communication quality, making it detrimental for 6G systems that utilize wide bandwidths.

To solve this problem, a TTD-based beamformer can be applied. A TTD delays the signal's time, rather than its phase, allowing it to maintain a constant beam direction regardless of frequency. However, applying TTDs to conventional architectures presents the following limitations.

First, in an RF beamformer architecture, applying a TTD directly in the high-frequency Sub-THz band results in a drastic increase in the insertion loss of the TTD circuit itself. As pointed out in Table 4.1-1, even the highest-performing TTD reported in the 140 GHz band has an insertion loss exceeding 20 dB, making its practical system application infeasible [4.1]. This substantial loss severely deteriorates the transmitter's power efficiency and the receiver's Noise Figure, creating a significant technical challenge for overall system performance.

Second, applying a TTD in an IF beamformer architecture is unsuitable for wideband Sub-THz systems because the frequency ratio difference (ω_{RF}/ω_{IF}) between the RF and IF signals actually exacerbate the beam squint problem. As such, conventional beamformer architectures show clear limitations in satisfying the wideband requirements of the Sub-THz band.

To overcome these technical challenges, the design is focuses on applying a TTD to the LO beamformer architecture. As specified in Table 4.1-1, simply applying a TTD in the LO path can cause beam squint, as the effective time delay varies with the RF frequency ($\theta_{LO}=\omega_{LO}\times\tau_{d(LO)}$). However, this effect is relatively insignificant compared to other methods, thanks to the very high center frequency of the Sub-THz band.

The presented transceiver design is mainly focused on the

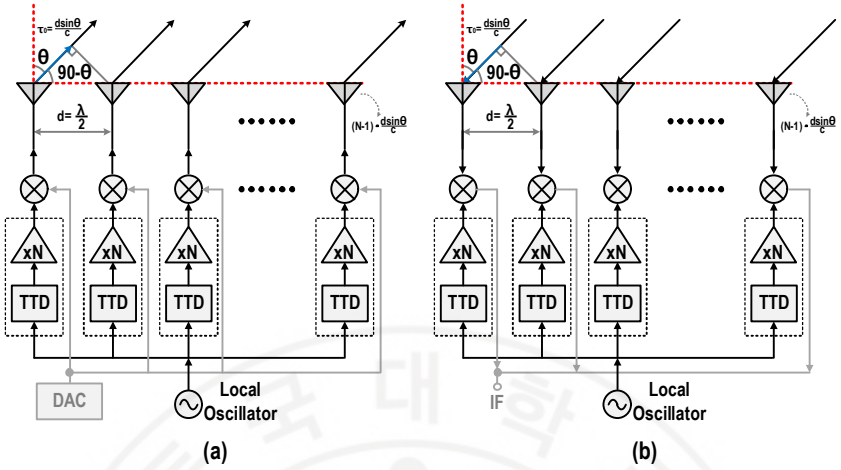

Figure 4.1-1 Proposed LO Path Time Delaying beamformer architecture: (a) Transmitter, (b) Receiver

realization of the proposed architecture presented in [4.2] that maximizes the advantages of the LO beamformer while compensating for its drawbacks. The core idea of the invention is to place the TTD in a low-frequency signal path that is 1/N times the final LO frequency, and then upscale it to the final LO frequency using a frequency multiplier. The proposed approach is described in detail in Section 4.1.1 and 4.1.2. Figure 4.1-1 illustrates the basic architecture of the LO Time Delaying phased-array beamformer realized in this thesis. Both the transmitter and receiver share the core idea of applying a TTD to a low-frequency signal, which is 1/N of the final LO frequency, and then generating the target LO frequency via a frequency multiplier (xN).

Table 4.1-1 A Simplified Comparison of Beamforming Architectures

	Advantage	Disadvantage	True Time Delay (TTD) Applicability
RF	- No need for separate I/Q phase - Spatial filtering relaxes mixer linearity requirements	- Extremely high insertion loss above 100 GHz, degrading system efficiency - Variable loss requires complex compensation circuits	- Theoretically possible, but practically unusable in sub-THz due to massive (>20 dB) insertion loss
LO	- Phase shifter linearity and bandwidth are not critical RF - No extra loss in the RF signal path improves power efficiency and reduces chip size.	- Requires a highly linear mixer due to the lack of spatial filtering - I/Q signal distribution can be susceptible to noise	- LO TTD ($\theta_{LO}=\omega_{LO}\times\tau_{d(LO)}$) causes minor beam squint, but the effect is negligible in the sub-THz band due to its high center frequency
IF	- Allows for low-loss, high-resolution phase shifters at a lower frequency	- Requires a highly linear mixer - Designing a wideband, high-linearity IF phase shifter is technically difficult	- Impractical, as it worsens beam-squint due to the $\Delta\omega/\omega_{IF}$ term and requires a larger time delay increased by a factor of ω_{RF}/ω_{IF}.

4.1.1 Preserving Time Delay Through Frequency Multiplier

To address the high insertion loss that occurs when implementing TTDs directly in the Sub-THz band, a new architecture is proposed in [4.2], which preserves the time delay value at a low frequency by utilizing a frequency multiplier. This principle can be explained by considering a low-frequency signal (ω_{LO}/N) with an applied time delay ($\tau_{d(LO)}$) at the input of an N-times frequency multiplier. The phase of this input signal ($\theta_{LO(IN)}$) is expressed as shown in Equation (4.1).

$$\theta_{LO(IN)} = \frac{\tau_{d(LO)}\omega_{LO}}{N} \tag{4.1}$$

Since a frequency multiplier amplifies the entire phase of the input signal by a factor of N, not just its frequency, the phase of the output signal ($\theta_{LO(OUT)}$) is formulated as shown in Equation (4.2).

$$\theta_{LO(OUT)} = N \times (\frac{\tau_{d(LO)}\omega_{LO}}{N}) = \tau_{d(LO)}\omega_{LO} \tag{4.2}$$

Equation (4.2) mathematically demonstrates that the effective time delay at the final output frequency (ω_{LO}) is identical to the initial time delay ($\tau_{d(LO)}$) applied at the multiplier's input.

By leveraging the fact that the time delay is preserved through frequency multiplication, we can design a high-efficiency,

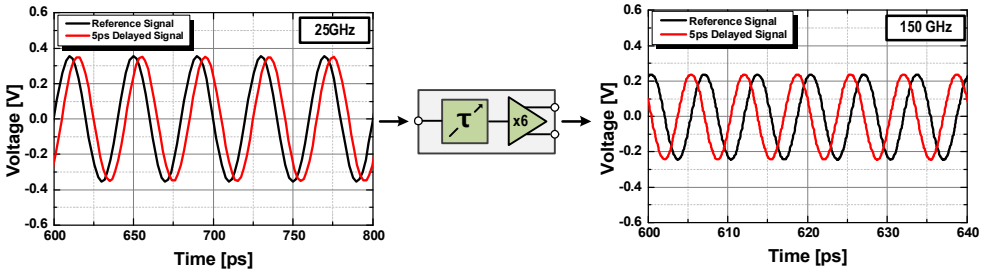

Figure 4.1-2 Comparison of a 5ps Time Delay Before (25GHz) and After (150GHz) Frequency Multiplication

low-loss TTD circuit at a 1/N lower frequency instead of at the challenging high frequency. The core approach of this research is to generate a precise time-delayed signal at this low-frequency stage, multiply it to a high frequency to use as the LO signal, and thereby implement effective RF beamforming.

Figure 4.1-2 presents the simulation results for the TTD and 6x frequency multiplier designed in a 28nm FDSOI process for this research, visually demonstrating the time delay preservation characteristic proven in Equation (4.1-2). The left waveform shows the 25 GHz reference signal at the input of the 6x frequency multiplier and the signal delayed by 5ps via the TTD. Observing the right waveform, which is after the signal has passed through the 6x multiplier, it is clear that while the signal's frequency has increased sixfold to 150 GHz, the time difference between the reference and delayed signals is identically maintained at 5ps.

4.1.2 RF Phase Alignment via LO-Path Time Delaying

The core principle of the proposed LO Time Delaying method is to align the phase of the RF signals radiated from each antenna element in a specific direction, θ. To form a beam in a phased-array antenna, it is necessary to compensate for the RF signal's time delay, τ_{RF}, which arises from the physical path difference between the elements. As shown in Figure 4.1-1, when the spacing between antenna elements is d=λ/2, the required RF time delay between adjacent elements is calculated as follows[4.2]:

$$\tau_{RF} = \frac{d\sin\theta}{c} = \frac{(\lambda/2)\sin\theta}{c} \tag{4.3}$$

To cancel out the phase shift caused by this RF-path time delay, an intentional time delay, τ_{LO}, must be introduced in the LO path to generate a phase shift of the same magnitude. This phase alignment condition is expressed in Equation (4.4)[4.2].

$$\omega_{LO}\tau_{LO} = \omega_{RF}\tau_{RF} \tag{4.4}$$

Here, ω_{LO} and ω_{RF} represent the angular frequencies of the LO and RF signals, respectively. Therefore, the final time delay (τ_{LO}) that must be applied to the LO path of each antenna channel can be calculated using Equation (4.5).

$$\tau_{LO} = \tau_{RF} \times \frac{\omega_{RF}}{\omega_{LO}} \tag{4.5}$$

Based on this relationship, by precisely controlling the necessary time delay for each antenna in the low-loss, low-frequency LO stage, the final high-frequency RF output signals are made to combine in-phase in the target direction, thus achieving effective beam steering.

4.1.3 Calculation of Required Maximum System Delay

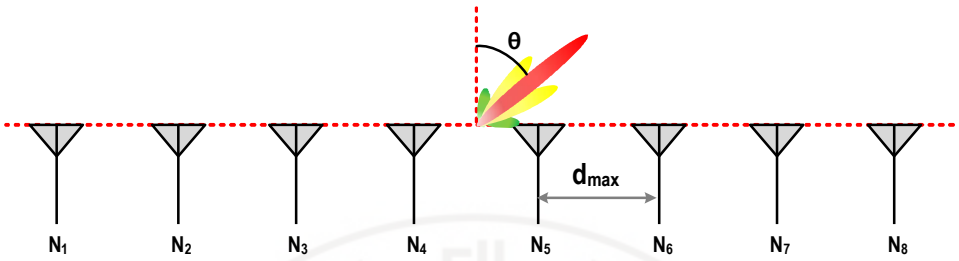

Figure 4.1-3 Architecture of an 8-element Uniform Linear Array (ULA) antenna

In an 8-element phased-array antenna system configured as a Uniform Linear Array (ULA), as shown in figure 4.1-3, the maximum time delay (τ_{max}) that the True Time Delay (TTD) must provide is determined by the system's maximum beam steering angle (θ_{max}) and the inter-element spacing (d). The inter-element spacing (d) can be determined from the condition to suppress the occurrence of grating lobes. Assuming a maximum beam steering angle of 60° at a frequency of 156.5 GHz, the maximum inter-element spacing (d_{max}) to prevent grating lobes is calculated to be approximately 2.21 mm.

In this study, the TTD was designed to target the physical maximum steering angle that the phased-array system can achieve—a 90° beam steering (end-fire) condition—going beyond the basic 60° steering range for the communication link. The maximum time delay (τ_{max}) required for the end-fire condition

(θ_{max}=90◦) can be recalculated as follows in Equation (4.6) [4.3] [4.4]:

$$\tau_{\max} = \frac{(N-1)d_{\max}\sin\theta}{c} \approx 51.8ps \quad (4.6)$$

Therefore, the TTD circuit designed in this study was implemented to provide the 51.8 ps of delay required for end-fire steering in order to verify the system's maximum performance. Given an RF frequency of 156.5 GHz and an LO frequency of 150 GHz, the actual maximum time delay that needs to be implemented in the LO path (τ_{LO}), according to Equation (4.5), is calculated as follows to be approximately 54 ps.

$$\tau_{LO\max} = 51.8ps \times \frac{156GHz}{150GHz} \approx 54ps \quad (4.7)$$

4.2 Proposed D-Band Transceiver with LO-Path Time Delaying

4.2.1 Proposed Architecture and Design of Core Building Blocks

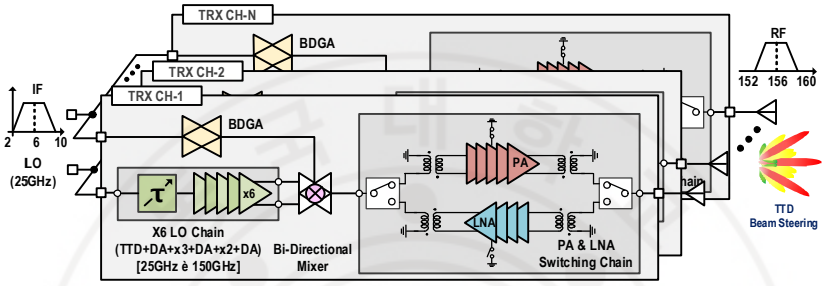

Figure 4.2-1 Architecture of the proposed 156 GHz transceiver applying the LO Time Delaying technique

Figure 4.2-1 shows the overall block diagram of a single transceiver (TRX) channel, which is the core of the 156 GHz beamforming system designed in a 28nm FDSOI process. This channel adopts a bi-directional architecture to enhance circuit integration and utilize chip area efficiently by sharing parts of the transmit (TX) and receive (RX) paths for Time-Division Duplexing (TDD) operation. In the core LO Time Delaying chain, a 25 GHz low-frequency LO signal has a time delay applied by the TTD (τ) before being converted to the 150 GHz LO signal required for mixer operation via a 6x frequency multiplier. In TX mode, an IF signal in the 2-10 GHz band is amplified by the Bi-Directional Gain Amplifier (BDGA), up-converted to the 152-160 GHz RF band by the bi-directional mixer, and then routed through the switching

chain to the Power Amplifier (PA) for final amplification before being transmitted to the antenna. Conversely, in RX mode, the RF signal received from the antenna is amplified by the Low-Noise Amplifier (LNA) via the switching chain, then down-converted to an IF signal by the bi-directional mixer, and finally output through the BDGA. Such an architecture effectively integrates the proposed LO Time Delaying beamforming technique into a compact, TDD-based single-channel transceiver.

Figure 4.2-2 shows the schematics of the core building blocks that constitute the transceiver channel shown in Figure 4.2-1. Each block was designed using a Samsung 28nm FDSOI process, with responsibilities divided among colleagues for efficient design. In this project, I designed the True Time Delay (TTD) buffer and x6 frequency multiplier for the LO chain, along with the Low-Noise Amplifier (LNA), Power Amplifier (PA), and bidirectional mixer for the RF chain.

Figure 4.2-2 (b) is a 25 GHz TTD buffer amplifier designed to compensate for the signal loss occurring in the TTD cell and to drive the subsequent frequency multiplier stage. It consumes 18mW and is designed to provide a high gain of 15dB at its 25 GHz operating frequency. To efficiently achieve this high gain, the circuit adopts a two-stage common-source (2-stage CS) amplifier architecture. Each amplification stage utilizes an inductive load to enhance gain and bandwidth by resonating with the transistor's

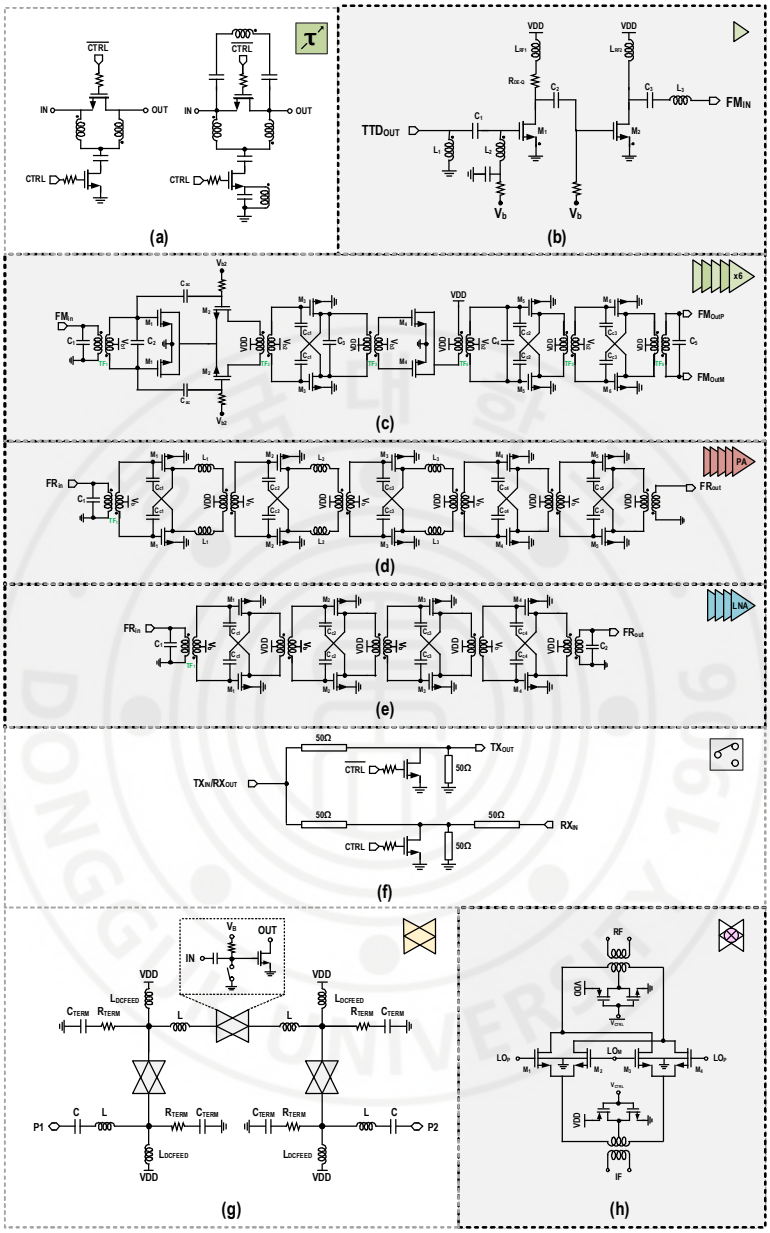

Figure 4.2-2 Schematics of the core building blocks for the proposed beamformer, including (a) the True Time Delay (TTD) cell, (b) the TTD output buffer, (c) the x6 frequency multiplier, (d) the 156 GHz power amplifier (PA), (e) the 156 GHz low-noise amplifier (LNA), (f) the 156 GHz T/R switch, (g) the bi-directional mixer and IF amplifier, and (h) the Gilbert-cell mixer.

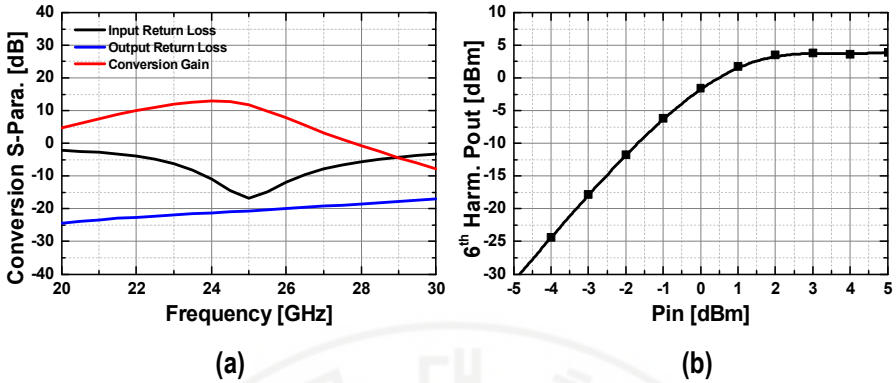

Figure 4.2-3 Simulation results of the x6 frequency multiplier: (a) Conversion gain and input/output return loss, (b) 6th harmonic output power

parasitic capacitance, and sophisticated L-C matching networks are applied at the input and output to minimize signal reflection.

Figure 4.2-2(c) shows the detailed schematic of the x6 frequency multiplier, a key block in the LO Time Delaying chain. To up-convert the 25 GHz input signal to the final 150 GHz LO signal, the circuit was designed with a five-stage cascaded architecture consisting of a frequency tripler, a driving amplifier, a frequency doubler, and two final driving amplifier stages.

The first stage, the Tripler, utilizes a self-mixing Gilbert-cell-like structure to generate the third harmonic component of the input signal, resulting in a 75 GHz signal. After passing through a driving amplifier, the signal is fed to the Doubler stage. The Doubler function, instead of a push-pull structure, is implemented by operating a differential amplifier in its non-linear region to generate

the second harmonic (150 GHz), which is then selectively amplified by a transformer-based resonant load. The final two driving amplifier stages serve to reliably amplify the 150 GHz signal to achieve the target output power. According to the simulation results in Figure 4.2-3, the proposed x6 frequency multiplier achieves a peak conversion gain of 12 dB and a saturated output power (Psat) of 4.5 dBm, with a total power consumption of 38 mW.

Figure 4.2-2(d) shows the schematic of the power amplifier (PA) operating in the 156 GHz band. To achieve high output power and gain, it was designed with a 5-stage architecture consisting of five cascaded push-pull differential amplifiers. The impedance matching and signal coupling between each amplification stage were efficiently implemented using transformers. According to the simulation results in Figure 4.2-4, this PA consumes 50 mW of power and achieves a peak gain of 22 dB and a power-added efficiency (PAE) of 6% at 156 GHz.

Figure 4.2-2(e) is the schematic of the 156 GHz low-noise amplifier (LNA), which determines the receiver's performance. To secure sufficient gain and optimize the noise figure, the LNA adopts a 4-stage architecture of four cascaded push-pull differential amplifiers. Similar to the PA, the matching between stages is transformer-based. This LNA consumes 36 mW of power and, as shown in the simulation results of Figure 4.2-5, achieves a peak gain of approximately 20 dB and a noise figure (NF) of 9.5 dB in the

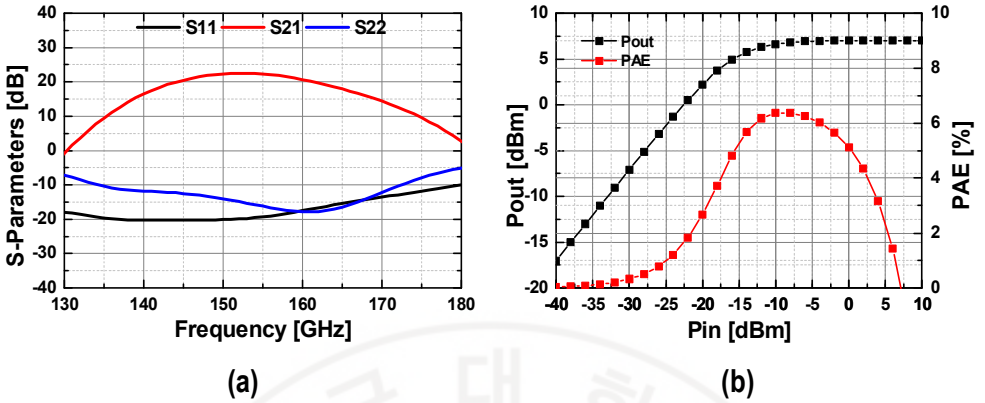

Figure 4.2-4 Simulation results of the power amplifier (PA): (a) S-parameters, (b) Output power (Pout) and power-added efficiency (PAE) at 156 GHz

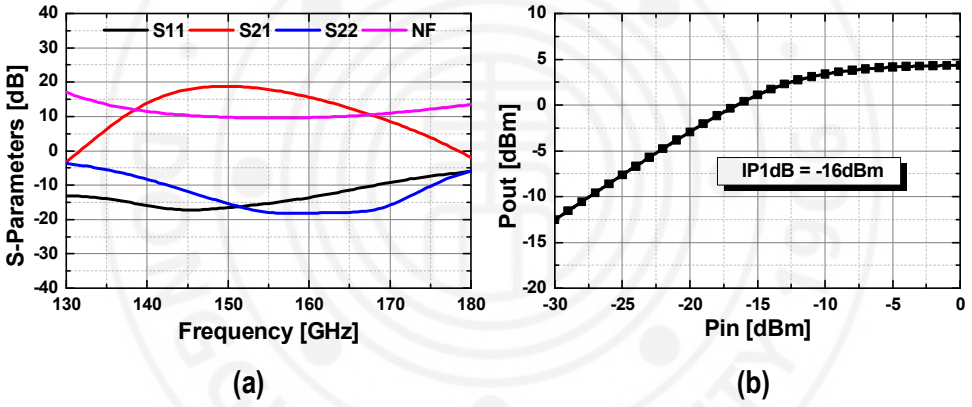

Figure 4.2-5 Simulation results of the low-noise amplifier (LNA): (a) S-parameters and noise figure (NF), (b) Input P1dB at 156 GHz

156 GHz band.

Figure 4.2-2 (h) shows the schematic of the bi-directional mixer, which is a key component of the bi-directional architecture where the transmitter and receiver share a common path. It is fundamentally based on a double-balanced mixer structure

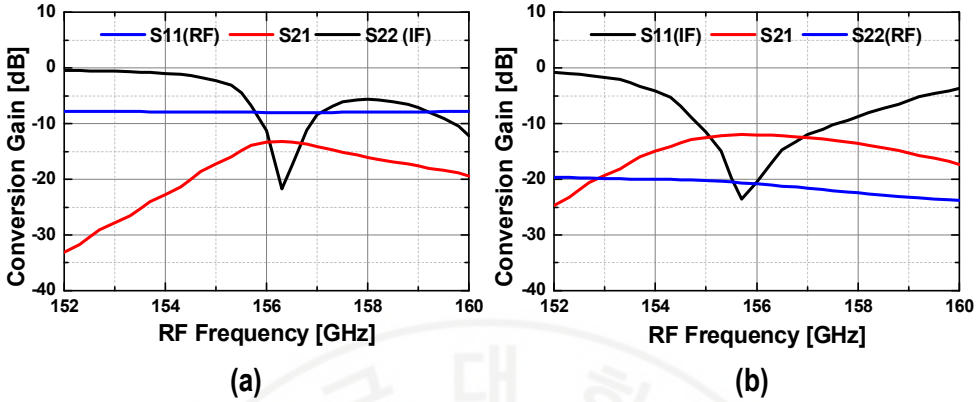

Figure 4.2-6 Simulation results of the bi-directional mixer: (a) Down-conversion mode, (b) Up-conversion mode

composed of a four-transistor switching quad controlled by a differential LO signal. Both the RF and IF ports are impedance-matched using transformers. The key feature of this mixer is that its operational direction is controlled by switching the VDD power supply. In transmit (TX) mode, the control signal (Vctrl) applies VDD to the center tap of the RF transformer to up-convert the IF signal to RF. Conversely, in receive (RX) mode, VDD is applied to the center tap of the IF transformer to down-convert the RF signal to IF. The performance simulation results for this bi-directional operation are presented in Figure 4.2-6. Sub-figure (a) shows the conversion gain and return loss characteristics for down-conversion, while (b) shows the characteristics for up-conversion, confirming that stable performance is achieved in both modes using a single mixer core.

Figure 4.2-7 shows the total layout of the proposed LO-path

time delaying 156GHz transceiver. The chip was designed using a 28nm FDSOI process, and the layout area of the core circuit blocks, excluding the pads, is 1100μm x 1980μm.

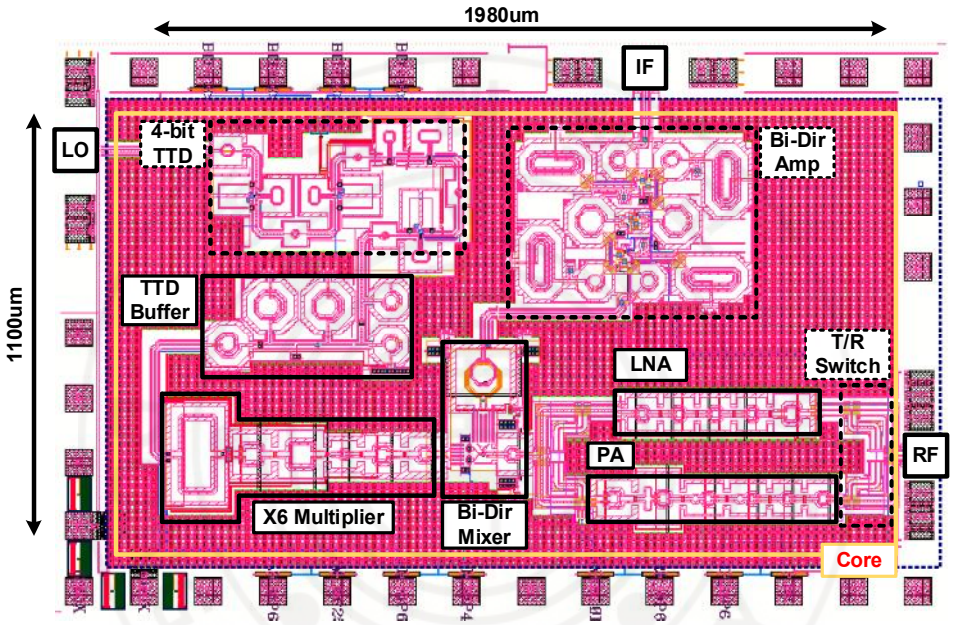

Figure 4.2-7 Total layout of proposed LO-path time delaying 156GHz Transceiver in 28nm FDSOI (Solid: My Work, Dash: Coworker Work)

4.2.2 Transceiver Simulation Results

Figure 4.2-8 shows the performance simulation results for the receiver (Rx) mode of the proposed transceiver. The down-conversion gain in figure (a) achieves a peak of 27 dB in the 156 GHz band. Figure (b) shows the output spectrum, indicating that when an RF signal of -25 dBm is input, the final IF output signal is converted to 5 dBm. The total power consumption in receiver mode is 140 mW.

Figure 4.2-9 shows the performance simulation results for the transmitter (Tx) mode. As can be seen in figure (a), the up-conversion gain shows a peak performance of 20 dB. Through the output spectrum in figure (b), it can be confirmed that when an IF signal of -25 dBm is input, the final RF output signal is amplified to 3.5 dBm for transmission. The total power consumption in transmitter mode is 153 mW.

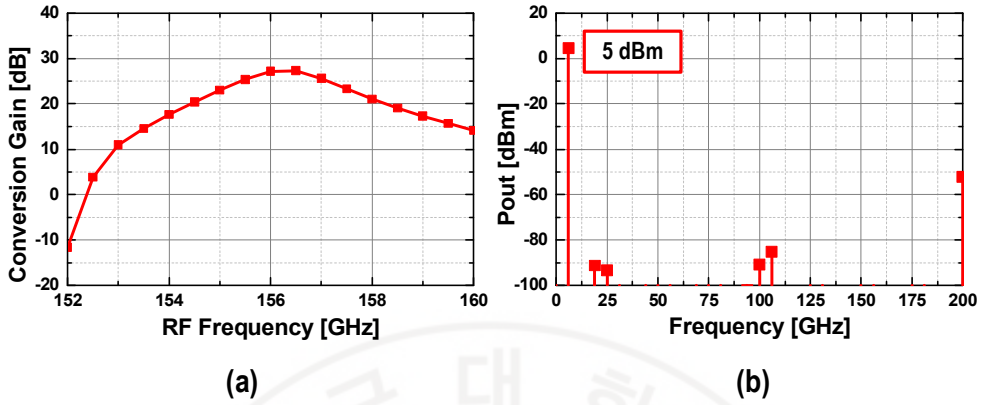

Figure 4.2-8 Simulation results of the receiver (Rx) mode performance: (a) Down-conversion gain, (b) Output spectrum and harmonic components

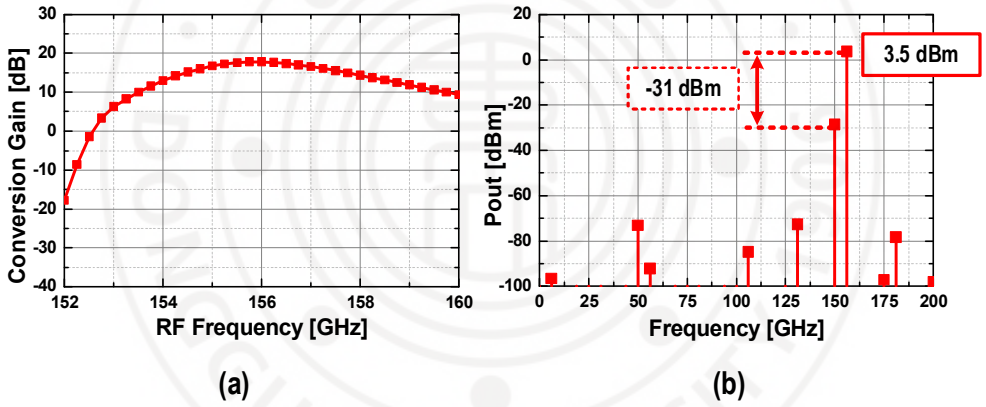

Figure 4.2-9 Simulation results of the transmitter (Tx) mode performance: (a) Up-conversion gain, (b) Output spectrum and harmonic components

4.2.3 Comparison with other D-Band Beamformer

Table 4.2-1 compares the performance of the transceiver proposed in this work with other state-of-the-art D-band beamformer research. Unlike the other compared works, which use conventional RF or IF Phase Shifter (PS) methods, this work is differentiated by being the world's first implementation of the LO-path Time Delaying (LO TTD) beamforming technique in a 28nm SOI process.

The most notable achievement is the world-class energy efficiency. The transmitter and receiver in this work achieve efficiencies of 20.4 pJ/bit and 18.65 pJ/bit, respectively, which are significantly superior to any other results in the comparison. This high efficiency is supported by the lowest power consumption per channel, at 153 mW for TX and 140 mW for RX.

Furthermore, the smallest chip area of 2.2 mm^2 proves that the proposed architecture also excels in terms of integration. The results of this work clearly demonstrate that the proposed LO TTD architecture is highly optimized for power efficiency and miniaturization, making it a very suitable technology for implementing 6G D-band terminals.

Table 4.2-1 Comparison table of D-Band beamformer (under fabrication)

Ref		This Work*	[4.5] ISSCC 2022	[4.6] JSSC 2022	[4.7] JSCC 2022	[4.8] RFIC 2020
Tech		**28nm SOI**	130nm SiGe BiCMOS	45nm SOI	45nm SOI	130nm SiGe BiCMOS
Integration		**1T1R**	4T & 4R	8T	8R	1T & 1R
Beamforming Type		**LO TTD**	RF PS	IF PS	IF PS	RF PS
Freq [GHz]		**152-160**	130-164	137-149	139-155	130-160
TX Psat [dBm]		**5**	12	12	-	11
Rx Gain [dB]		**27**	30	-	26.5	22
RX NF [dB]		**15**	7.57.5	-	6.4	10
Area [mm^2]		**2.2†**	4.45	27.54	24.91	4‡
Power / Channel [mW]	TX	**153**	265	231	-	330
	RX	**140**	200	-	145	165
Modulation		**64-QAM**	64-QAM	64-QAM	64-QAM	Not reported
Eff. / Element [pJ/bit]	TX	**20.4**	35.32	115.2	-	
	RX	**18.65**	26.67	-	116	

* Simulation Result

† Excluding pad size

‡ The sum of Tx Chip and Rx Chip

4.3 Reference

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Chapter 5. Future Work

Based on the design results and simulation outcomes derived from this study, the following future research directions are proposed.

First, by applying the high-density and high-resolution hybrid TTD technology proposed in Chapter 2 to a practical transceiver architecture, we propose the design of a high-density TTD beamformer-based transceiver capable of suppressing beam squint even in wideband signal environments.

Furthermore, we propose the implementation of a high-power TRM system that integrates the 4-channel MFC discussed in Chapter 3 with compound semiconductor-based power amplifiers, low-noise amplifiers, and T/R switches into a single module.

Finally, for the D-Band LO path time-delaying transceiver beamformer currently under fabrication, we plan to conduct precise measurements and performance analysis upon its completion to verify the design validity. Subsequently, we propose a study to expand the existing single-channel structure into a multi-channel system (four channels or more) and to evaluate and optimize the performance of the final D-Band beamforming system integrated with an array antenna.

국문 초록

빔포밍은 다중 안테나 배열을 구성하는 각 요소의 위치별 신호전달 시 발생하는 시간지연에 따른 위상차를 정밀 제어하여 신호를 원하는 방위로 집속하는 기술이다. 이 기술은 능동전자조향배열 (Active Electronically Scanned Array)형 고성능 레이더 시스템 구현에 핵심적인 역할을 수행하며, 차세대 무선통신 시스템에 있어서는 MIMO(Multiple-Input Multiple-Output) 기술을 통해 공간 다중화와 간섭 억제를 달성하고 여러 독립 채널의 동시 신호 처리를 가능케 하여 통신 용량과 커버리지를 대폭으로 향상할 수 있다. 빔포밍을 구현하는 하드웨어는 주로 위상변위기(phase shifter, PS)와 실시간 시간지연기(true time delay, TTD)로 구성되며, 전자는 안테나 요소별 시간지연에 따른 위상 보상을, 후자는 안테나 요소간 경로에 따른 시간 지연 보상을 담당한다. 본 석사학위 논문은 RF 빔포밍 소자인 실시간 시간지연기(TTD)의 고성능/ 소형화 구현 연구를 수행하였으며, 제 6세대(6G) 무선통신용 하드웨어의 성공적인 구현을 위한 핵심 기술인 빔포머를 초고주파 (FR3) 대역과 서브테라헤르츠 (156GHz) 대역에서 상용 CMOS 공정으로 각각 설계하였다. 초고주파 대역 4채널 빔포머는 65nm CMOS 공정으로 FR3 대역 (8-11GHz)에서 스위치형 위상변위기와 디지털 가변감쇠기를 집적화하여 4mm*3.5mm의 소형화를 달성하였고, 서브테라헤르츠 대역 (156GHz) 빔포밍 송수신기는 28nm CMOS 공정으로 초고주파 TTD와 6채배기를 이용하여 고효율 LO 위상변위 기술을 구현하였다.

1장 : 본 장에서는 6G 후보 대역인 FR3 및 서브테라헤르츠(sub-THz) 대역의 동향과, 위상 배열 안테나 및 빔포밍을 구현하는 핵심 하드웨어인 위상 천이기(PS)와 실시간 시간지연기(TTD)를 개관한다.

2장 : 본 장에서는 CMOS 28 nm FDSOI 공정으로 9–11 GHz에서 동작하는 X-band 6-bit 하이브리드 실시간 시간 지연기(TTD)의 설계를 다룬다. TTD는 기존의 위상변위기의 문제점인 광대역 신호전송에서 발생하는 빔스퀸트 (Beam-squint) 현상을 근본적으로 해결할 수 있으나, 종래의 TTD는 최대 지연시간이 짧고, 선형 제어가 어려우며, 삽입손실이 클 뿐만 아니라, 크기가 큰 단점이 있다. 제안된 하이브리드 TTD는 소지연 단계(1.56, 3.125, 6.25, 12.5 ps)는 SPDT/DPDT 스위치망을 적용하고, 대지연 단계(25, 50, 75 ps)는 SPNT 선택망과 Gm-C 전대역 통과 필터를 결합하여 긴 지연 시간을 선형적으로 정밀하게 제어가 가능하도록 구성하였다. 구현된 회로는 측정결과, 9 GHz에서 이득 편차 9 dB를 보이며, 9–11 GHz 전 대역에서 반사손실 ≥ 10 dB($-|S11| \leq -10$ dB)를 만족한다. 총 전력 소모는 13.53 mW, 실리콘 면적은 0.54 mm^2이다. 지연 해상도는 최대 지연 대비 1.56%로 높은 분해능을 제공하며, 비교표 대비 최고 수준의 FoM(Figure-of-Merit)을 달성하였다.

3장 : 본 장에서는 65-nm bulk CMOS로 제작된, 패드 레벨 ESD 보호를 포함하여 2.85 mm^2를 차지하는 완전 집적된 4채널 X-밴드 다기능 칩(MFC)을 제시한다. 3.3V 동작을 가능하게 하기 위해, 증폭기 코

어는 3-스택 소자 토폴로지를 채택한다. 교차 결합된 Rn-Cn 피드백을 가진 양방향 이득 증폭기는 안정성과 대역폭을 개선하며, 반면 트랜스포머 인터페이스에서의 스위칭 가능한 션트 커패시터들은 최소한의 손실로 공진 정합을 실현한다. 위상 변위기는 전송 선로 지연을 사용하며, 낮은 삽입 손실과 DPDT 미스매치의 효과적인 제거를 달성하여 정밀한 제어와 함께 컴팩트한 구현을 가능하게 한다. 측정된 소신호 성능은 송신 모드에서 9.5 dB, 수신 모드에서 9 dB의 피크 이득을 확인해주며, 3-dB 대역폭은 각각 8.5–9.7 GHz와 8.2–9.8 GHz이다. 수신 경로 잡음 지수(NF)는 9 GHz에서 6.2 dB이다. 위상 변위기는 DPDT 튜닝으로 2.7° 이내의 RMS 위상 오차를 달성하고, 감쇠기는 트리밍 비트를 사용하여 0.55 dB 이내의 RMS 이득 오차를 달성하여 높은 제어 정확도를 보여준다. 선형성은 8–10 GHz에서 −14.8 dBm보다 나은 IP1dB로 검증되었다. 채널당 소비 전력은 200 mW(Tx)와 135 mW(Rx)이다.

4장 : CMOS 28 nm FDSOI 공정으로 25GHz True-Time-Delay(TTD)를 6채배기와 함께 LO단에 적용하여 LO 경로에 빔포밍을 적용한 고효율 156 GHz 송수신기를 설계하였다. TTD 회로는 주파수 체배기 이전의 저주파 구간에 배치하여 지연기의 삽입 손실을 최소화하여 효율을 높였으며, 체배 후 생성된 고주파 LO를 믹서에 인가해 채널별 RF 위상을 정렬하여 빔포밍을 구현한다. 아키텍처는 IF 체인의 양방향 증폭기(BDGA), LO 체인의 TTD와 ×6 주파수 체배기, RF 체인의 송수신 스위치(T/R switch, TRSW)·전력 증폭기(PA)·저잡음 증폭기

(LNA)로 구성되며, 주파수 변환부는 트랜스포머 기반 VDD 스위칭을 이용한 양방향 믹서로 구현하였다. 시뮬레이션 결과, 동작 대역은 150–160 GHz, 최대지연시간은 53.7ps, 송신 포화출력(Psat)은 5 dBm, 수신 변환이득은 27 dB, 수신 저잡음지수(NF)는 15 dB를 달성하였다. 칩 면적은 2.47 mm² 이며, 전력 소모는 송신 시 153 mW, 수신 시 140 mW이다.